

SN74LV240A Octal Inverting Buffers/Drivers With 3-State Outputs

1 Features

- V_{CC} operation of 2V to 5.5V
- Max t_{pd} of 6.5ns at 5V
- Typical V_{OLP} (output ground bounce) <0.8V at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- Typical V_{OHV} (output V_{OH} undershoot) >2.3V at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- Support mixed-mode voltage operation on all ports
- Latch-up performance exceeds 250mA per JESD 17
- I_{off} supports live insertion, partial power-down mode, and back drive protection

2 Applications

- Handset: Smartphone
- Network Switch
- Health and Fitness / Wearables

3 Description

These octal buffers/drivers with inverted outputs are designed for 2V to 5.5V V_{CC} operation.

The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LV240A	DGV (TVSOP, 20)	5 mm × 6.4 mm	5mm × 4.4mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



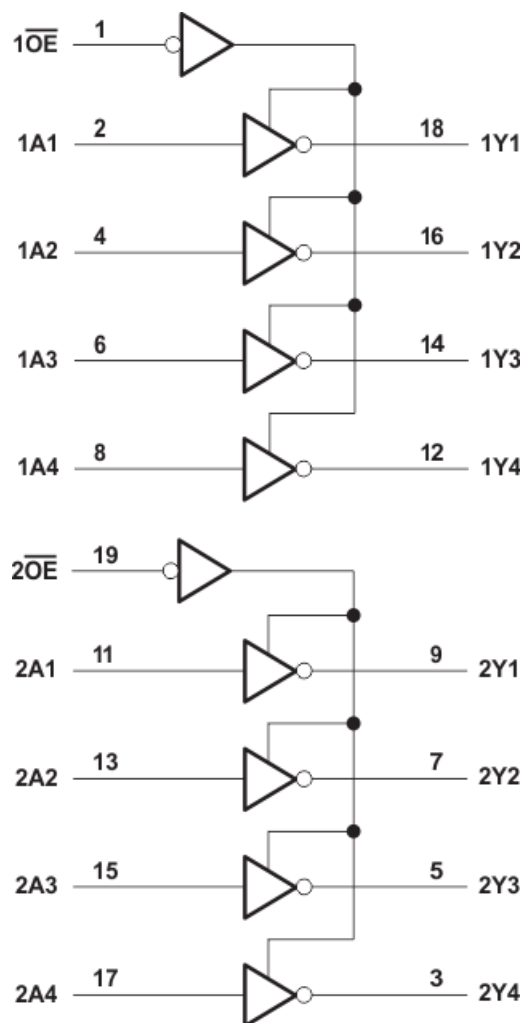


Table of Contents

1 Features	1	7.2 Functional Block Diagram.....	11
2 Applications	1	7.3 Feature Description.....	12
3 Description	1	7.4 Device Functional Modes.....	12
4 Pin Configuration and Functions	4	8 Application and Implementation	13
5 Specifications	5	8.1 Application Information.....	13
5.1 Absolute Maximum Ratings	5	8.2 Typical Application.....	13
5.2 ESD Ratings.....	5	8.3 Power Supply Recommendations.....	14
5.3 Recommended Operating Conditions.....	6	8.4 Layout.....	14
5.4 Thermal Information.....	6	9 Device and Documentation Support	15
5.5 Electrical Characteristics.....	7	9.1 Documentation Support (Analog).....	15
5.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	7	9.2 Receiving Notification of Documentation Updates....	15
5.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	7	9.3 Support Resources.....	15
5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	9.4 Trademarks.....	15
5.9 Noise Characteristics.....	8	9.5 Electrostatic Discharge Caution.....	15
5.10 Operating Characteristics.....	8	9.6 Glossary.....	15
5.11 Typical Characteristics.....	9	10 Revision History	15
6 Parameter Measurement Information	10	11 Mechanical, Packaging, and Orderable Information	16
7 Detailed Description	11		
7.1 Overview.....	11		

4 Pin Configuration and Functions

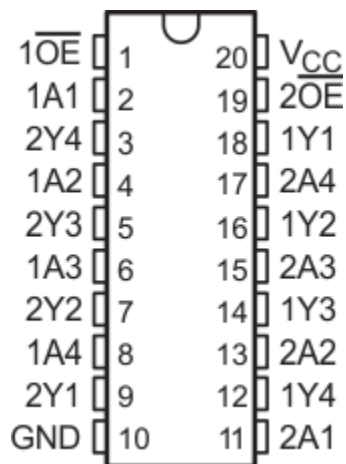


Figure 4-1. SN74LV240A DB, DGV, DW, NS, or PW Package; 20-Pin SSOP, TVSOP, SOIC, SOP, or TSSOP (Top View)

Table 4-1. Pin Functions

NAME ⁽¹⁾	PIN	TYPE	DESCRIPTION
1OE	1	I	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	—	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	I	Output enable 2
VCC	20	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		–0.5	7	V
V _I	Input voltage ⁽²⁾		–0.5	7	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	7	V
V _O	Output voltage ⁽²⁾ ⁽³⁾		–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–20	mA
I _{OK}	Output clamp current	V _O < 0		–50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	–35	35	mA
	Continuous current through V _{CC} or GND		–70	70	mA
T _{stg}	Storage temperature		–65	150	°C
T _J	Junction Temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value is limited to 5.5-V maximum.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
		Machine model (A115-A)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 to 2.7 V		V _{CC} × 0.3	
		V _{CC} = 3 to 3.6 V		V _{CC} × 0.3	
		V _{CC} = 4.5 to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V		–50	μA
		V _{CC} = 2.3 to 2.7 V		–2	mA
		V _{CC} = 3 to 3.6 V		–8	
		V _{CC} = 4.5 to 5.5 V		–16	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 to 2.7 V		2	mA
		V _{CC} = 3 to 3.6 V		8	
		V _{CC} = 4.5 to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 to 2.7 V		200	ns/V
		V _{CC} = 3 to 3.6 V		100	
		V _{CC} = 4.5 to 5.5 V		20	
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DW (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	UNIT
		20 PINS					
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	79.2	94.5	116.2	76.7	128.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.7	56.4	31.2	43.2	70.5	
R _{θJB}	Junction-to-board thermal resistance	47.0	49.7	57.7	44.2	79.3	
Ψ _{JT}	Junction-to-top characterization parameter	18.6	18.5	0.9	16.8	23.4	
Ψ _{JB}	Junction-to-board characterization parameter	46.5	49.3	57.0	43.8	78.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	High level output voltage	I _{OH} = –50 µA	2 to 5.5 V	V _{CC} – 0.1			V
		I _{OH} = –2 mA	2.3 V	2			
		I _{OH} = –8 mA	3 V	2.48			
		I _{OH} = –16 mA	4.5 V	3.8			
V _{OL}	Low level output voltage	I _{OL} = 50 µA	2 to 5.5 V			0.1	V
		I _{OL} = 2 mA	2.3 V			0.4	
		I _{OL} = 8 mA	3 V			0.44	
		I _{OL} = 16 mA	4.5 V			0.55	
I _I	Input leakage current	V _I = 5.5 V or GND	0 to 5.5 V			±1	µA
I _{OZ}	Off-State (High-Impedance State) Output Current (of a 3-State Output)	V _O = V _{CC} or GND	5.5 V			±5	µA
I _{CC}	Supply current	V _I = V _{CC} or GND, I _O = 0	5.5 V			20	µA
I _{off}	Input/Output Power-Off Leakage Current	V _I or V _O = 0 to 5.5 V	0			5	µA
C _i	Input Capacitance	V _I = V _{CC} or GND	3.3 V		2.3		pF

5.6 Switching Characteristics, V_{CC} = 2.5 V ±0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	A	Y	C _L = 15 pF		6.3 ⁽¹⁾	11.6 ⁽¹⁾	1 ⁽²⁾	14 ⁽²⁾	ns
t _{en}	$\overline{OE}$				8.5 ⁽¹⁾	14.6 ⁽¹⁾	1 ⁽²⁾	17 ⁽²⁾	
t _{dis}	$\overline{OE}$				9.7 ⁽¹⁾	14.1 ⁽¹⁾	1 ⁽²⁾	16 ⁽²⁾	
t _{pd}	A	Y	C _L = 50 pF		8.2	14.4	1	17	ns
t _{en}	$\overline{OE}$				10.3	17.8	1	21	
t _{dis}	$\overline{OE}$				14.2	19.2	1	21	
t _{sk(o)}						2		2 ⁽³⁾	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) Value applies for SN74LV240A only

5.7 Switching Characteristics, V_{CC} = 3.3 V ±0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	A	Y	C _L = 15 pF		4.6 ⁽¹⁾	7.5 ⁽¹⁾	1 ⁽²⁾	9 ⁽²⁾	ns
t _{en}	$\overline{OE}$				6.2 ⁽¹⁾	10.6 ⁽¹⁾	1 ⁽²⁾	12.5 ⁽²⁾	
t _{dis}	$\overline{OE}$				8.3 ⁽¹⁾	12.5 ⁽¹⁾	1 ⁽²⁾	13.5 ⁽²⁾	

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	A	Y	C _L = 50 pF		5.9	11	1	12.5	ns
t _{en}	$\overline{\text{OE}}$				7.5	14.1	1	16	
t _{dis}	$\overline{\text{OE}}$				11.8	15	1	17	
t _{sk(o)}						1.5		1.5 ⁽³⁾	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
 (2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.
 (3) Value applies for SN74LV240A only

5.8 Switching Characteristics, V_{CC} = 5 V ±0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	A	Y	C _L = 15 pF		3.4 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽²⁾	6.5 ⁽²⁾	ns
t _{en}	$\overline{\text{OE}}$				4.6 ⁽¹⁾	7.3 ⁽¹⁾	1 ⁽²⁾	8.5 ⁽²⁾	
t _{dis}	$\overline{\text{OE}}$				7.4 ⁽¹⁾	12.2 ⁽¹⁾	1 ⁽²⁾	13.5 ⁽²⁾	
t _{pd}	A	Y	C _L = 50 pF		4.4	7.5	1	8.5	ns
t _{en}	$\overline{\text{OE}}$				5.6	9.3	1	10.5	
t _{dis}	$\overline{\text{OE}}$				9.7	14.2	1	15.5	
t _{sk(o)}						1		1 ⁽³⁾	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
 (2) This note applies to SN54LV240A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.
 (3) This values applies for SN74LV240A only

5.9 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.56		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		–0.49		
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		2.82		
V _{IH(D)}	High-level dynamic input voltage	2.31			
V _{IL(D)}	Low-level dynamic input voltage			0.99	

- (1) Characteristics are for surface-mount packages only.

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF f = 10 MHz	3.3 V	14	pF
			5 V	16.4	

5.11 Typical Characteristics

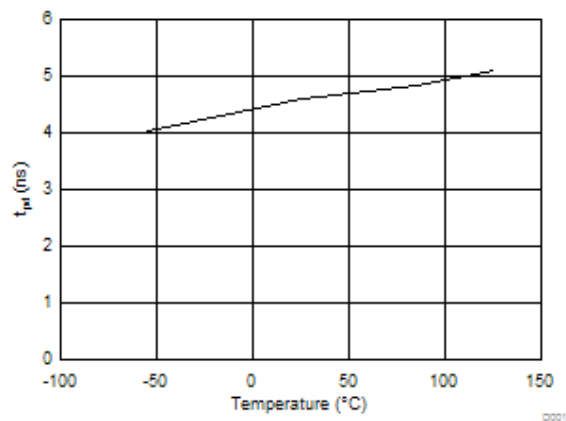


Figure 5-1. t_{pd} vs Temperature at 3.3-V V_{CC}

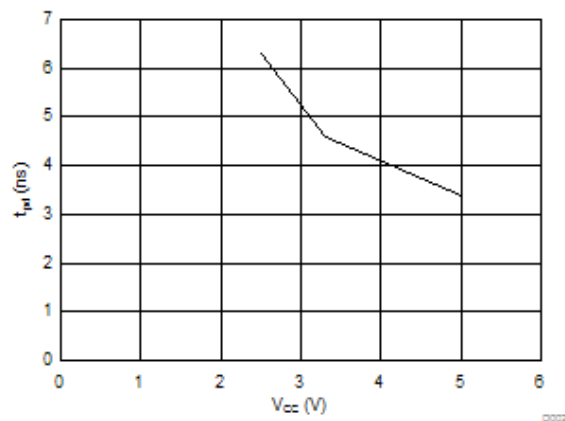
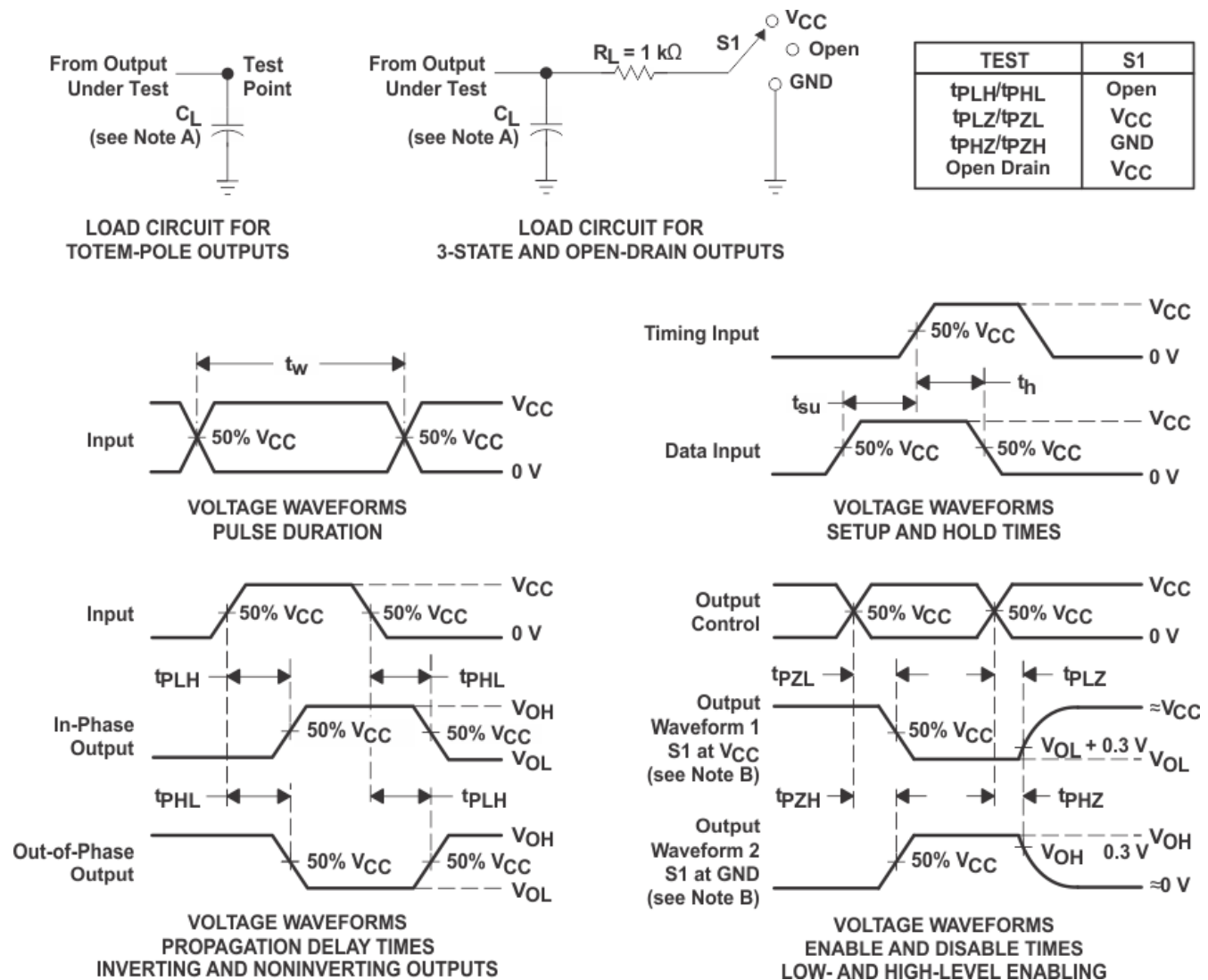


Figure 5-2. t_{pd} vs V_{CC} at 25°C

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These octal buffers/drivers with inverted outputs are designed for 2 V to 5.5 V V_{CC} operation.

The 'LV240A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

7.2 Functional Block Diagram

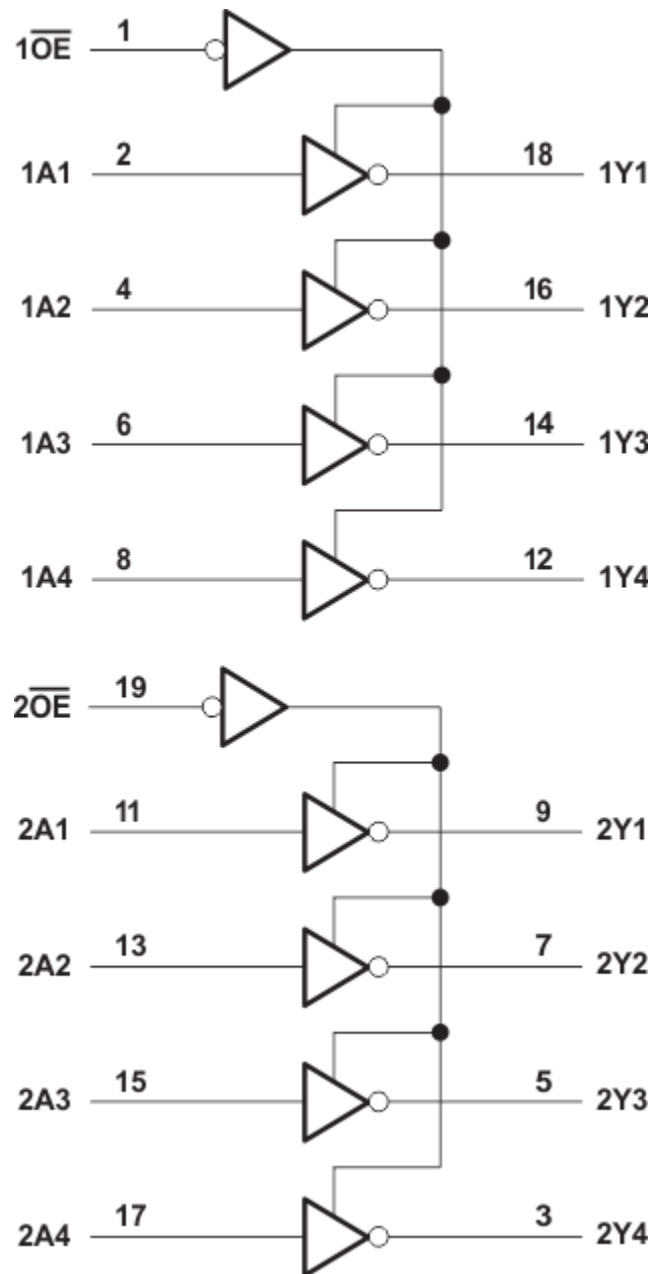


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- Wide operating voltage range operates from 2 V to 5.5 V operation
- Allow down voltage translation inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V

7.4 Device Functional Modes

**Table 7-1. Function Table
(Each Buffer)**

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
OE	A	Y
L	H	L
L	L	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LV240A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 8 mA of drive current at 3.3 V making it ideal for driving multiple outputs and low-noise applications. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC} .

8.2 Typical Application

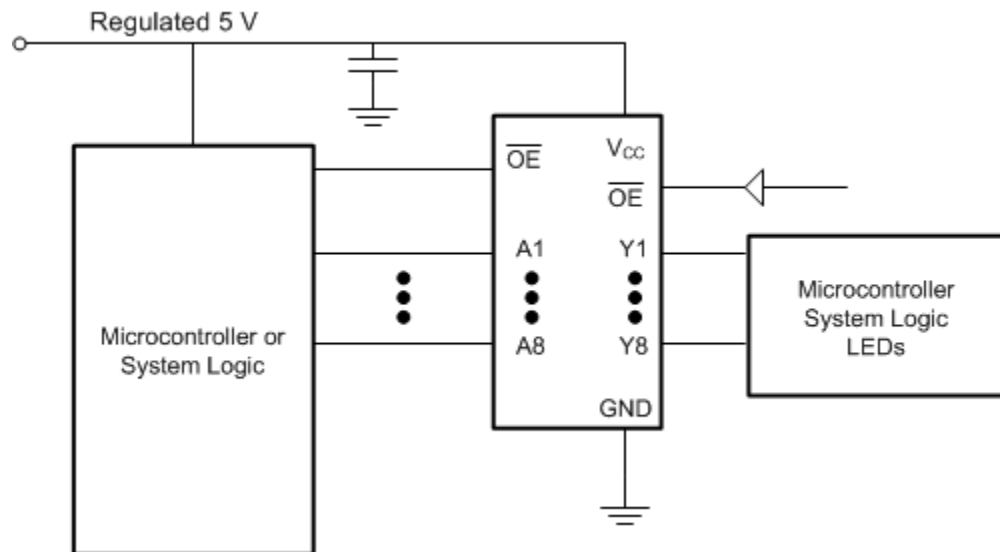


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
 - Rise time and fall time specifications see $(\Delta t/\Delta V)$ in [Section 5.3](#).
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in [Section 5.3](#).
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part
 - Outputs should not be pulled above V_{CC}

8.2.3 Application Curve

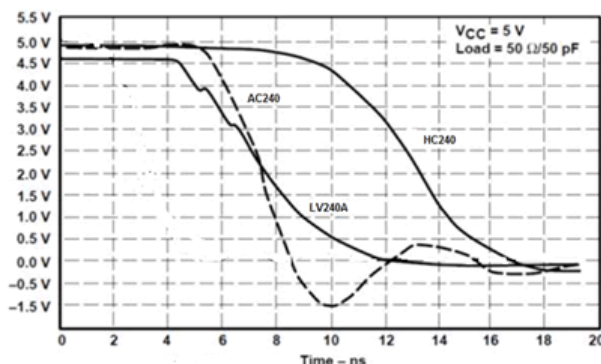


Figure 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [Section 5.3](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 μF and if there are multiple V_{CC} terminals, then TI recommends .01 μF or .022 μF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

8.4.2 Layout Example

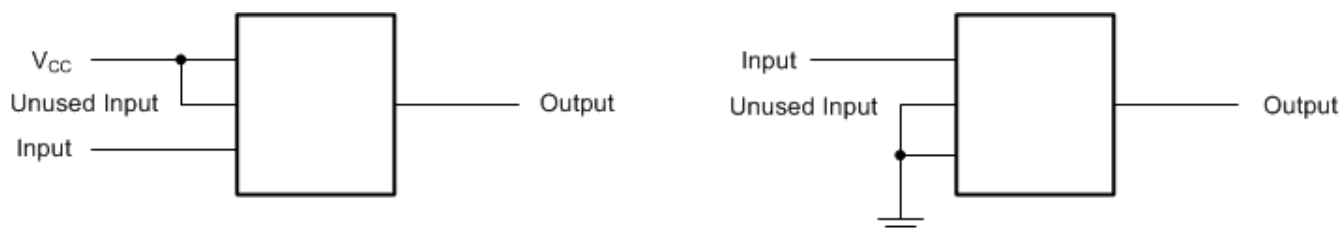


Figure 8-3. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV240A	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision J (December 2022) to Revision K (May 2024)	Page
• Updated format and body size in <i>Package Information</i> table	1
• Updated structural layout of document.....	1
• Updated thermal values for PW package from RθJA = 102.4 to 128.2, RθJC(top) = 36.5 to 70.5, RθJB = 53.6 to 79.3, ΨJT = 2.4 to 23.4, ΨJB = 52.9 to 78.9, all values in °C/W.....	6

Changes from Revision I (February 2015) to Revision J (December 2022)	Page
• Updated the format for tables, figures, and cross-references throughout the document.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV240ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ADBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ADBRE4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ADGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L240A
SN74LV240ADGSR.A	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L240A
SN74LV240ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ADGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	LV240A
SN74LV240ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV240A
SN74LV240ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV240A
SN74LV240APW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	LV240A
SN74LV240APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A
SN74LV240APWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV240A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV240ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV240ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV240ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV240ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV240ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV240APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV240ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV240ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV240ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LV240ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV240ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV240APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV240APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

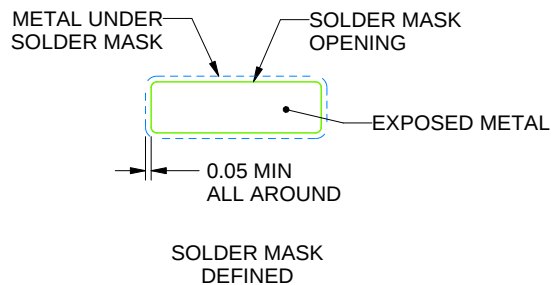
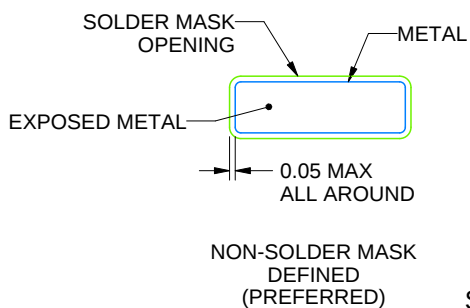
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

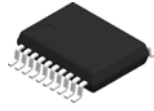


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

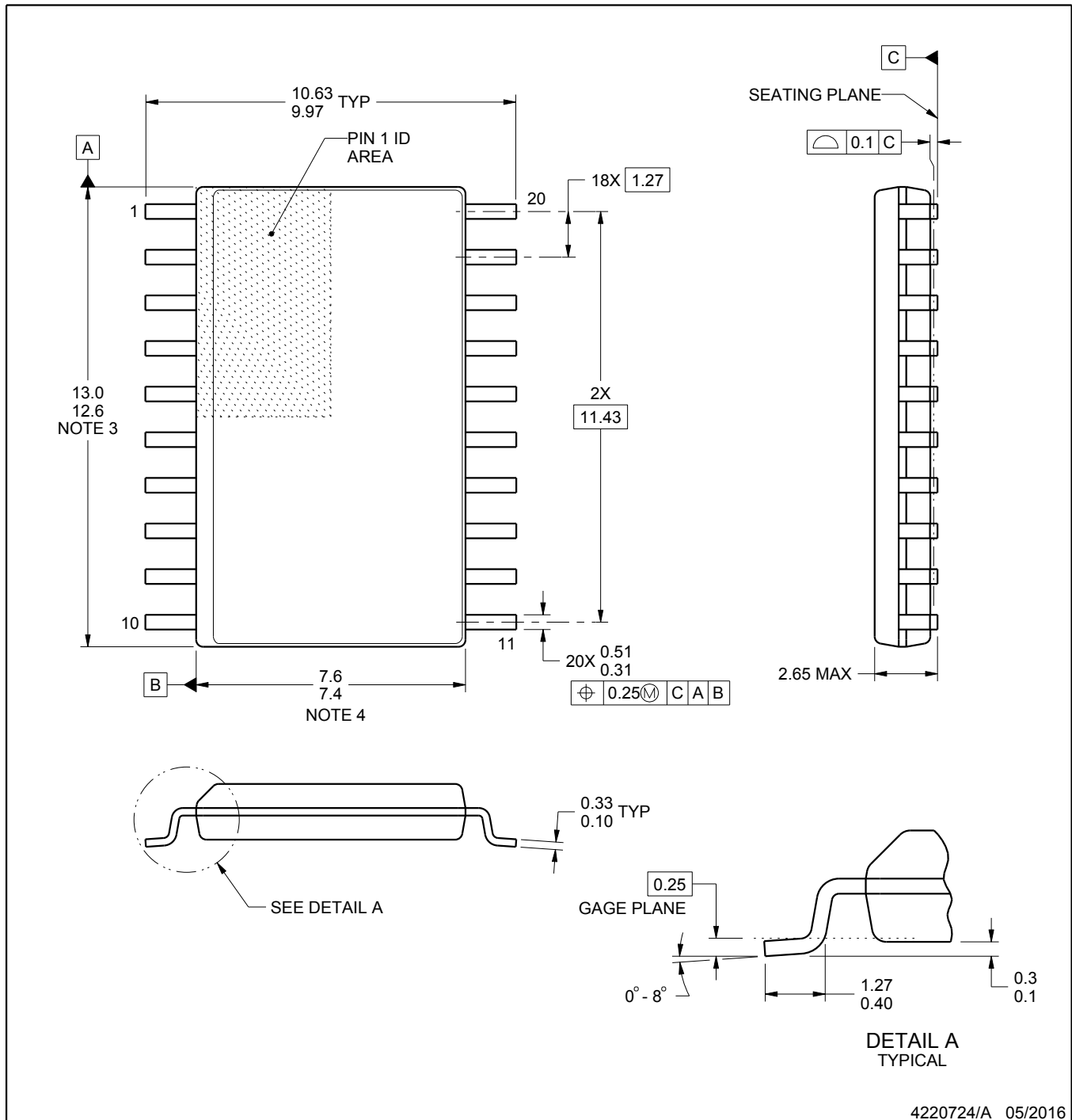
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

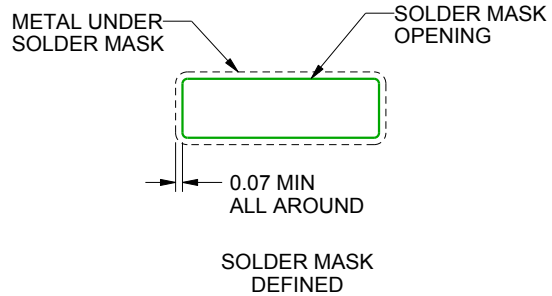
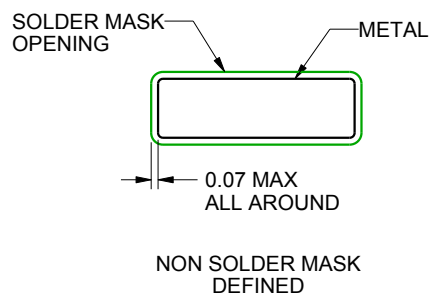
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated