# SNx4LV221A Dual Monostable Multivibrators with Schmitt-trigger Inputs

## 1 Features

- 2V to 5.5V $V_{CC}$ operation
- Max $t_{pd}$ of 11ns at 5V
- Support mixed-mode voltage operation on all ports Schmitt-trigger circuitry on $\overline{A}$, B, and $\overline{CLR}$ inputs for slow input transition rates
- Overriding clear terminates output pulse
- Glitch-free power-up reset on outputs
- $I_{off}$ supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, class II

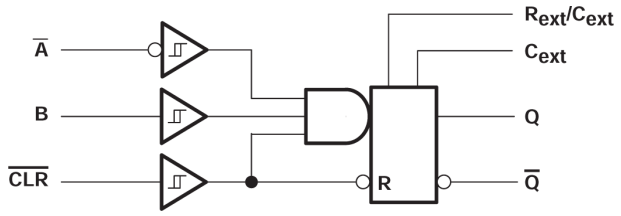
## 2 Description

The ’LV221A devices are dual multivibrators designed for 2V to 5.5V $V_{CC}$ operation. Each multivibrator has a negative-transition-triggered ($\overline{A}$) input and a positive-transition-triggered (B) input, either of which can be used as an inhibit input.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74LV221A | DB (SSOP, 16) | 6.2mm × 7.8mm | 6.2mm × 5.3mm |
| | DGV (TVSOP, 16) | 3.6mm × 6.4mm | 3.6mm × 4.4mm |
| | PW (TSSOP, 16) | 5.00mm × 6.4mm | 5.00mm × 4.40mm |
| | NS (SOP, 16) | 10.2mm × 7.8mm | 10.3mm × 5.30mm |
| | D (SOIC, 16) | 9.9mm × 6mm | 9.9mm × 3.90mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram, Each Multivibrator (Positive Logic)**

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# 3 Pin Configuration and Functions

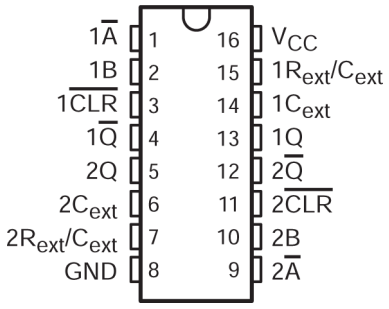



**Figure 3-1. SN74LV221A D, DB, DGV, NS, or PW Package; 16-Pin SOIC, SSOP, TVSOP, SOP, or TSSOP (Top View)**

**Table 3-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1 $\overline{A}$ | I | Channel 1 falling edge trigger input when 1B = H; Hold low for other input methods |
| 2 | 1B | I | Channel 1 rising edge trigger input when 1 $\overline{A}$ = L; Hold high for other input methods |
| 3 | 1 $\overline{CLR}$ | I | Channel 1 rising edge trigger when 1 $\overline{A}$ = L and 1B = H; Hold high for other input methods; Can cut pulse length short by driving low during output |
| 4 | 1 $\overline{Q}$ | O | Channel 1 inverted output |
| 5 | 2Q | O | Channel 2 output |
| 6 | 2$C_{ext}$ | — | Channel 2 external capacitor negative connection |
| 7 | 2$R_{ext}/C_{ext}$ | — | Channel 2 external capacitor and resistor junction connection |
| 8 | GND | — | Ground |
| 9 | 2 $\overline{A}$ | I | Channel 2 falling edge trigger input when 2B = H; Hold low for other input methods |
| 10 | 2B | I | Channel 2 rising edge trigger input when 2 $\overline{A}$ = L; Hold high for other input methods |
| 11 | 2 $\overline{CLR}$ | I | Channel 2 rising edge trigger when 2 $\overline{A}$ = L and 2B = H; Hold high for other input methods; Can cut pulse length short by driving low during output |
| 12 | 2 $\overline{Q}$ | O | Channel 2 inverted output |
| 13 | 1Q | O | Channel 1 output |
| 14 | 1$C_{ext}$ | — | Channel 1 external capacitor negative connection |
| 15 | 1$R_{ext}/C_{ext}$ | — | Channel 1 external capacitor and resistor junction connection |
| 16 | $V_{CC}$ | — | Power supply |

(1) I = inputs O = outputs

# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | −0.5 | 7 | V |
| $V_I$ (2) | Input voltage range | | −0.5 | 7 | V |
| $V_O$ (2) | Output voltage range in high or low state | | −0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ (2) | Output voltage range in power-off state | | −0.5 | 7 | V |
| $I_{IK}$ | Input clamp current | ($V_I$ < 0) | | −20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0) | | −50 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | −65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

## 4.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)(1)

| | | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | −2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | −6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | −12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |

over operating free-air temperature (unless otherwise noted)(1)

| | | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $R_{ext}$ | External timing resistance | $V_{CC}$ = 2 V | 5k | | Ω |
| | | $V_{CC}$ ≥ 3 V | 1k | | |
| $C_{ext}$ | External timing capacitance | | No restriction | | pF |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 1 | | ms/V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV221A | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | NS (SOP) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73 | 82 | 120 | 64 | 108 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | SN74LV221A | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{OH}$ | | $I_{OH}$ = −50 µA | 2 V to 5.5 V | $V_{CC}$−0.1 | | | V |
| | | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | |
| | | $I_{OH}$ = −6 mA | 3 V | 2.48 | | | |
| | | $I_{OH}$ = −12 mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | |
| $I_I$ | $R_{ext}/C_{ext}$ (1) | $V_I$ = 5.5 V or GND | 2 V to 5.5 V | | | ±2.5 | µA |
| | $\overline{A}$, B, and $\overline{CLR}$ | $V_I$ = 5.5 V or GND | 0 | | | ±1 | |
| | | | 0 to 5.5 V | | | ±1 | |
| $I_{CC}$ | Quiescent | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | µA |
| $I_{CC}$ | Active state (per circuit) | $V_I$ = $V_{CC}$ or GND, $R_{ext}$ /$C_{ext}$ = 0.5 $V_{CC}$ | 2.3 V | | | 220 | µA |
| | | | 3 V | | | 280 | |
| | | | 4.5 V | | | 650 | |
| | | | 5.5 V | | | 975 | |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.9 | | pF |
| | | | 5 V | | 1.9 | | |

(1) This test is performed with the terminal in the off-state condition.

## 4.6 Timing Requirements, $V_{CC}$ = 2.5V ± 0.2V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5V ± 0.2V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | $T_A$ = 25°C | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | 6 | | 6.5 | | ns |
| | | $\overline{A}$ or B trigger | 6 | | 6.5 | | |

## 4.7 Timing Requirements, $V_{CC}$ = 3.3V ± 0.3V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | $T_A$ = 25°C | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | 5 | | 5 | | ns |
| | | $\overline{A}$ or B trigger | 5 | | 5 | | |

## 4.8 Timing Requirements, $V_{CC}$ = 5V ± 0.5V

over recommended operating free-air temperature range, $V_{CC}$ = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | $T_A$ = 25°C | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ | 5 | | 5 | | ns |
| | | $\overline{A}$ or B trigger | 5 | | 5 | | |

## 4.9 Switching Characteristics, $V_{CC}$ = 2.5V ± 0.2V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5V ± 0.2V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 14.6[1] | 31.4[1] | 1 | 37 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 13.2[1] | 25[1] | 1 | 29.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 15.2[1] | 33.4[1] | 1 | 39 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 16.7 | 36 | 1 | 42 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 15 | 32.8 | 1 | 34.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 17.4 | 38 | 1 | 44 | |
| $t_w$ [2] | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 203 | 260 | | 320 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | 1.1 | ms |
| $\Delta t_w$ [3] | | | $C_L$ = 50 pF | | ±1 | | | | % |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) $t_w$ = Pulse duration at Q and $\overline{Q}$ outputs
(3) $\Delta_{tw}$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## 4.10 Switching Characteristics, $V_{CC}$ = 3.3V ± 0.3V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 10.2(1) | 20.6(1) | 1 | 24 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 9.3(1) | 15.8(1) | 1 | 18.5 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 10.6(1) | 22.4(1) | 1 | 26 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 11.8 | 24.1 | 1 | 27.5 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 10.6 | 19.3 | 1 | 22 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 12.3 | 25.9 | 1 | 29.5 | |
| $t_w$ (2) | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 186 | 240 | | 300 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | 1.1 | ms |
| $\Delta t_w$ (3) | | | $C_L$ = 50 pF | | ±1 | | | | % |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) $t_w$ = Pulse duration at Q and $\overline{Q}$ outputs
(3) $\Delta_{tw}$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## 4.11 Switching Characteristics, $V_{CC}$ = 5V ± 0.5V

over recommended operating free-air temperature range, $V_{CC}$ = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN74LV221A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.1(1) | 12(1) | 1 | 14 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 6.5(1) | 9.4(1) | 1 | 11 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 7.3(1) | 12.9(1) | 1 | 15 | |
| $t_{pd}$ | $\overline{A}$ or B | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 8.2 | 14 | 1 | 16 | ns |
| | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 7.4 | 11.4 | 1 | 13 | |
| | $\overline{CLR}$ trigger | Q or $\overline{Q}$ | | | 8.6 | 14.9 | 1 | 17 | |
| $t_w$ (2) | | Q or $\overline{Q}$ | $C_L$ = 50 pF, $C_{ext}$ = 28 pF, $R_{ext}$ = 2 kΩ | | 171 | 200 | | 240 | ns |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.01 µF, $R_{ext}$ = 10 kΩ | 90 | 100 | 110 | 90 | 110 | µs |
| | | | $C_L$ = 50 pF, $C_{ext}$ = 0.1 µF, $R_{ext}$ = 10 kΩ | 0.9 | 1 | 1.1 | 0.9 | 1.1 | ms |
| $\Delta t_w$ (3) | | | $C_L$ = 50 pF | | ±1 | | | | % |

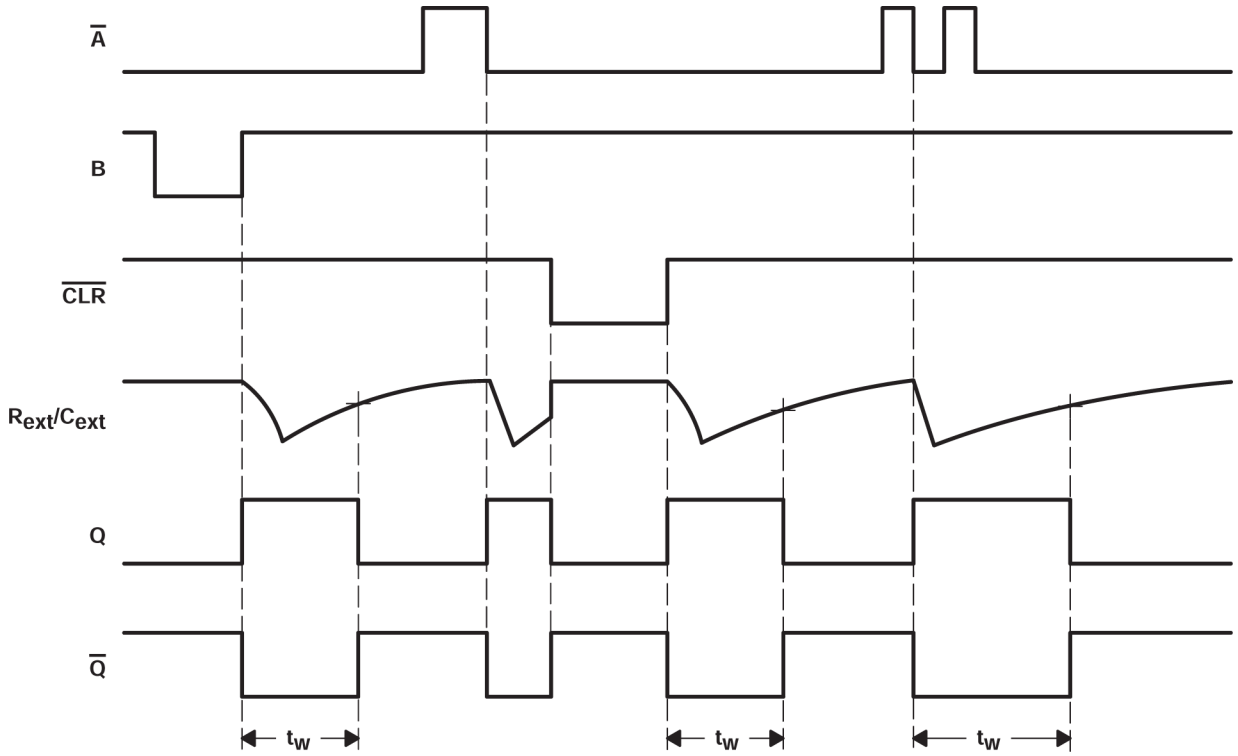
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) $t_w$ = Pulse duration at Q and $\overline{Q}$ outputs
(3) $\Delta_{tw}$ = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

## 4.12 Operating Characteristics

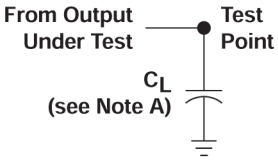
$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 10 MHz | 3.3 V | 50 | pF |
| | | | 5 V | 51 | |

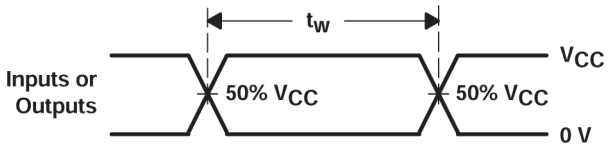
## 4.13 Input/Output Timing Diagram



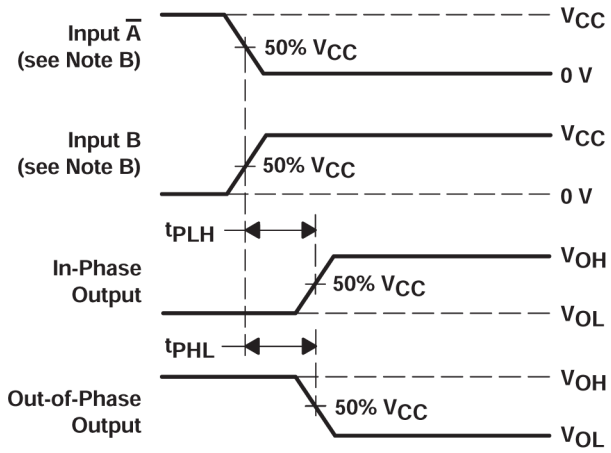
## 5 Parameter Measurement Information



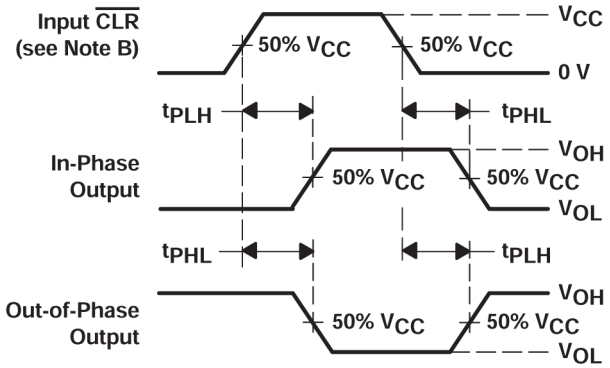

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
DELAY TIMES

A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ + 3 ns, $t_f$ + 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

**Figure 5-1. Load Circuit and Voltage Waveforms**

# 6 Detailed Description

## 6.1 Overview

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between $C_{ext}$ and $R_{ext}/C_{ext}$(positive) and an external resistor connected between $R_{ext}/C_{ext}$ and $V_{CC}$. To obtain variable pulse durations, connect an external variable resistor between $R_{ext}/C_{ext}$ and $V_{CC}$. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not related directly to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse duration can be varied by choosing the appropriate timing components. Output rise and fall times are TTL compatible and independent of pulse duration. Typical triggering and clearing sequences are illustrated in the input/output timing diagram.

The variance in output pulse duration from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the ’LV221A is shown in Figure 7-7. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 7-4.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Pin assignments are identical to those of the ’AHC123A and ’AHCT123A devices, so the ’LV221A can be substituted for those devices not using the retrigger feature.

For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

## 6.2 Functional Block Diagram

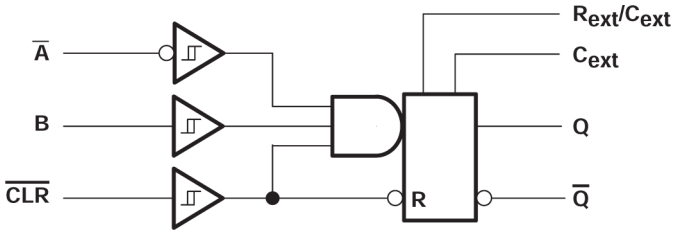



**Figure 6-1. Logic Diagram, Each Multivibrator (Positive Logic)**

## 6.3 Device Functional Modes

**Table 6-1. Function Table (Each Multivibrator)**

| INPUTS | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{A}$ | B | Q | $\overline{Q}$ | |
| L | X | X | L | H | Reset |
| H | H | X | L | H | Inhibit |
| H | X | L | L | H | Inhibit |
| H | L | ↑ | ⎍ | ⎍ | Outputs enabled |

**Table 6-1. Function Table (Each Multivibrator) (continued)**

| INPUTS | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{A}$ | B | Q | $\overline{Q}$ | |
| H | ↓ | H | ⎍ | ⎏ | Outputs enabled |
| ↑(1) | L | H | ⎍ | ⎏ | Outputs enabled |

(1) This condition is true only if the output of the latch formed by the NAND gate has been conditioned to the logic 1 state prior to $\overline{CLR}$ going high. This latch is conditioned by taking either $\overline{A}$ high or B low while $\overline{CLR}$ is inactive (high).

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

### *7.1.1 Caution in Use*

To prevent malfunctions due to noise, connect a high-frequency capacitor between $V_{CC}$ and GND, and keep the wiring between the external components and $C_{ext}$ and $R_{ext}/C_{ext}$ terminals as short as possible.

### *7.1.2 Power-down Considerations*

Large values of $C_{ext}$ can cause problems when powering down the 'LV221A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from $V_{CC}$ through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the $V_{CC}$ power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if $V_{CC}$ = 5 V and $C_{ext}$ = 15 pF, the $V_{CC}$ supply must turn off no faster than t = (5 V) × (15 pF)/30 mA = 2.5 ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of $V_{CC}$ to zero occurs, the 'LV221A can sustain damage. To avoid this possibility, use external clamping diodes.

### *7.1.3 Output Pulse Duration*

The output pulse duration, $t_w$, is determined primarily by the values of the external capacitance ($C_T$) and timing resistance ($R_T$). The timing components are connected as shown in Figure 7-1.

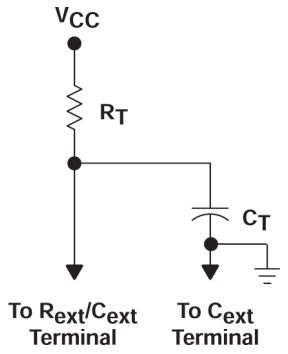



**Figure 7-1. Timing-Component Connections**

The pulse duration is given by:

$t_w + K \times R_T \times C_T$ (1)

if $C_T$ is ≥ 1000 pF, K = 1.0

or

if $C_T$ is < 1000 pF, K can be determined from Figure 7-6

where:

$t_w$ = pulse duration in ns

$R_T$ = external timing resistance in kΩ

$C_T$ = external capacitance in pF

K = multiplier factor

Equation 1 and Figure 7-2 or Figure 7-3 can be used to determine values for pulse duration, external resistance, and external capacitance.

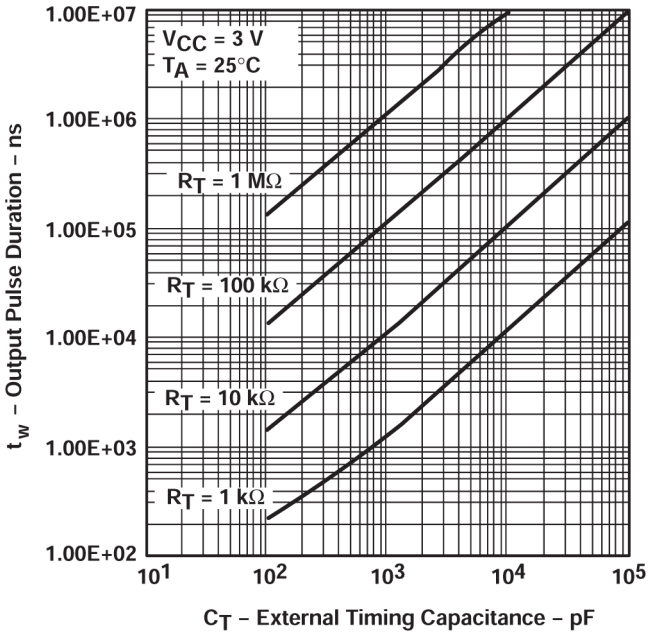



**Figure 7-2. Output Pulse Duration vs External Timing Capacitance**

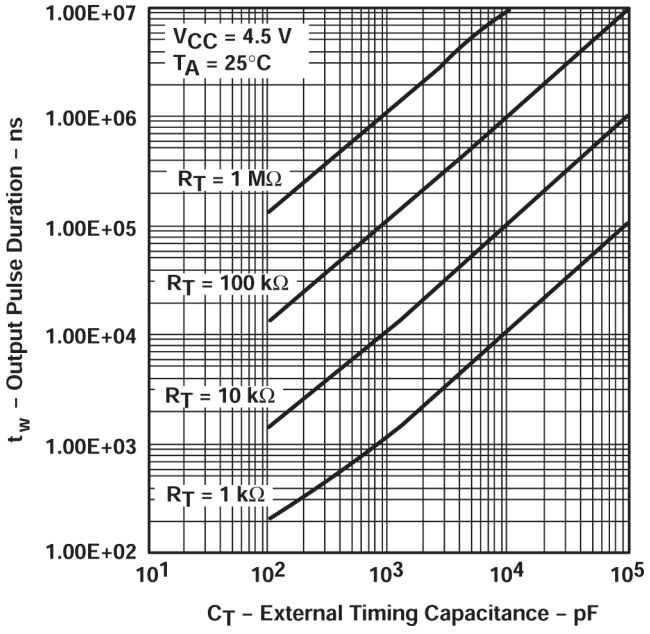



**Figure 7-3. Output Pulse Duration vs External Timing Capacitance**

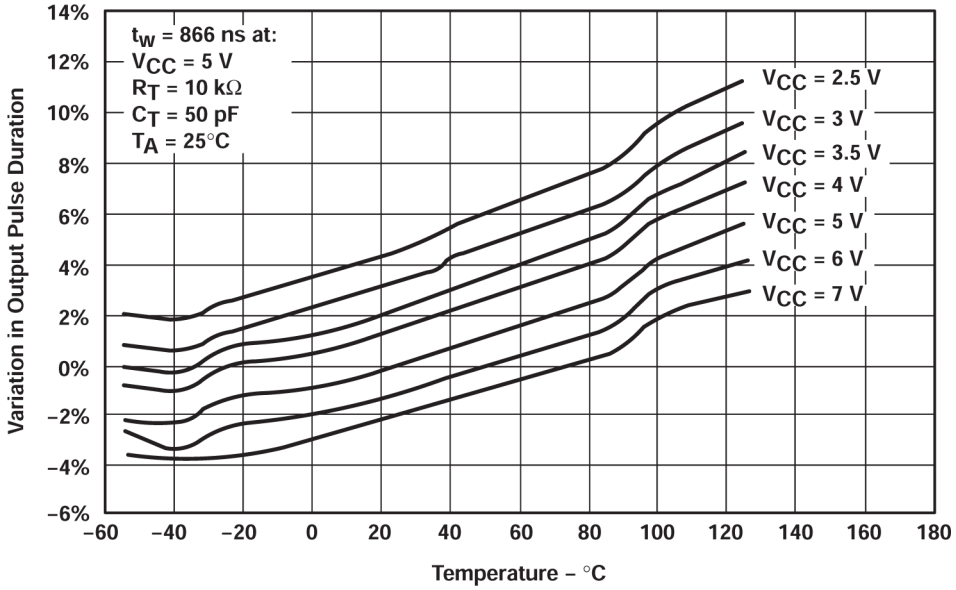



**Figure 7-4. Variation in Output Pulse Duration vs Temperature**

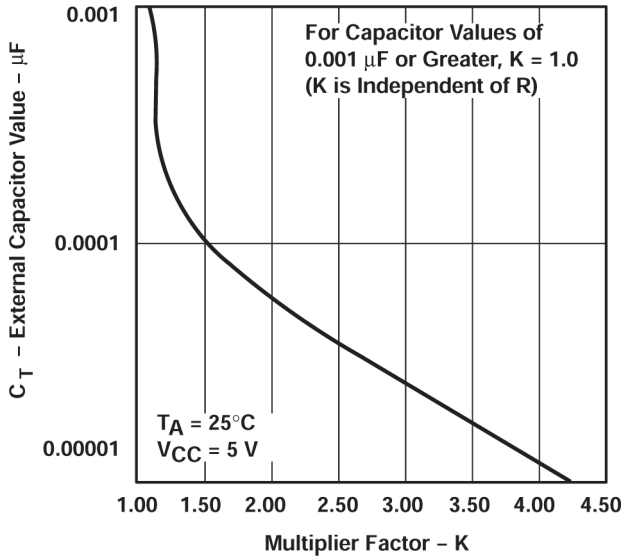



**Figure 7-5. External Capacitance vs Multiplier Factor**

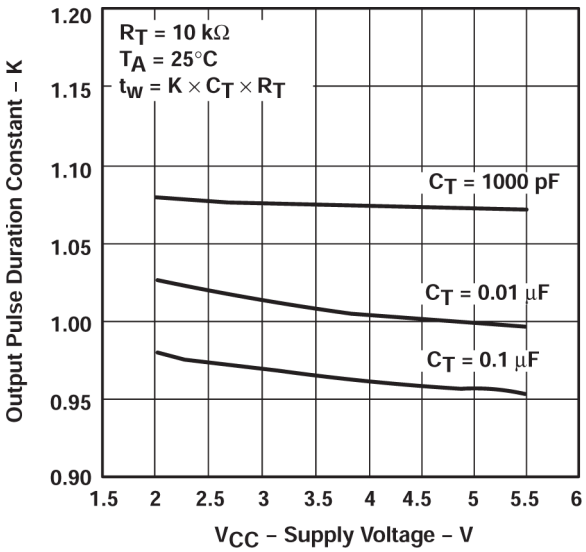



**Figure 7-6. Output Pulse Duration Constant vs Supply Voltage**

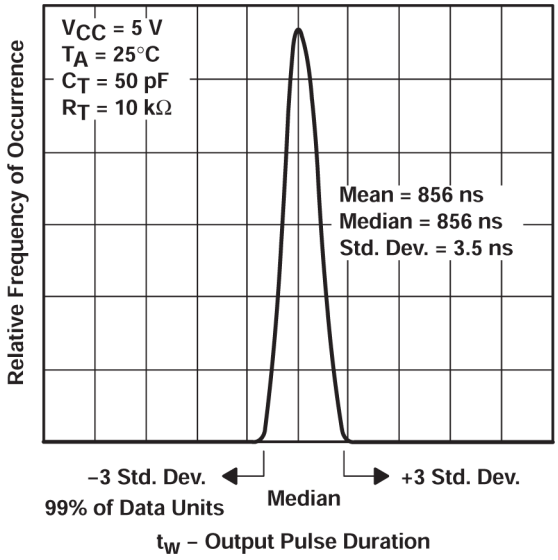



**Figure 7-7. Distribution of Units vs Output Pulse Duration**

## 7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.3 Layout

### *7.3.1 Layout Guidelines*

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible

- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

### *7.3.2 Layout Example*

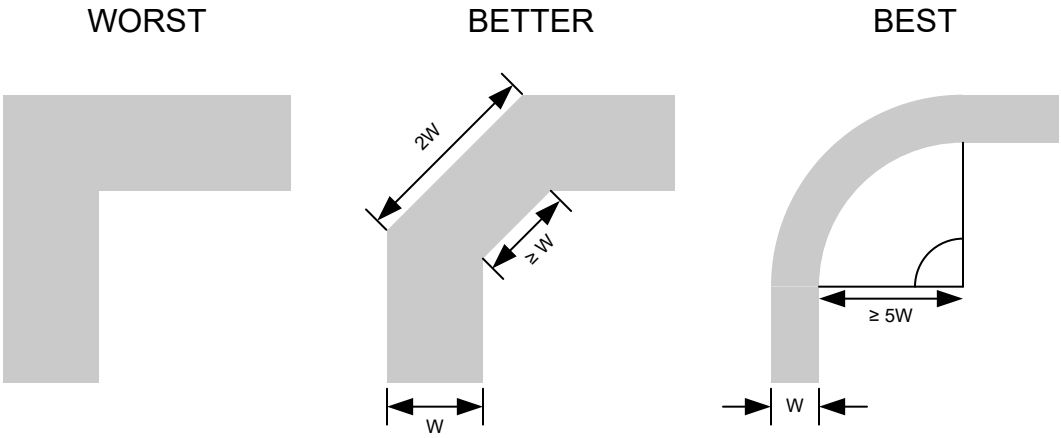



**Figure 7-8. Example Trace Corners for Improved Signal Integrity**

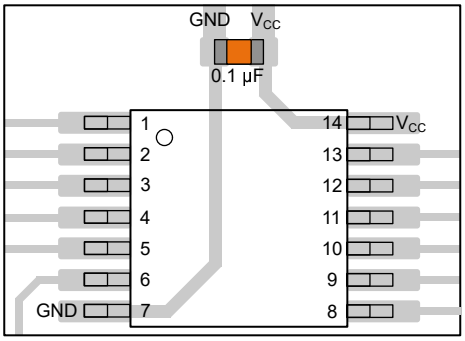



**Figure 7-9. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

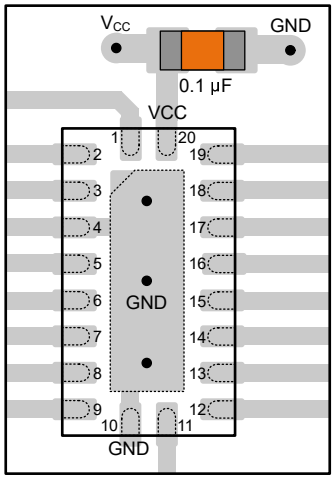



**Figure 7-10. Example Bypass Capacitor Placement for WQFN and Similar Packages**

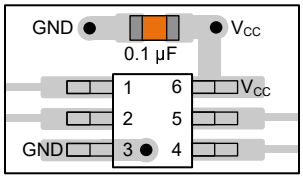



**Figure 7-11. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

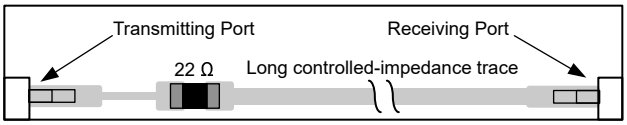



**Figure 7-12. Example Damping Resistor Placement for Improved Signal Integrity**

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Documentation Support

### *8.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (April 2005) to Revision H (January 2025) | Page |
|---|---|
| • Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,* Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Deleted references to SN54LV221A product preview and machine model throughout the data sheet | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV221AD | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | LV221A |
| SN74LV221ADGVR | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV221A |
| SN74LV221ADGVR.A | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV221A |
| SN74LV221ADR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV221A |
| SN74LV221ADR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV221A |
| SN74LV221ANSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV221A |
| SN74LV221ANSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV221A |
| SN74LV221APW | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 85 | LV221A |
| SN74LV221APWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV221A |
| SN74LV221APWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV221A |
| SN74LV221APWT | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 85 | LV221A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN74LV221A :**

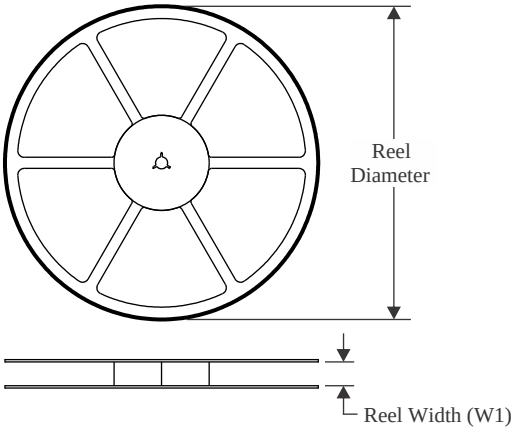
- Automotive : SN74LV221A-Q1

NOTE: Qualified Version Definitions:

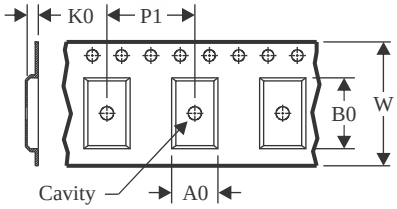
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

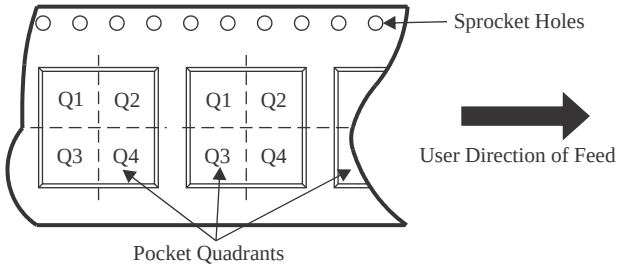



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

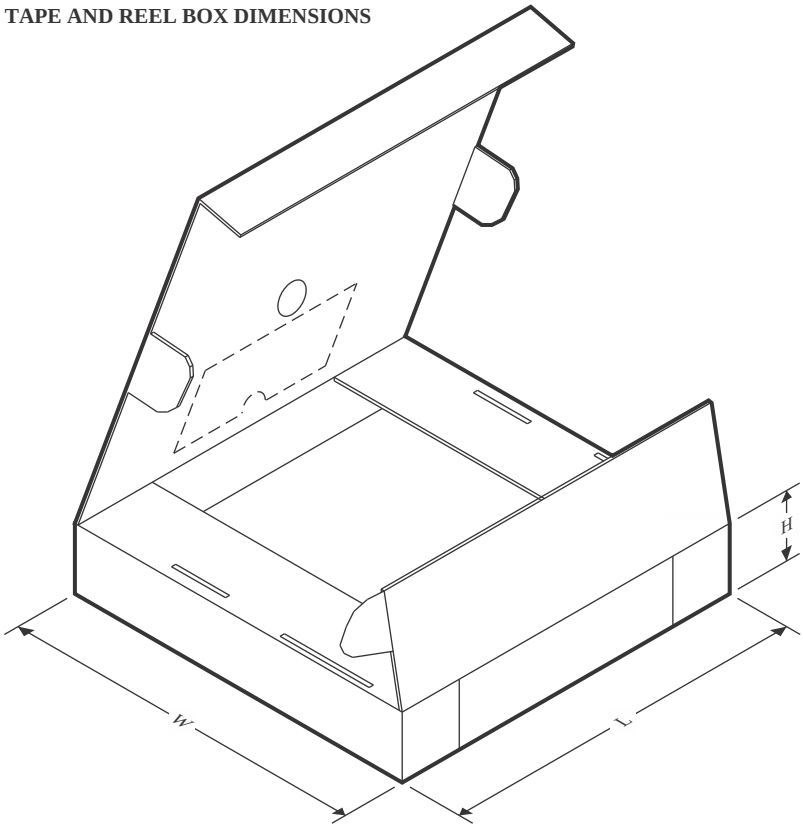
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV221ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV221ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV221ANSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV221APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

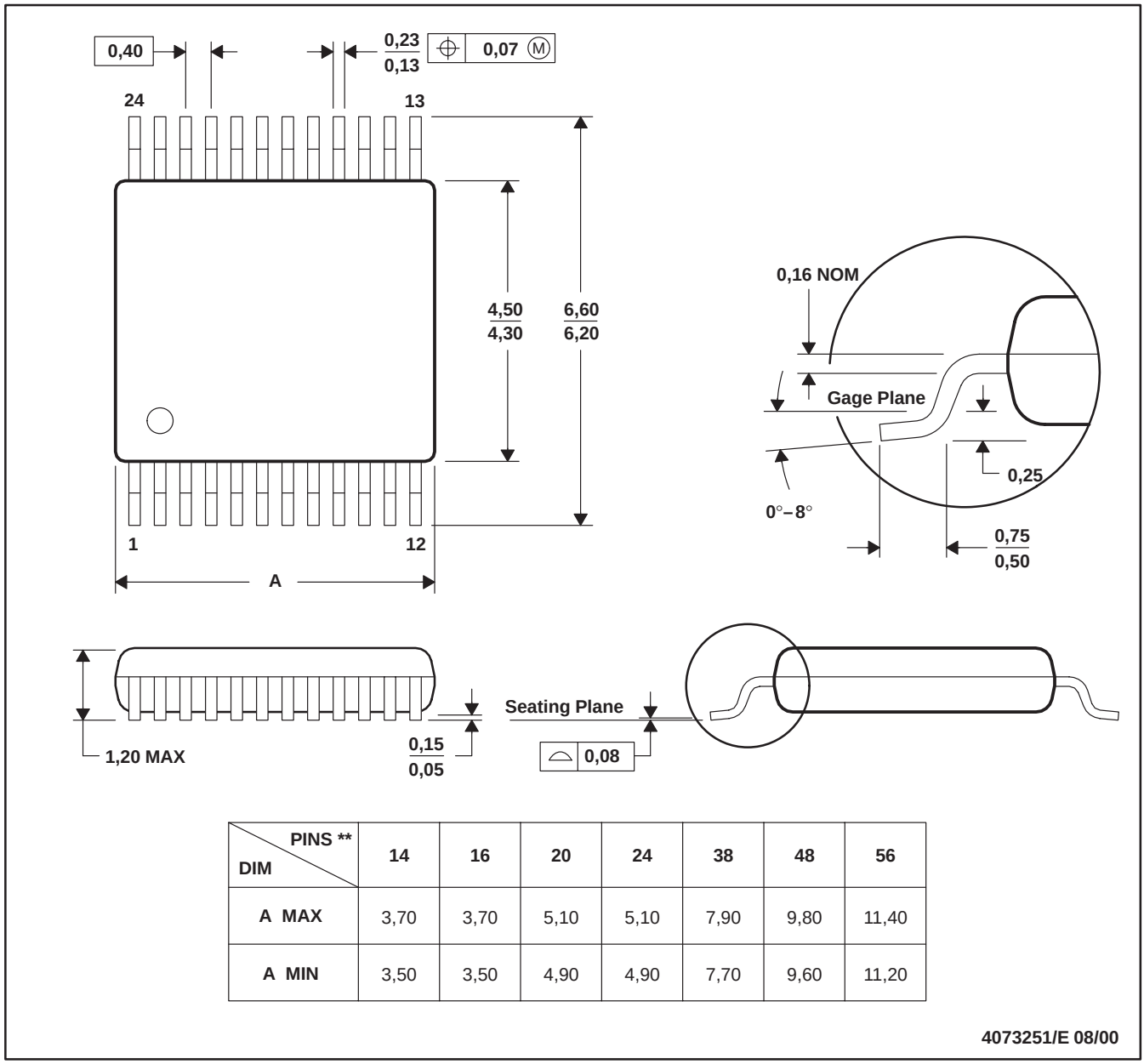



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV221ADGVR | TVSOP | DGV | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV221ADR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LV221ANSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV221APWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

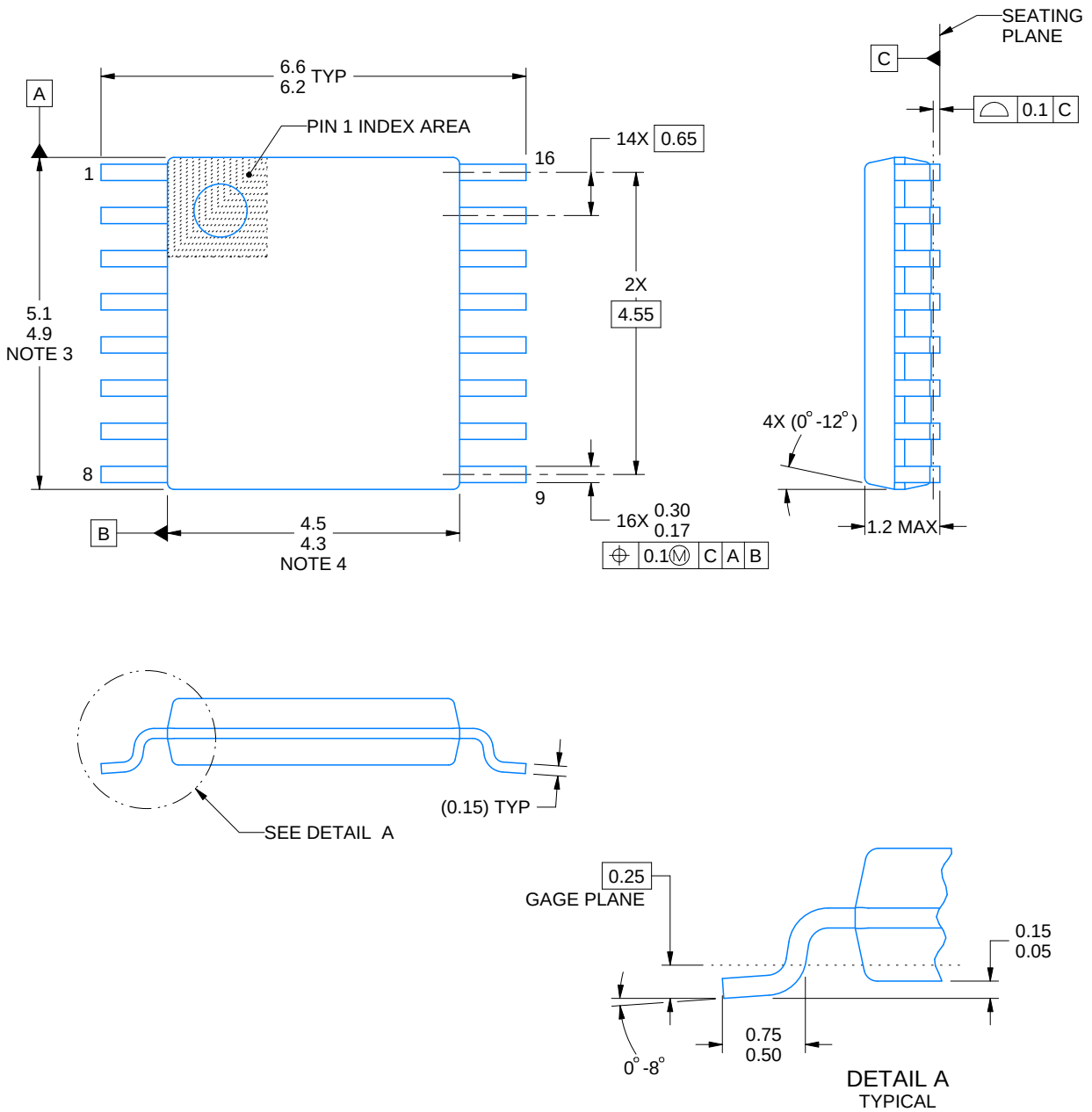
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# PACKAGE OUTLINE

## PW0016A

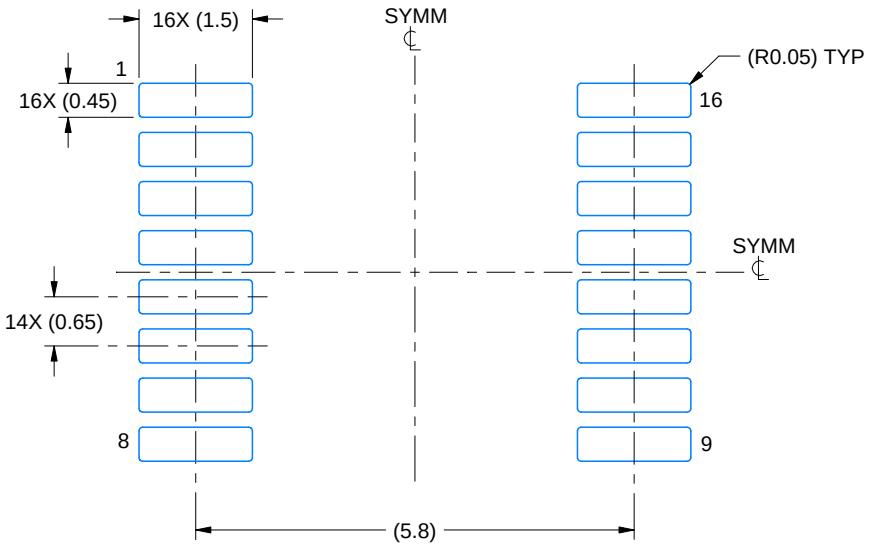
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



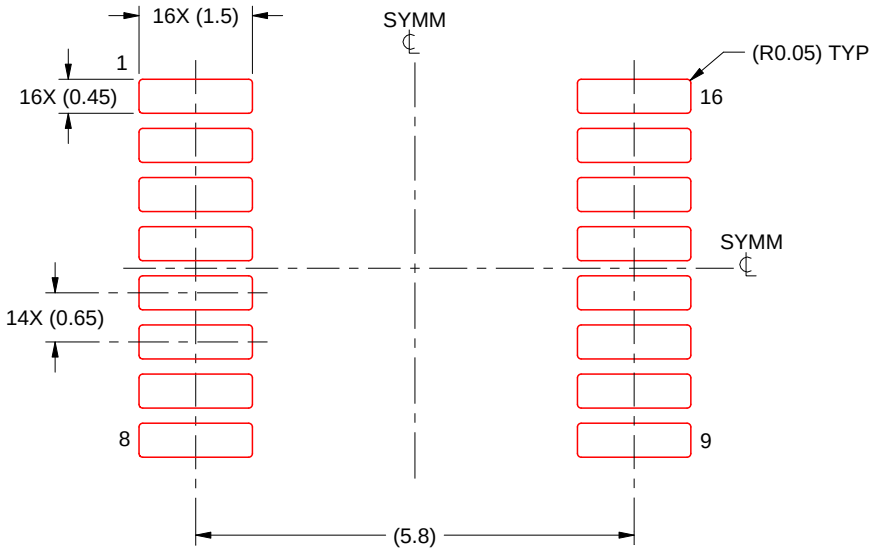

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

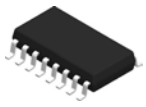



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

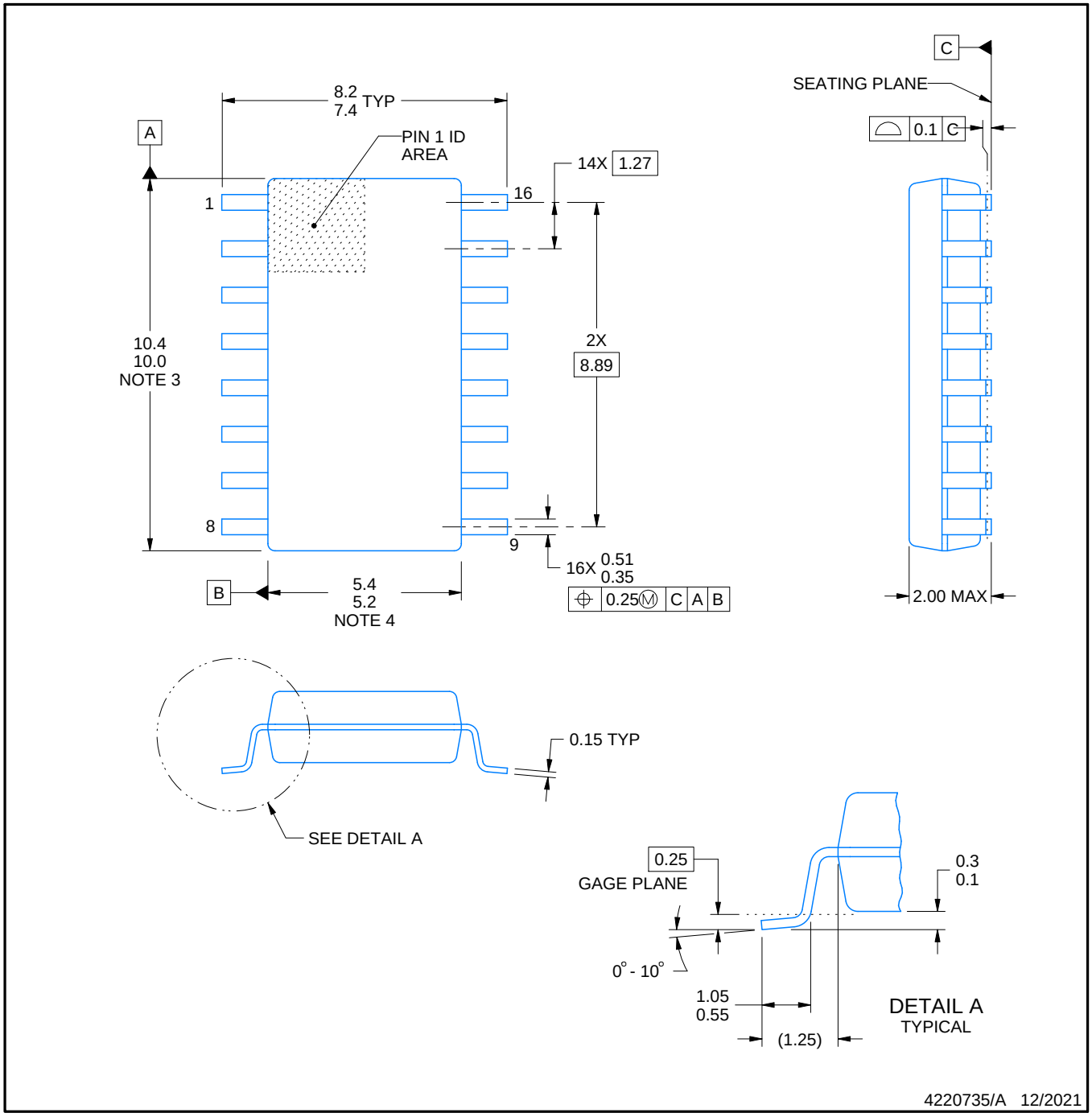


# PACKAGE OUTLINE

## NS0016A

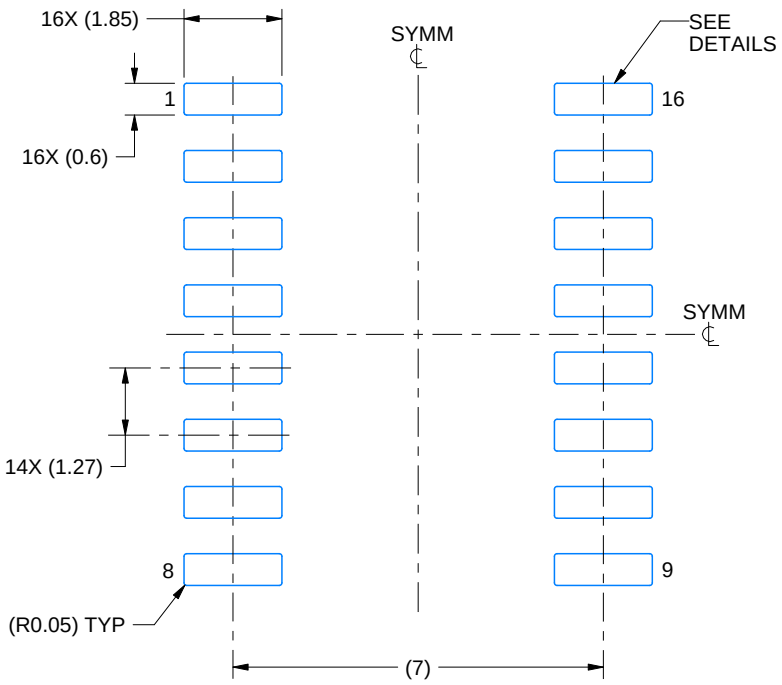
## SOP - 2.00 mm max height

SOP

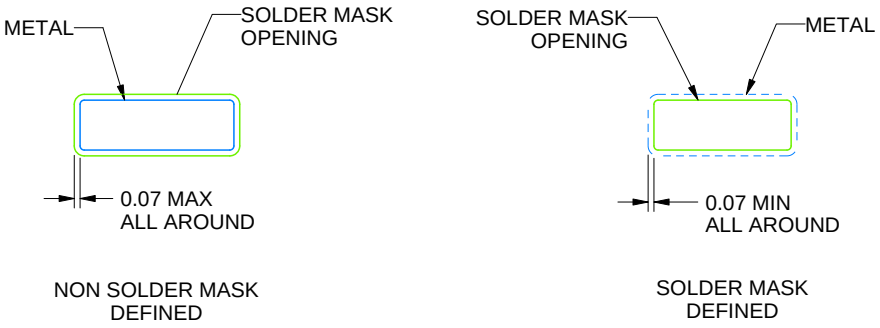



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

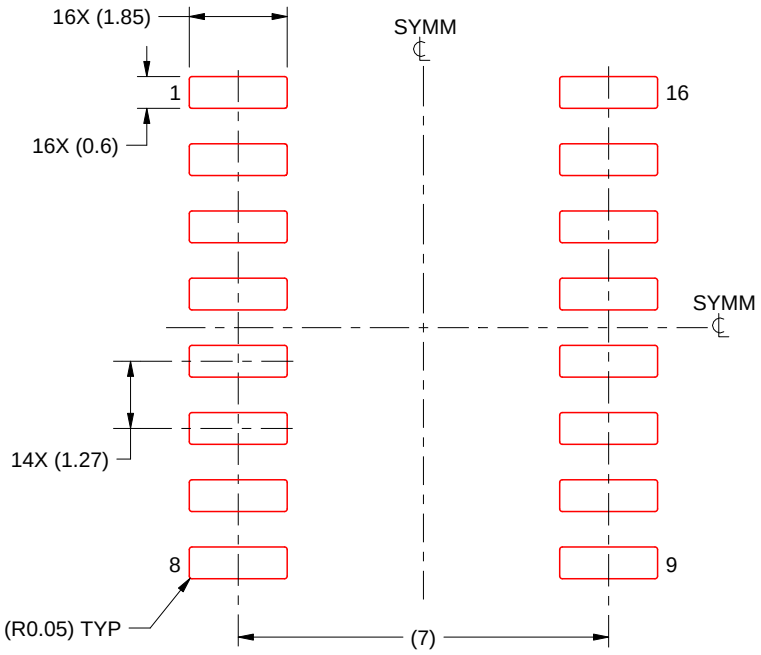
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



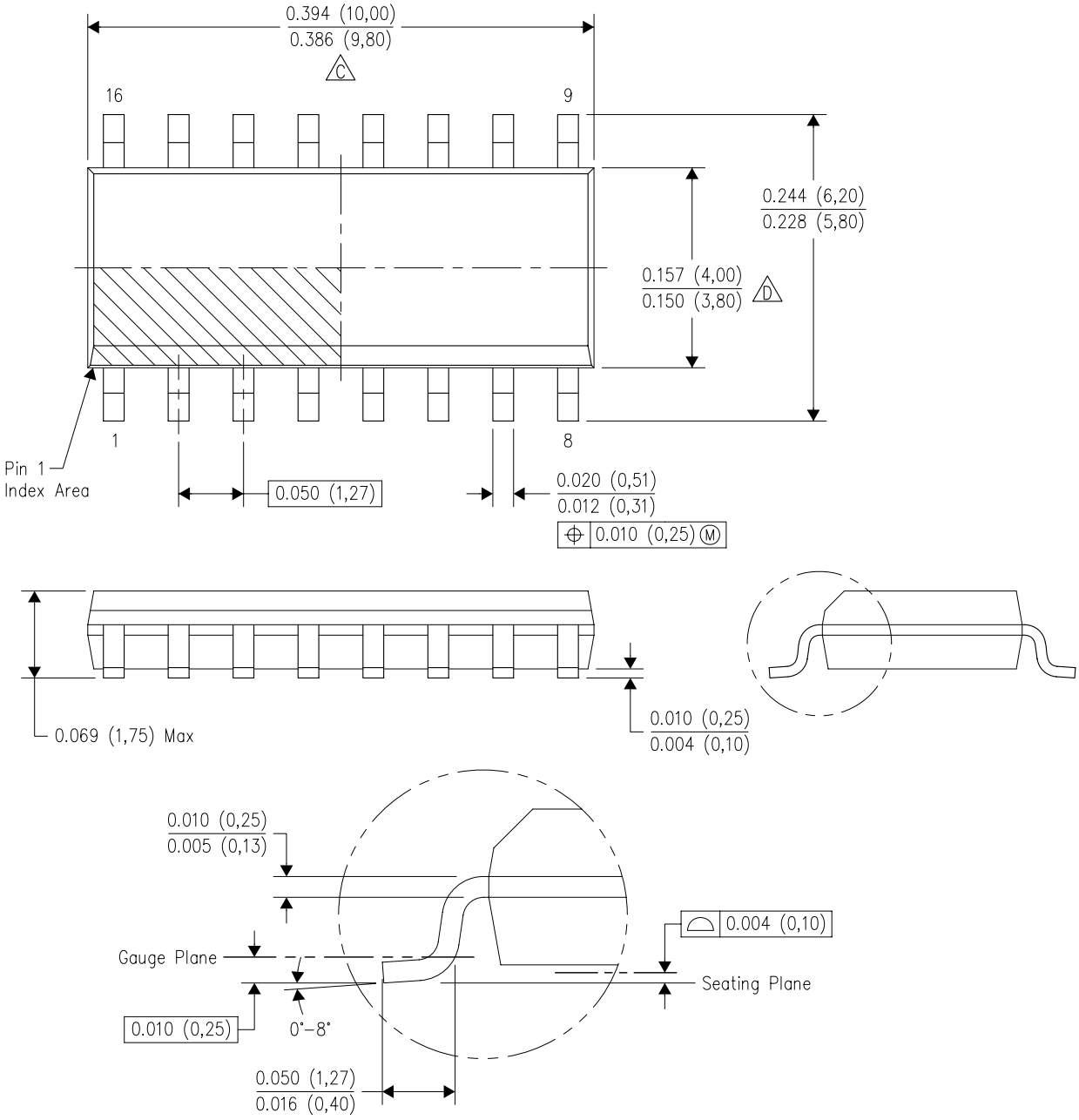

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

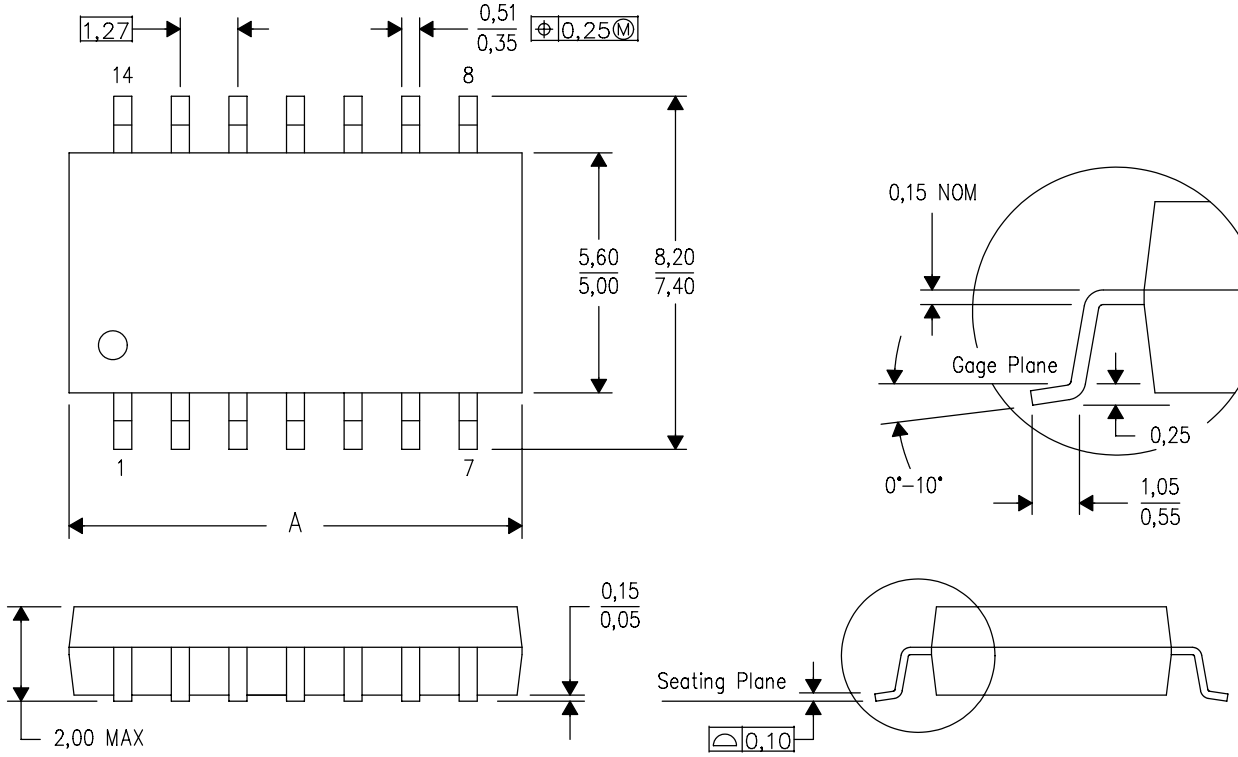



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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