

SN74LV14A Hex Schmitt-Trigger Inverters

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Max t_{pd} of 10 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Network Switches
- Wearable Health and Fitness Devices
- PDAs
- LCD TVs
- Power Infrastructure

3 Description

These hex Schmitt-trigger inverters are designed for 2 V to 5.5 V V_{CC} operation.

The SN74LV14A devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74LV14A	TVSOP (14)	3.60 mm × 4.40 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Figure 3-1. Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1 Features	1	8.1 Overview.....	9
2 Applications	1	8.2 Functional Block Diagram.....	9
3 Description	1	8.3 Feature Description.....	9
4 Revision History	2	8.4 Device Functional Modes.....	9
5 Pin Configuration and Functions	3	9 Application and Implementation	10
Pin Functions.....	3	9.1 Application Information.....	10
6 Specifications	4	9.2 Typical Application.....	10
6.1 Absolute Maximum Ratings.....	4	10 Power Supply Recommendations	12
6.2 ESD Ratings.....	4	11 Layout	12
6.3 Recommended Operating Conditions.....	4	11.1 Layout Guidelines.....	12
6.4 Thermal Information.....	5	11.2 Layout Example.....	12
6.5 Electrical Characteristics.....	5	12 Device and Documentation Support	13
6.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	12.1 Related Links.....	13
6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	12.2 Receiving Notification of Documentation Updates.....	13
6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	12.3 Support Resources.....	13
6.9 Noise Characteristics.....	6	12.4 Trademarks.....	13
6.10 Operating Characteristics.....	6	12.5 Electrostatic Discharge Caution.....	13
6.11 Typical Characteristics.....	7	12.6 Glossary.....	13
7 Parameter Measurement Information	8	13 Mechanical, Packaging, and Orderable Information	13
8 Detailed Description	9		

4 Revision History

Changes from Revision K (September 2014) to Revision L (December 2022) Page

- Updated the format for tables, figures, and cross-references throughout the document..... **1**

Changes from Revision J (September 1997) to Revision K (September 2014) Page

- Updated document to new TI data sheet format..... **1**
- Removed Ordering Information table..... **1**
- Added Applications..... **1**
- Added Device Information table..... **1**
- Added Pin Functions table..... **3**
- Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. **4**
- Added Thermal Information table..... **5**
- Added Typical Characteristics..... **7**
- Added Application and Implementation section..... **10**
- Added Power Supply Recommendations and Layout sections..... **12**

5 Pin Configuration and Functions

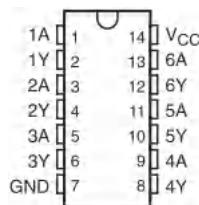


Figure 5-1. SN74LV14A D, DB, DGV, NS OR PW Package Top View

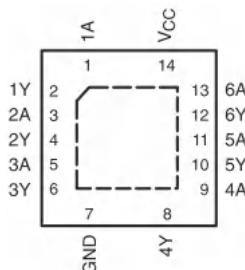


Figure 5-2. SN74LV14A RGY Package Top View

Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION		
	SN74LV14A					
	D, DB, DGV, NS, PW	RGY				
1A	1	1	I	Input 1A		
1Y	2	2	O	Output 1Y		
2A	3	3	I	Input 2A		
2Y	4	4	O	Output 2Y		
3A	5	5	I	Input 3A		
3Y	6	6	O	Output 3Y		
4Y	8	8	O	Output 4Y		
4A	9	9	I	Input 4A		
5Y	10	10	O	Output 5Y		
5A	11	11	I	Input 5A		
6Y	12	12	O	Output 6Y		
6A	13	13	I	Input 6A		
GND	7	7	—	Ground Pin		
NC	—	—	—	No Connection		
V _{CC}	14	14	—	Power Pin		

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range ⁽²⁾		-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	7	V
V_O	Output voltage range ^{(2) (3)}		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-20	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under [Section 6.1](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

$V_{(ESD)}$	Electrostatic discharge		VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 1000	
		Machine Model	± 200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LV14A		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	2	5.5	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		μA
		$V_{CC} = 2.3$ V to 2.7 V		-50
		$V_{CC} = 3$ V to 3.6 V		-2
		$V_{CC} = 4.5$ V to 5.5 V		-6
I_{OL}	Low-level output current	$V_{CC} = 2$ V		μA
		$V_{CC} = 2.3$ V to 2.7 V		-12
		$V_{CC} = 3$ V to 3.6 V		50
		$V_{CC} = 4.5$ V to 5.5 V		2
T_A	Operating free-air temperature	$V_{CC} = 3$ V to 3.6 V		6
		$V_{CC} = 4.5$ V to 5.5 V		12
		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV14A						UNIT °C/W
		D	DB	DGV	NS	PW	RGY	
		14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	94.9	107.4	130.4	91.4	122.6	57.6	°C/W
R _θ JC(top)	Junction-to-case (top) thermal resistance	56.3	59.9	53.4	49.0	51.3	70.4	
R _{θJB}	Junction-to-board thermal resistance	49.2	54.7	63.5	50.2	64.4	33.6	
Ψ _{JT}	Junction-to-top characterization parameter	20.7	21.0	7.3	15.3	6.8	3.5	
Ψ _{JB}	Junction-to-board characterization parameter	48.9	51.2	62.8	49.8	63.8	33.7	
R _θ JC(bot)	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	14.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LV14A –40°C to 85°C			SN74LV14A –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{T+}	Positive-going threshold		2.5 V		1.75			1.75	V
			3.3 V		2.31			2.31	
			5 V		3.5			3.5	
V _{T–}	Negative-going threshold		2.5 V	0.75		0.75			V
			3.3 V	0.99		0.99			
			5 V	1.5		1.5			
ΔV _T (V _{T+} – V _{T–})	Hysteresis		2.5 V	0.25		0.25			V
			3.3 V	0.33		0.33			
			5 V	0.5		0.5			
V _{OH}	High-level output voltage	I _{OH} = –50 µA	2 V to 5.5 V	V _{CC} – 0.1		V _{CC} – 0.1			V
		I _{OH} = –2 mA	2.3 V	2		2			
		I _{OH} = –6 mA	3 V	2.48		2.48			
		I _{OH} = –12 mA	4.5 V	3.8		3.8			
V _{OL}	Low-level output voltage	I _{OL} = 50 µA	2 V to 5.5 V		0.1			0.1	V
		I _{OL} = 2 mA	2.3 V		0.4			0.4	
		I _{OL} = 6 mA	3 V		0.44			0.44	
		I _{OL} = 12 mA	4.5 V		0.55			0.55	
I _I	Input leakage current	V _I = V _{CC} or GND	0 to 5.5 V		±1			±1	µA
I _{CC}	Static supply current	V _I = V _{CC} or GND, I _O = 0	5.5 V		20			20	µA
I _{off}	Input/Output Power-Off Leakage Current	V _I or V _O = 0 to 5.5 V	0		5			5	µA
C _i	Input capacitance	V _I = V _{CC} or GND	3.3 V		2.3			2.3	pF
			5 V		2.3			2.3	

6.6 Switching Characteristics, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV14A -40°C to 85°C		SN74LV14A -40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15 \text{ pF}$	10.2 ⁽¹⁾	19.7 ⁽¹⁾	22	1	22	1	23	ns
			$C_L = 50 \text{ pF}$	13.3	24	27	1	27	1	28	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV14A -40°C to 85°C		SN74LV14A -40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15 \text{ pF}$	7.3 ⁽¹⁾	12.8 ⁽¹⁾	15	1	15	1	16	ns
			$C_L = 50 \text{ pF}$	9.6	16.3	18.5	1	18.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV14A -40°C to 85°C		SN74LV14A -40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15 \text{ pF}$	5.1 ⁽¹⁾	8.6 ⁽¹⁾	10	1	10	1	11	ns
			$C_L = 50 \text{ pF}$	6.7	10.6	12	1	12	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

$V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

				$SN74LV14A$			UNIT
				MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic				0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic				-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic				3.1		V
$V_{IH(D)}$	High-level dynamic input voltage			2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage					0.99	V

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

	PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}$ $f = 10 \text{ MHz}$	3.3 V	8.8	pF
			5 V	9.6	

6.11 Typical Characteristics

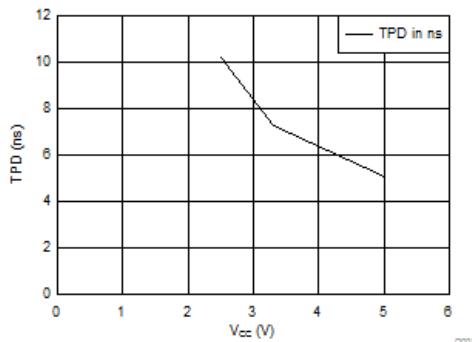


Figure 6-1. TPD vs V_{CC}

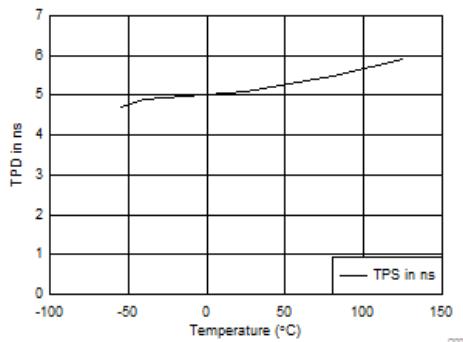
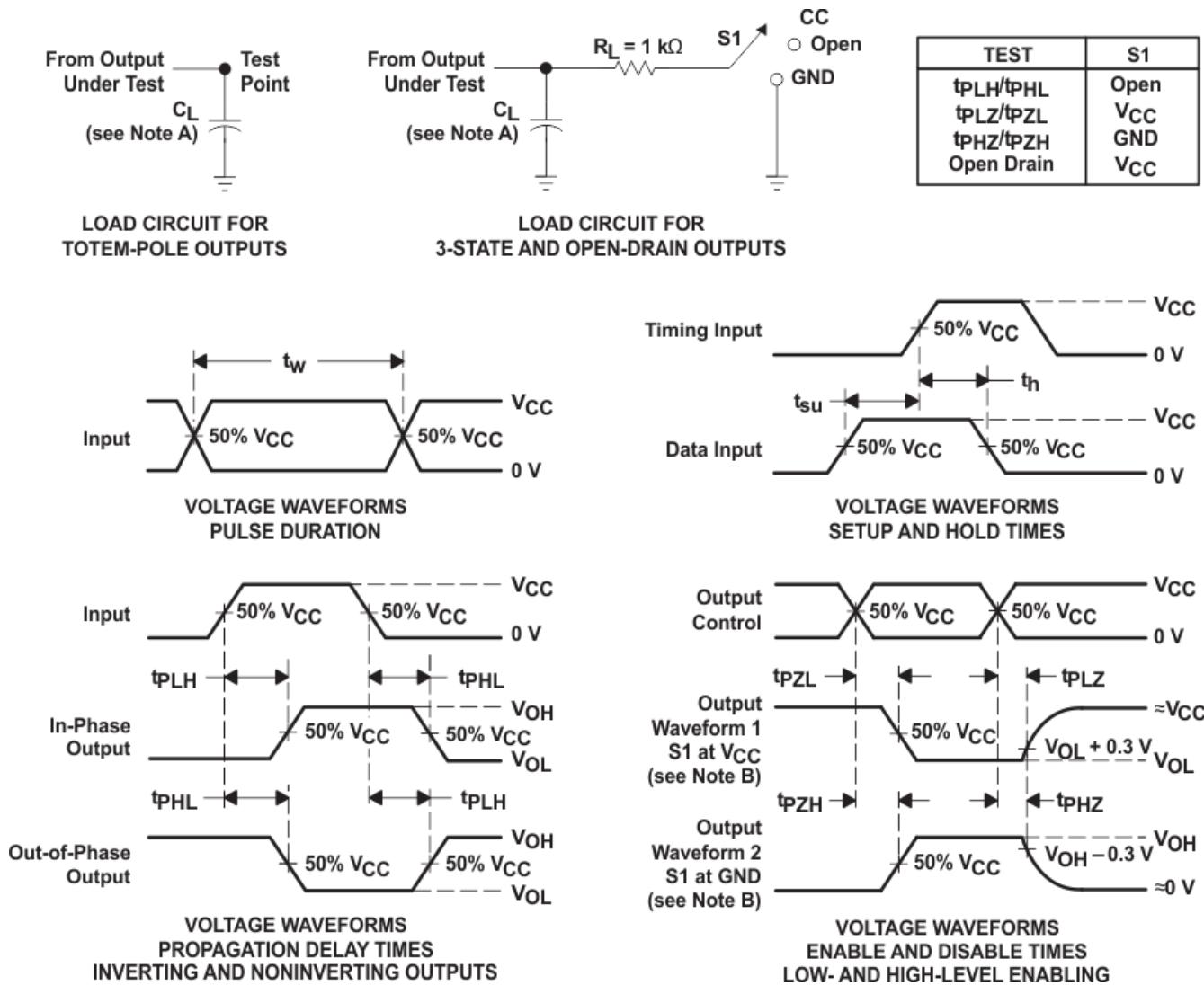


Figure 6-2. TPD vs Temperature

7 Parameter Measurement Information

7.1



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PZL} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These hex Schmitt-trigger inverters are designed for 2 V to 5.5 V V_{CC} operation.

The SN74LV14A devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

These devices are fully specified for partial-power-down application using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram



Figure 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.3 Feature Description

- Wide operating voltage range
 - Operates From 2 V to 5.5 V
- Allows up or down voltage translation
 - Inputs and outputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V
- Schmitt-trigger inputs allow for slow or noisy inputs

8.4 Device Functional Modes

**Table 8-1. Function Table
(Each Inverter)**

INPUT ⁽¹⁾ A	OUTPUT ⁽²⁾ Y
H	L
L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Schmitt triggers should be used anytime you need to translate a sine wave into a square wave as shown in Figure 9-1. They may also be used where a slow or noisy input needs to be sped up or cleaned up as shown in Figure 9-2.

9.2 Typical Application

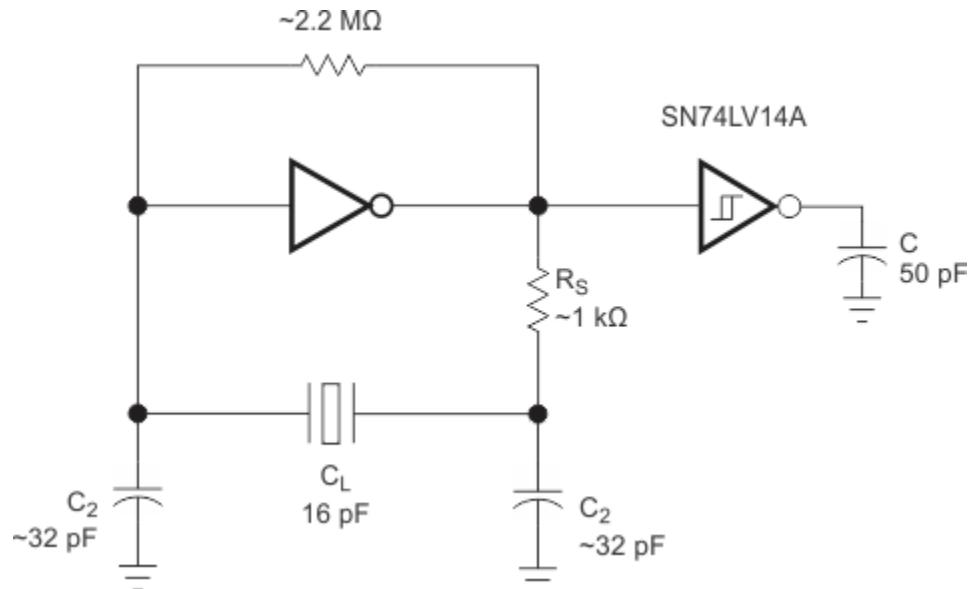


Figure 9-1. Oscillator Application Schematic

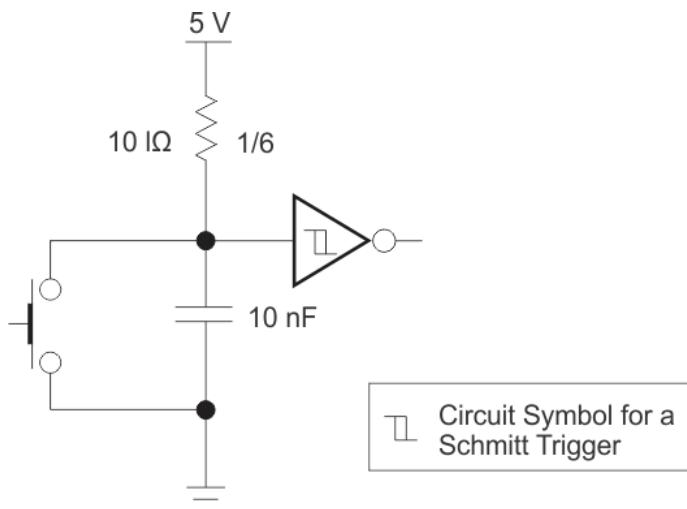


Figure 9-2. Switch De-bouncer Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:

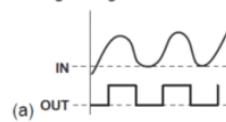
- For rise time and fall time specifications, see $\Delta t/\Delta V$ in [Section 6.3](#) table.
- For specified high and low levels, see V_{IH} and V_{IL} in [Section 6.3](#) table.
- Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .

2. Recommended Output Conditions:

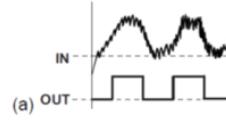
- Load currents should not exceed 35 mA per output and 50 mA total for the part.

9.2.3 Application Curves

Schmitt triggers should be used any time you need to
1. Change a sine wave into a square wave.



2. Have noisy signals that need to be cleaned up



3. Have slow edges that need to be converted to fast edges.



Figure 9-3. Schmitt Trigger Curves

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 6.3](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the [Figure 11-1](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

11.2 Layout Example

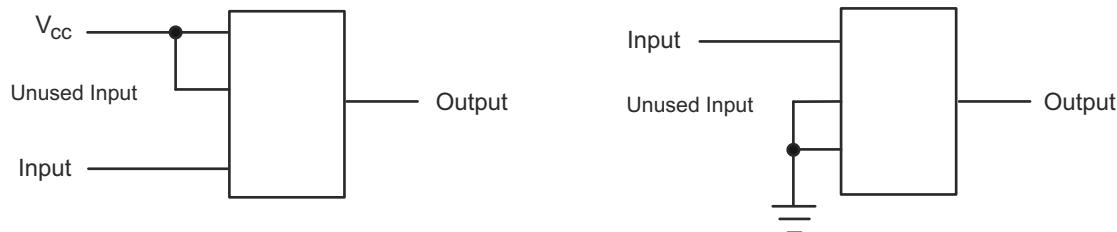


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV14A	Click here				
SN74LV14A	Click here				

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV14AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	LV14A
SN74LV14ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADGVR.A	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADRG4.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV14A
SN74LV14ANSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV14A
SN74LV14APW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	LV14A
SN74LV14APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG3	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG3.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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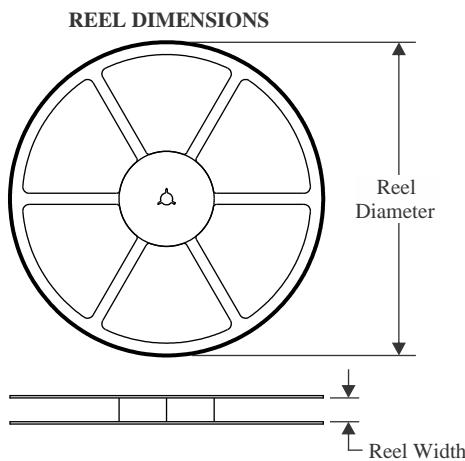
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV14A :

- Automotive : [SN74LV14A-Q1](#)
- Enhanced Product : [SN74LV14A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV14ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV14ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ANSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74LV14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV14ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV14ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV14ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV14ADR	SOIC	D	14	2500	340.5	336.1	32.0
SN74LV14ADRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV14ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74LV14ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV14APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV14APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV14APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV14ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

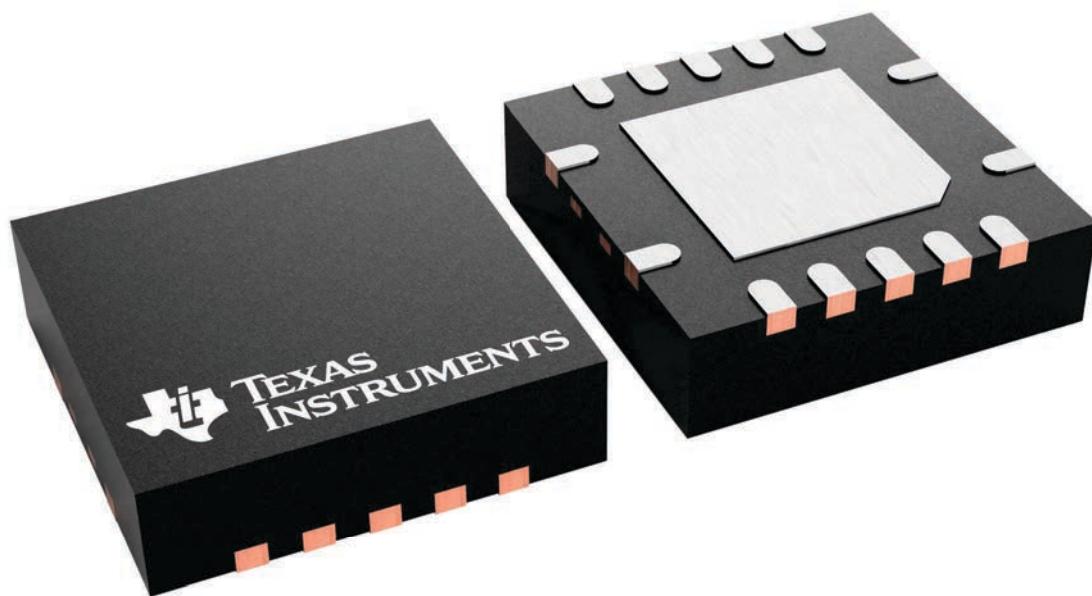
RGY 14

VQFN - 1 mm max height

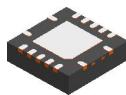
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



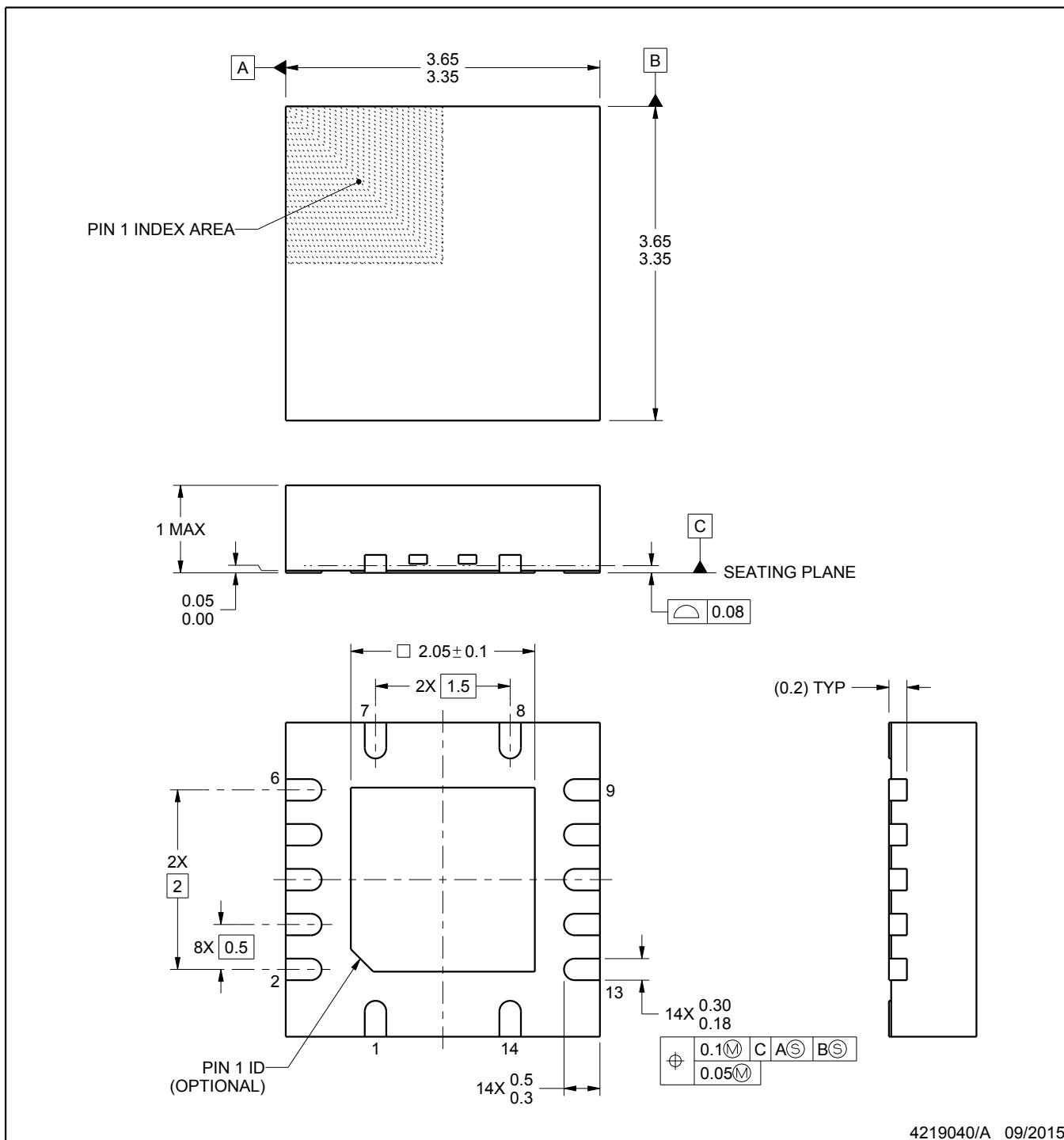
4231541/A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

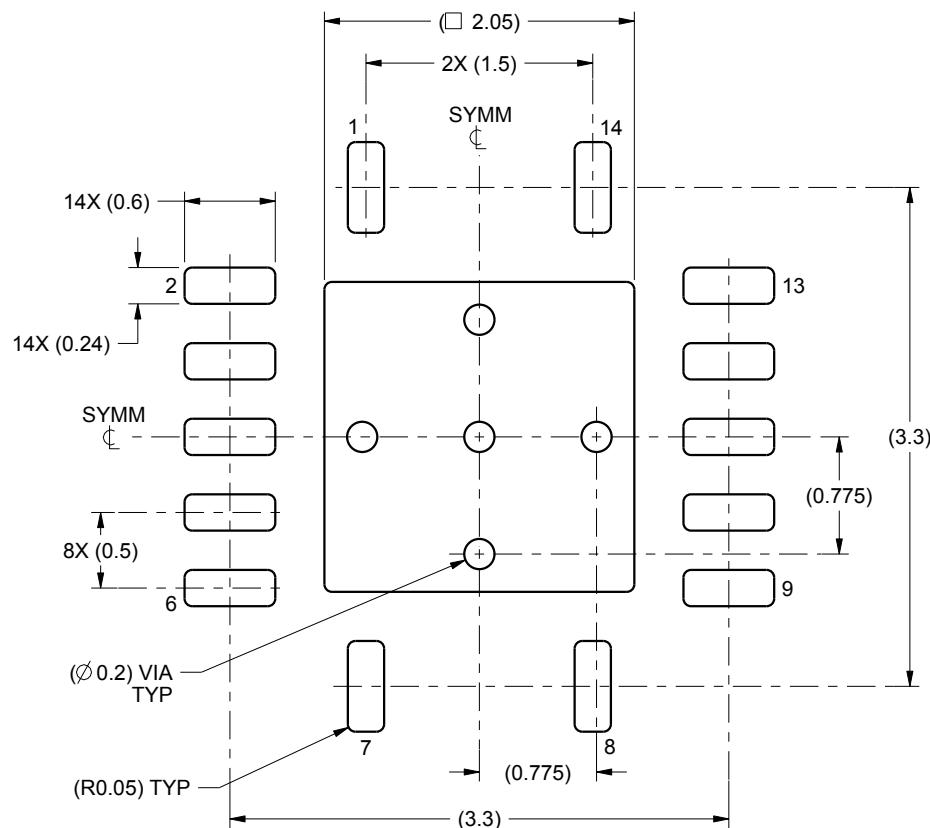
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

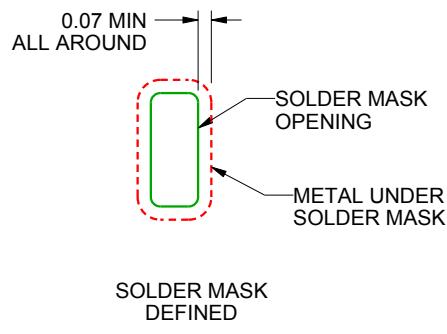
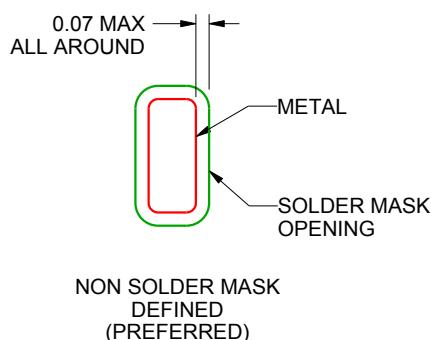
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

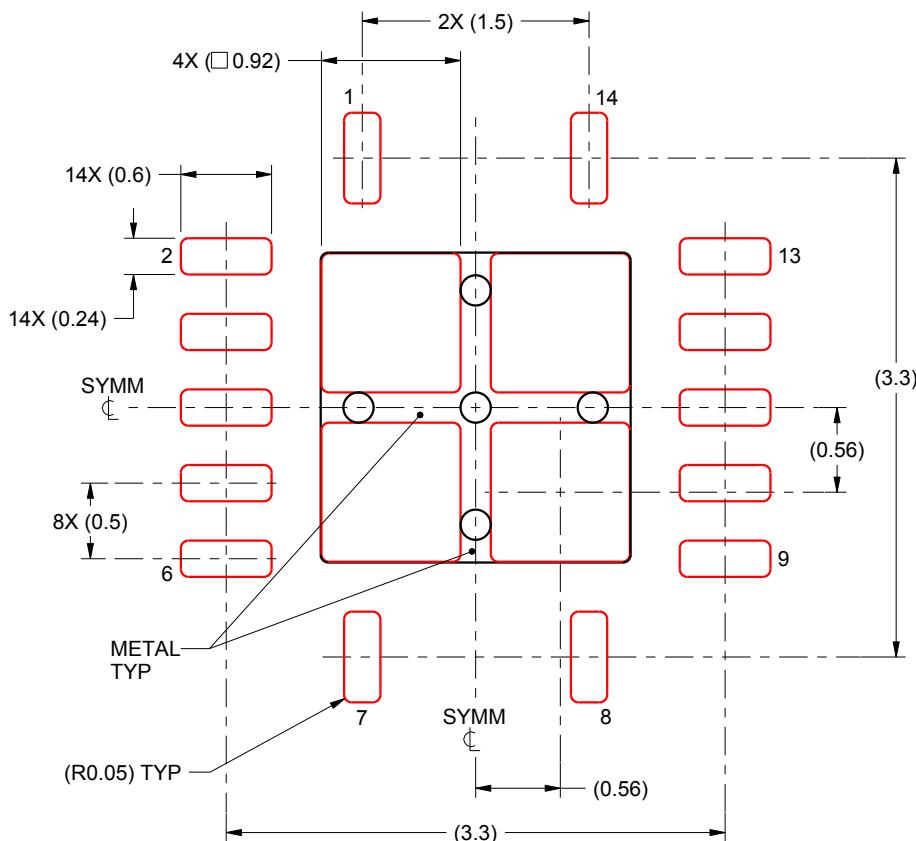
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

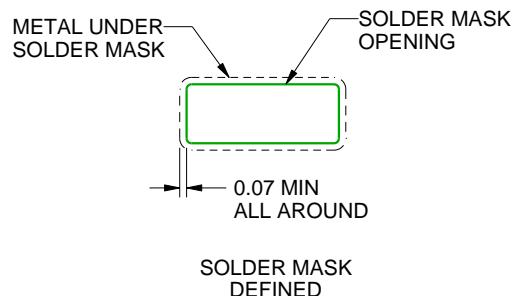
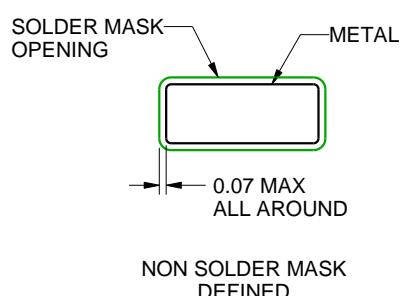
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

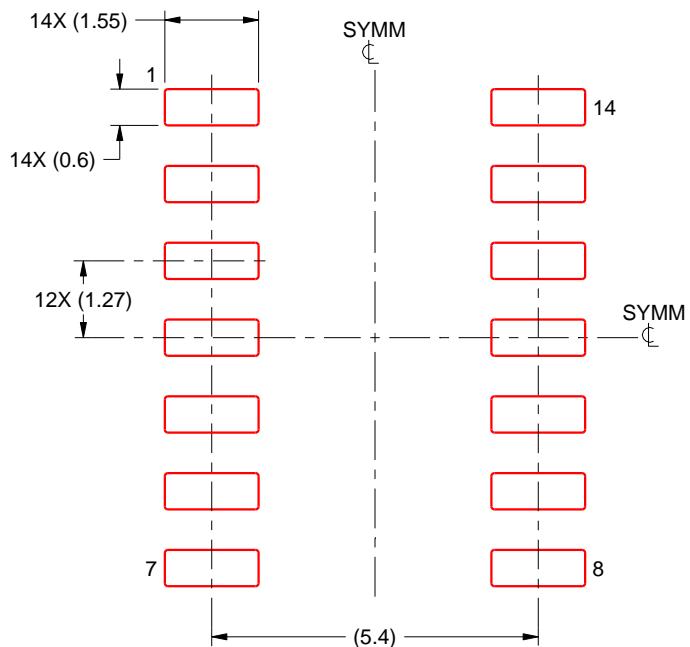
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



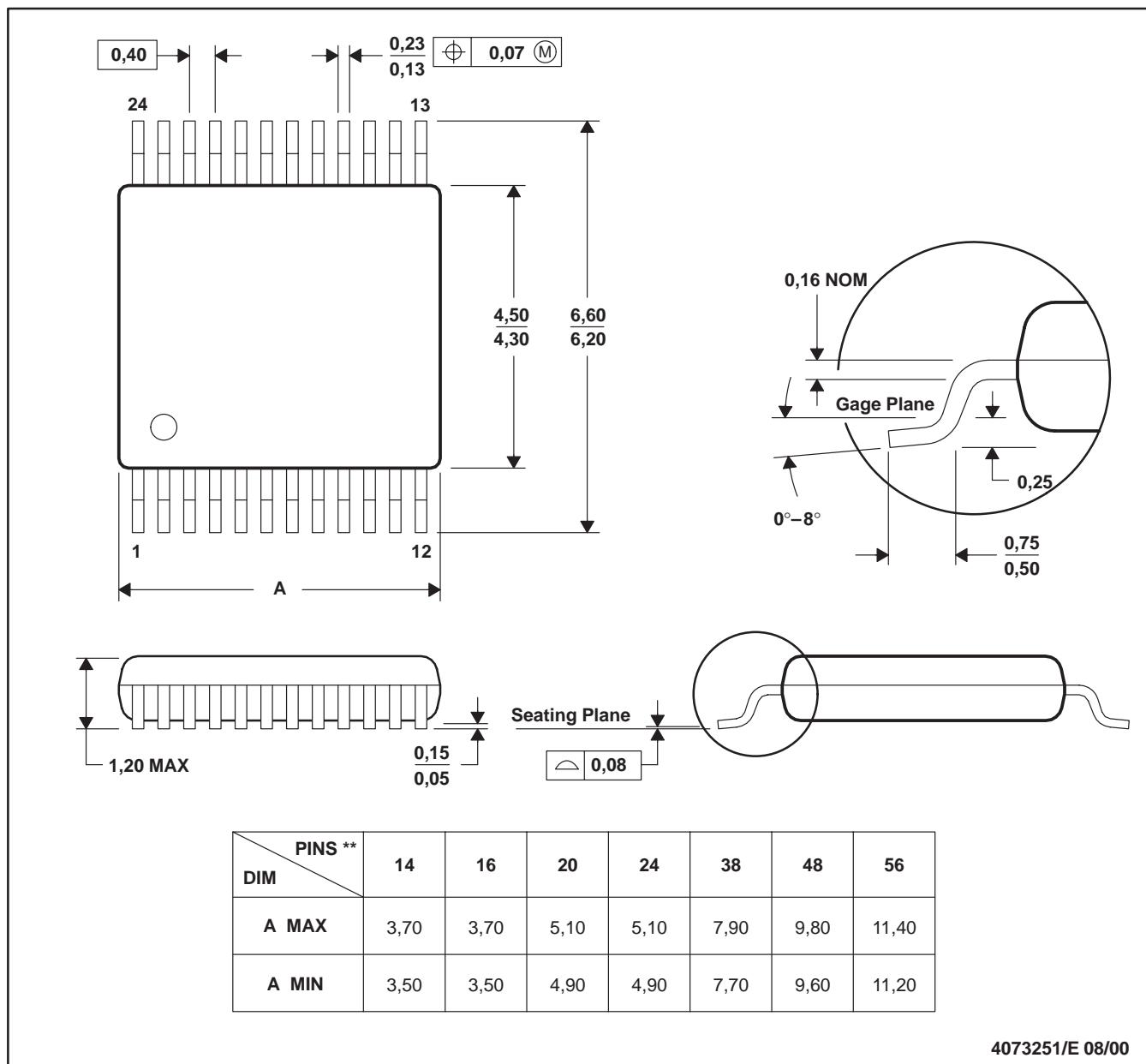
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

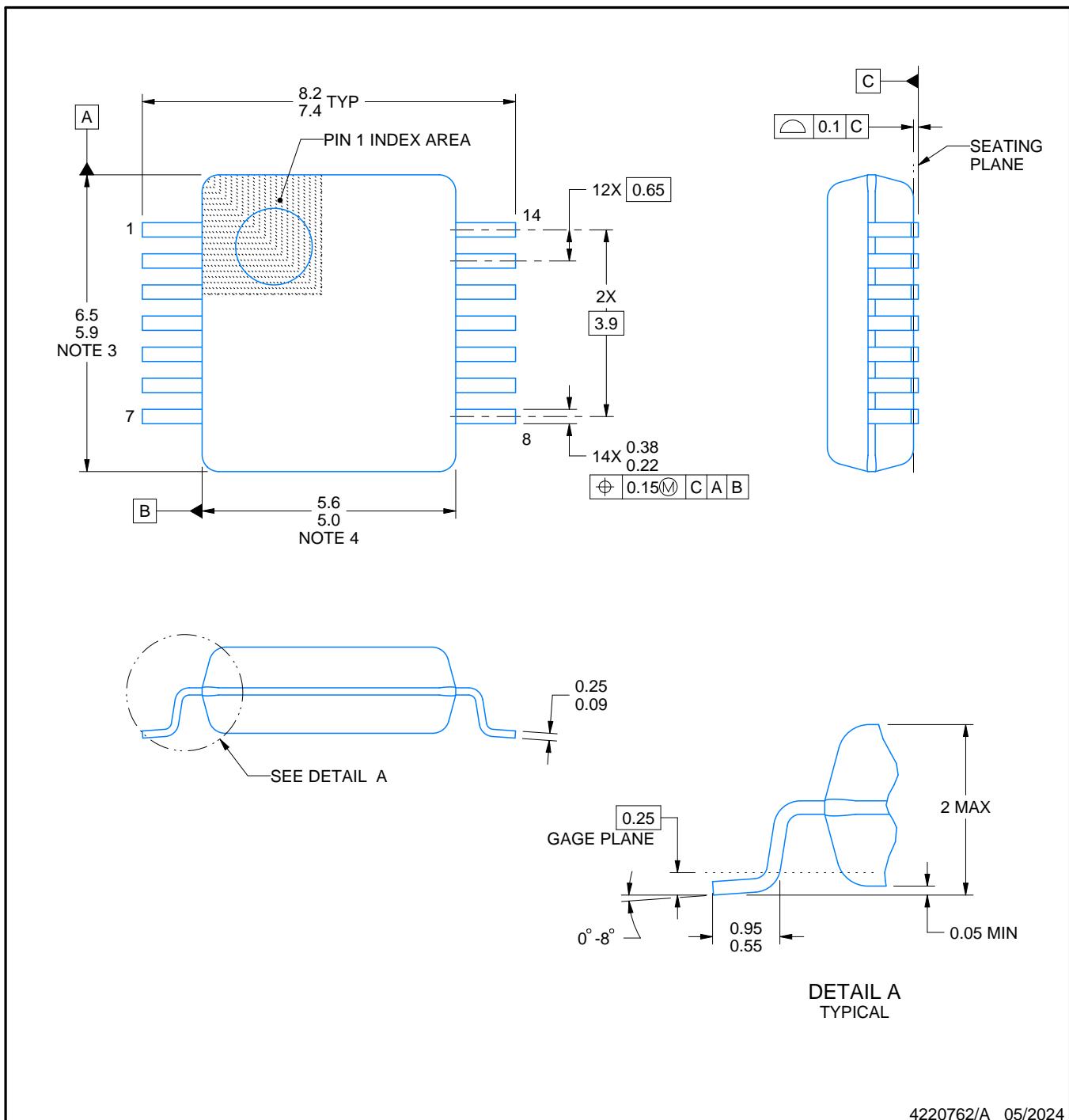


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

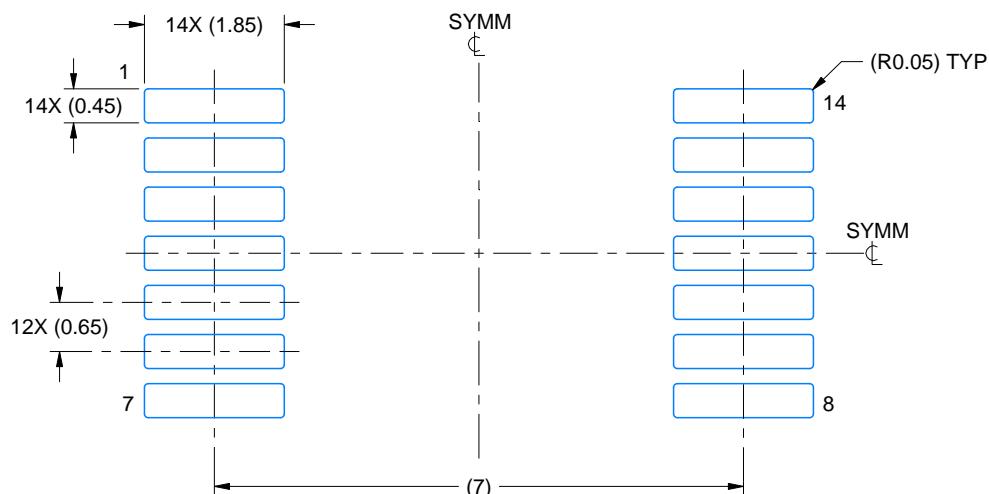
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

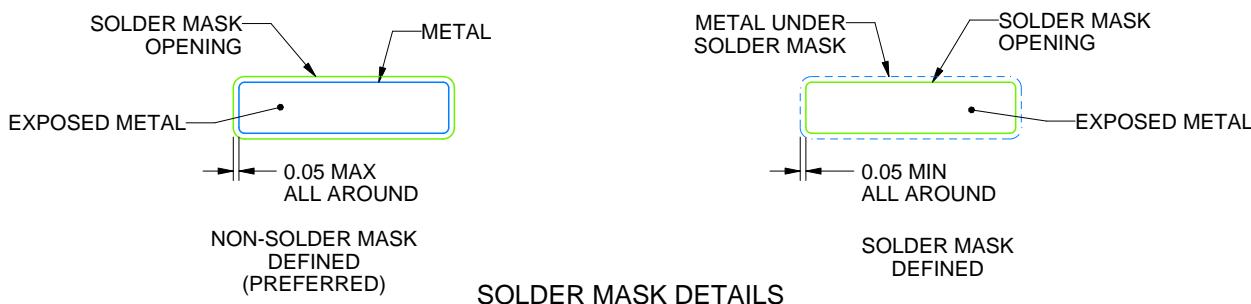
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

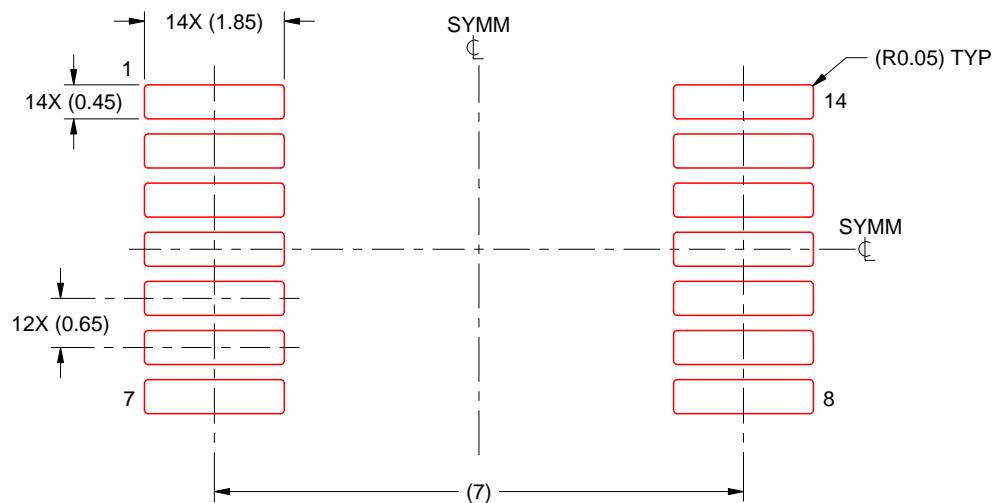
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

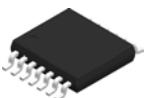
4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

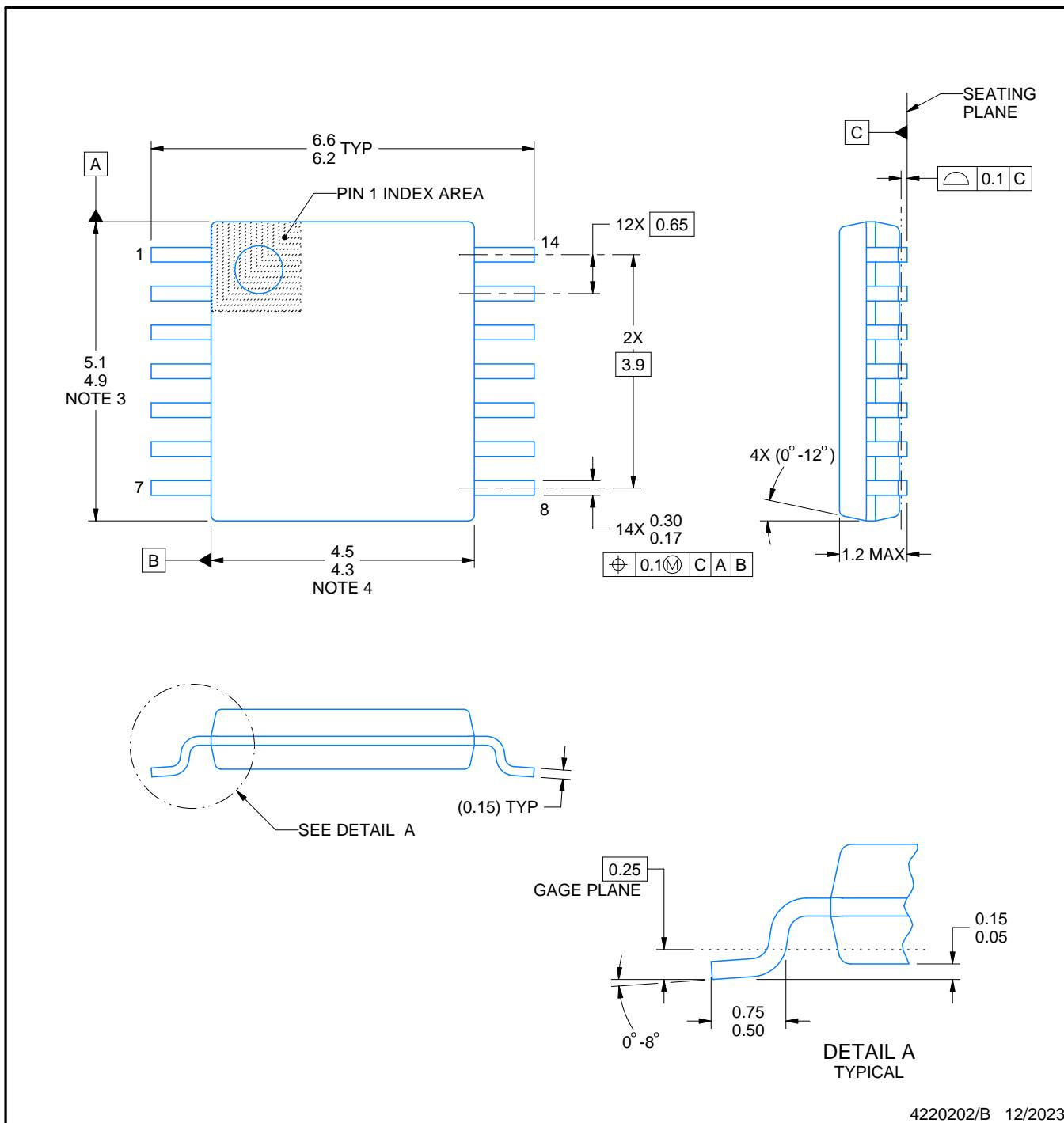
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

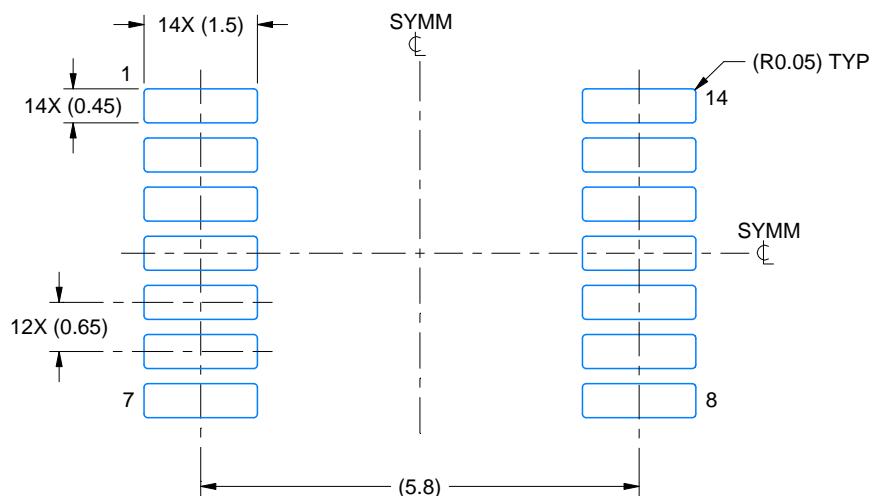
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

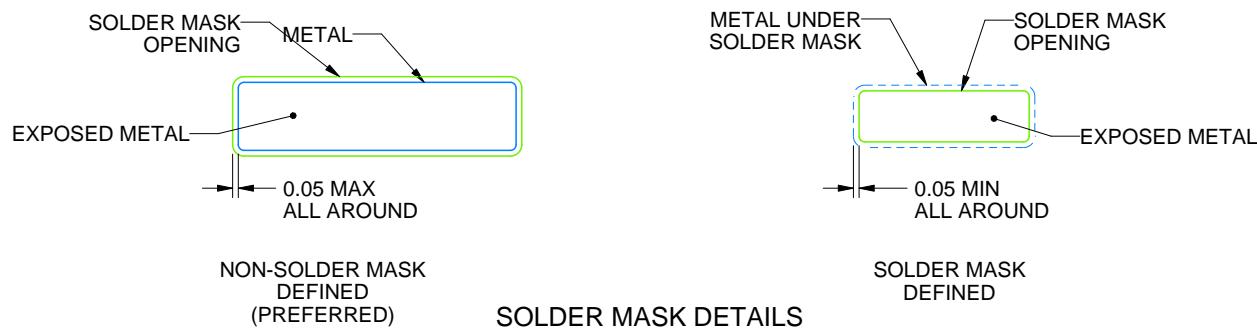
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

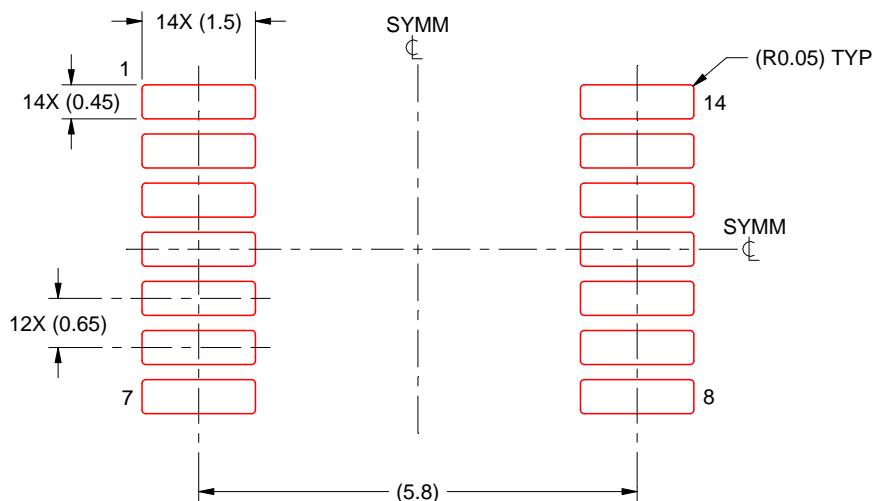
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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