TEXAS INSTRUMENTS

SN54LV00A, SN74LV00A

SCLS389K –SEPTEMBER 1997–REVISED FEBRUARY 2015

Quadruple 2-Input Positive-NAND Gates

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Power Infrastructure
- Network Switch
- Automotive Infotainment
- Servers

3 Description

These quadruple 2-input positive-NAND gates are designed for 2-V to 5.5-V V_{CC} operation.

The SNx4LV00A devices perform the boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4LV00A	VQFN (14)	3.50 mm x 3.50 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOP (14)	10.30 mm x 5.30 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

Table of Contents

5 Revision History

Changes from Revision J (April 2005) to Revision K   **Page**
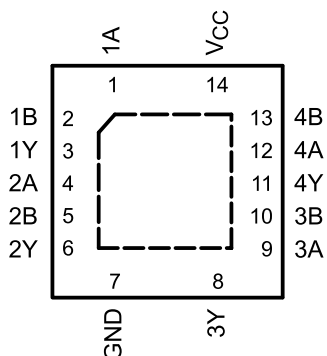
Product Folder Links: *SN54LV00A SN74LV00A*

6 Pin Configuration and Functions

**SN54LV00A . . . J OR W PACKAGE
SN74LV00A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)**

1A	1	14	V_{CC}
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y
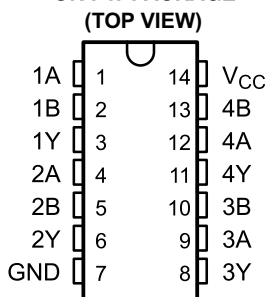
**SN74LV00A . . . RGY PACKAGE
(TOP VIEW)**

		1A	V_{CC}		
		1	14		
1B	2			13	4B
1Y	3			12	4A
2A	4			11	4Y
2B	5			10	3B
2Y	6			9	3A
		7	8		
		GND	3Y		

**SN54LV00A . . . FK PACKAGE
(TOP VIEW)**

	1B	1A	NC	V_{CC}	4B	
	3	2	1	20	19	
1Y	4					18	4A
NC	5					17	NC
2A	6					16	4Y
NC	7					15	NC
2B	8					14	3B
	9	10	11	12	13	
	2Y	GND	NC	3Y	3A	
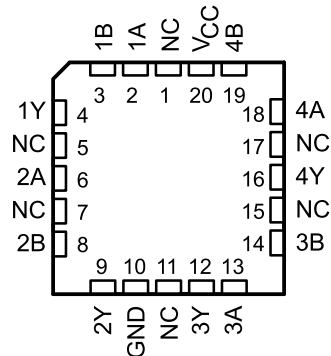
NC - No internal connection

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1A	I	1A Input
2	1B	I	1B Input
3	1Y	O	1Y Output
4	2A	I	2A Input
5	2B	I	2B Input
6	2Y	O	2Y Output
7	GND	–	GND
8	3Y	O	3Y Output
9	3A	I	3A Input
10	3B	I	3B Input
11	4Y	O	4Y Output
12	4A	I	4A Input
13	4B	I	4B Input
14	V_{CC}	—	Power Pin

Submit Documentation Feedback   3

Product Folder Links: *SN54LV00A SN74LV00A*

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Output voltage range[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	+2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			SN54LV00A[2]		SN74LV00A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50		−50	µA
		$V_{CC} = 2.3$ V to 2.7 V		−2		−2	mA
		$V_{CC} = 3$ V to 3.6 V		−6		−6	
		$V_{CC} = 4.5$ V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 2.3$ V to 2.7 V		2		2	mA
		$V_{CC} = 3$ V to 3.6 V		6		6	
		$V_{CC} = 4.5$ V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200		200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100		100	
		$V_{CC} = 4.5$ V to 5.5 V		20		20	
T_A	Operating free-air temperature		−40	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) Product Preview.

7.4 Thermal Information

	THERMAL METRIC[1]	SNx4LV00A						UNIT
		D	DB	DGV	NS	PW	RGY	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.6	107.1	129.0	90.7	122.6	57.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.9	59.6	521	48.3	51.4	70.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	54.4	62.0	49.4	64.4	33.6	
ψ_{JT}	Junction-to-top characterization parameter	14.7	20.5	6.5	14.6	6.7	34	
ψ_{JB}	Junction-to-board characterization parameter	44.5	53.8	61.3	49.1	63.8	33.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	13.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV00A[1]			−40°C to 85°C SN74LV00A		−40°C to 125°C SN74LV00A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC} − 0.1			V_{CC} − 0.1		V_{CC} − 0.1		V
	I_{OH} = −2 mA	2.3 V	2			2		2		
	I_{OH} = −6 mA	3 V	2.48			2.48		2.48		
	I_{OH} = −12 mA	4.5 V	3.8			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I_{OL} = 2 mA	2.3 V			0.4		0.4		0.4	
	I_{OL} = 6 mA	3 V			0.44		0.44		0.44	
	I_{OL} = 12 mA	4.5 V			0.55		0.55		0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20		20		20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5		5		5	µA
C_i	V_I = V_{CC} or GND	3.3 V		3.3					3.3	pF
		5 V		3.3					3.3	

(1) Product Preview.

7.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV00A[1]		−40°C to 85°C SN74LV00A		−40°C to 125°C SN74LV00A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		7.1[2]	12.9[2]	1[2]	16[2]	1	15	1	16	ns
			C_L = 50 pF		9.6	16.6	1	21	1	20	1	21	

(1) Product Preview.
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV00A[1]		−40°C to 85°C SN74LV00A		−40°C to 125°C SN74LV00A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		5[2]	7.9[2]	1[2]	10.5[2]	1	9.5	1	10.5	ns
			C_L = 50 pF		6.9	11.4	1	14	1	13	1	14	

(1) Product Preview.
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV00A[1]		−40°C to 85°C SN74LV00A		−40°C to 125°C SN74LV00A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		3.6[2]	5.5[2]	1[3]	7.5[3]	1	6.5	1	7	ns
			C_L = 50 pF		4.9	7.5	1	9.5	1	8.5	1	9	

(1) Product Preview.
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Product Folder Links: *SN54LV00A SN74LV00A*

7.9 Noise Characteristics[1]

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

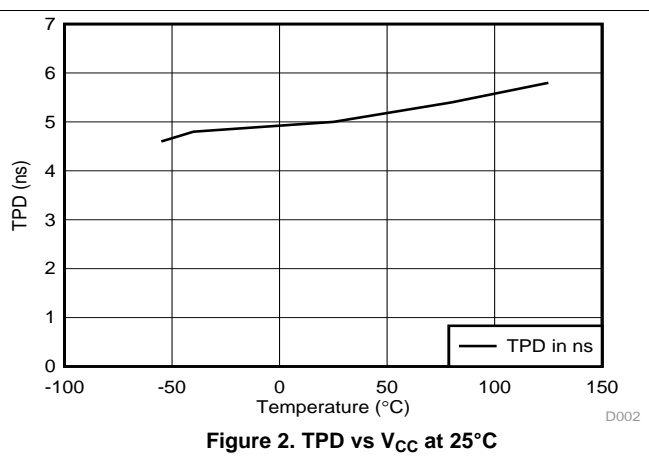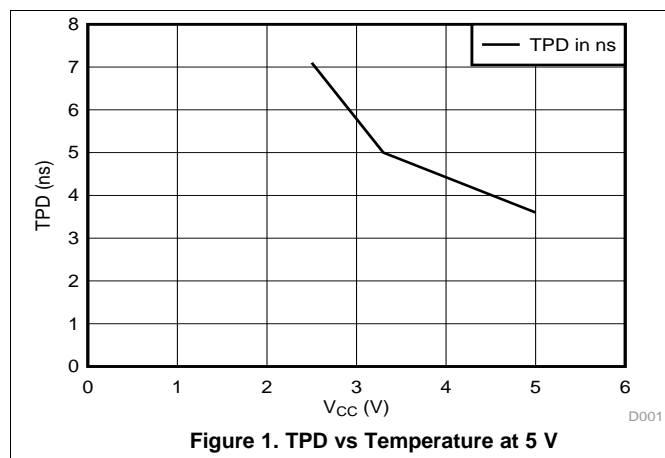| PARAMETER		SN74LV04A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.1	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1)   Characteristics are for surface-mount packages only.
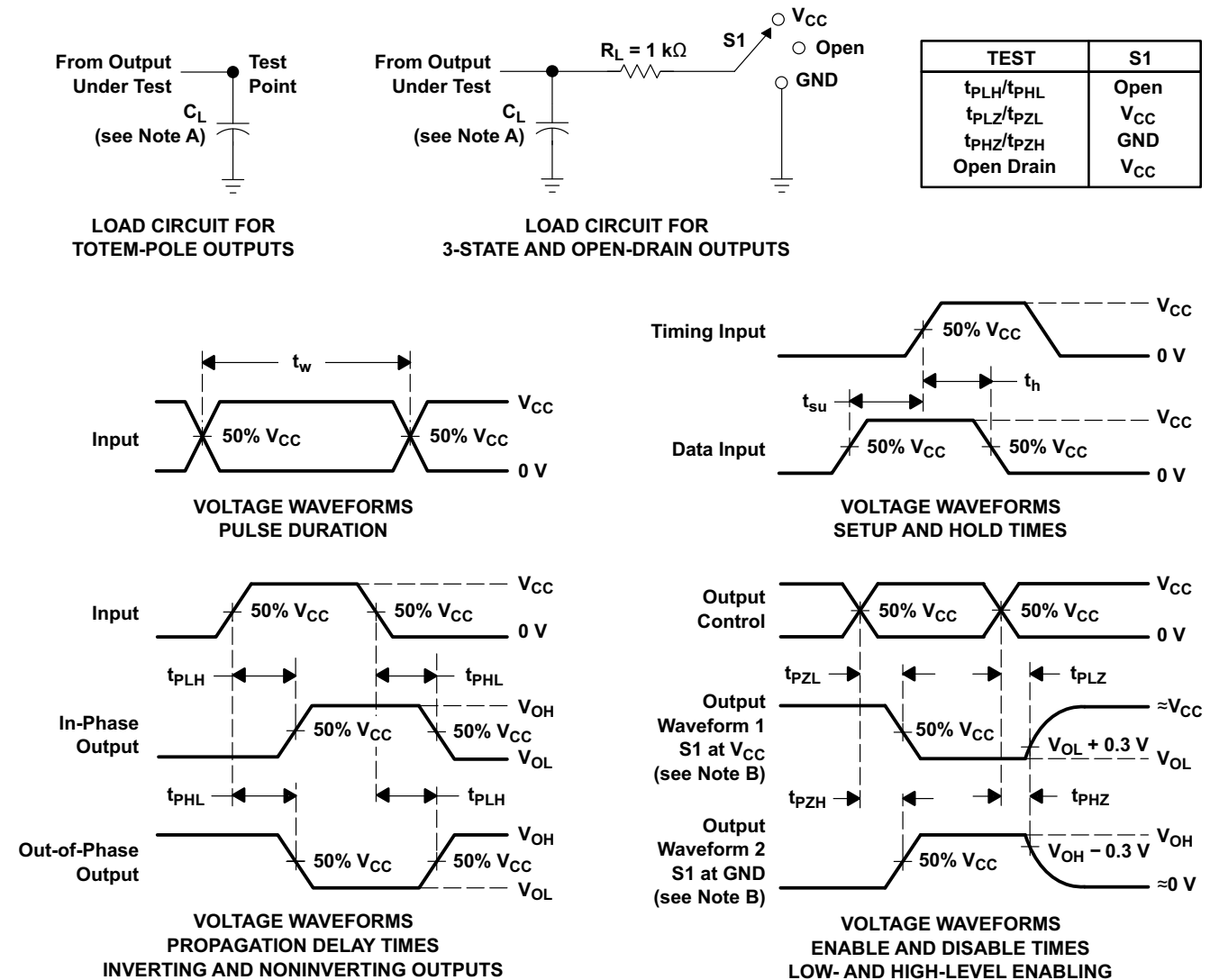
7.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	9.5	pF
				5 V	11	

7.11 Typical Characteristics

Figure 1. TPD vs Temperature at 5 V

Figure 2. TPD vs V_{CC} at 25°C

8 Parameter Measurement Information

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
   D. The outputs are measured one at a time, with one input transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PHL} and t_{PLH} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Product Folder Links: *SN54LV00A SN74LV00A*

# 9 Detailed Description

9.1 Overview

These quadruple 2-input positive-NAND gates are designed for 2-V to 5.5-V V_{CC} operation.

The SNx4LV00A devices perform the boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic

These devices are fully specified for partial-power-down application using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

9.2 Functional Block Diagram
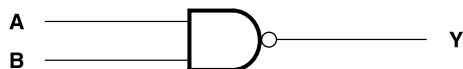
9.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the input or output when V_{CC} is 0 V.

9.4 Device Functional Modes

Table 1. Function Table
(Each Gate)

INPUT		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LV00A is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation.
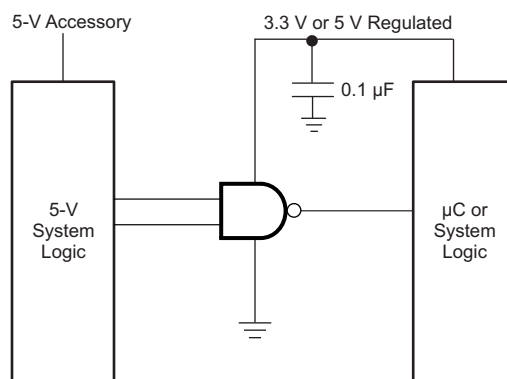
10.2 Typical Application

Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Condition
   – Specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   – Load currents should not exceed 25 mA per output and 50 mA total for the part.
   – Outputs should not be pulled above V_{CC}.

Typical Application (continued)
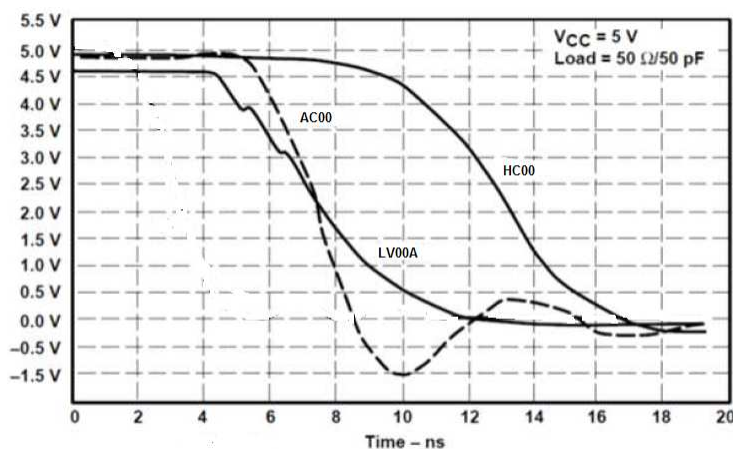
10.2.3 Application Curves

Figure 5. Typical Application Curve

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF capacitors are recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.
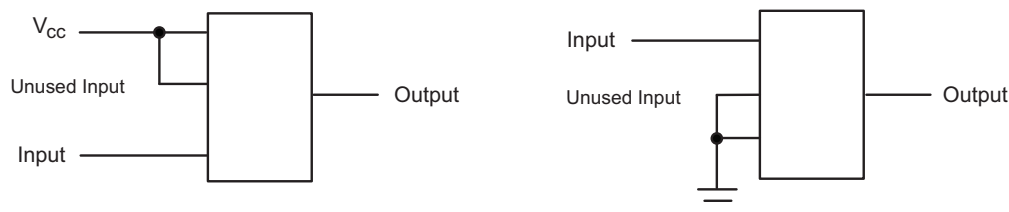
12.2 Layout Example

Figure 6. Layout Diagram

Product Folder Links: *SN54LV00A SN74LV00A*

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV04A	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV00AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	LV00A
SN74LV00ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00ADGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00ADGVR.A	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV00A
SN74LV00ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV00A
SN74LV00APW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	LV00A
SN74LV00APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWRG4	Active	Production	TSSOP (PW) | 14	2000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWRG4	Active	Production	TSSOP (PW) | 14	2000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV00A
SN74LV00APWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	LV00A
SN74LV00ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV00A
SN74LV00ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV00A
SN74LV00ARGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV00A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

User Direction of Feed

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV00ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV00ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV00ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV00ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV00APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV00ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV00ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV00ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV00ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV00ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV00APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV00ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

A

8.2 / 7.4 TYP

PIN 1 INDEX AREA

1

14

12X 0.65

6.5 / 5.9 NOTE 3

2X 3.9

7

8

B

5.6 / 5.0 NOTE 4

14X 0.38 / 0.22

⊕ 0.15 Ⓜ C A B

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

0.25 / 0.09

GAGE PLANE

0.25

0°-8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4220762/A   05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

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14X (1.85)

1

14X (0.45)

SYMM

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220762/A   05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.85)

1

14X (0.45)

SYMM ₵

(R0.05) TYP

14

SYMM ₵

12X (0.65)

7

8

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A   05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

14

12X 0.65

2X

3.9

5.1
4.9
NOTE 3

7

8

14X 0.30
0.17

B

4.5
4.3
NOTE 4

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

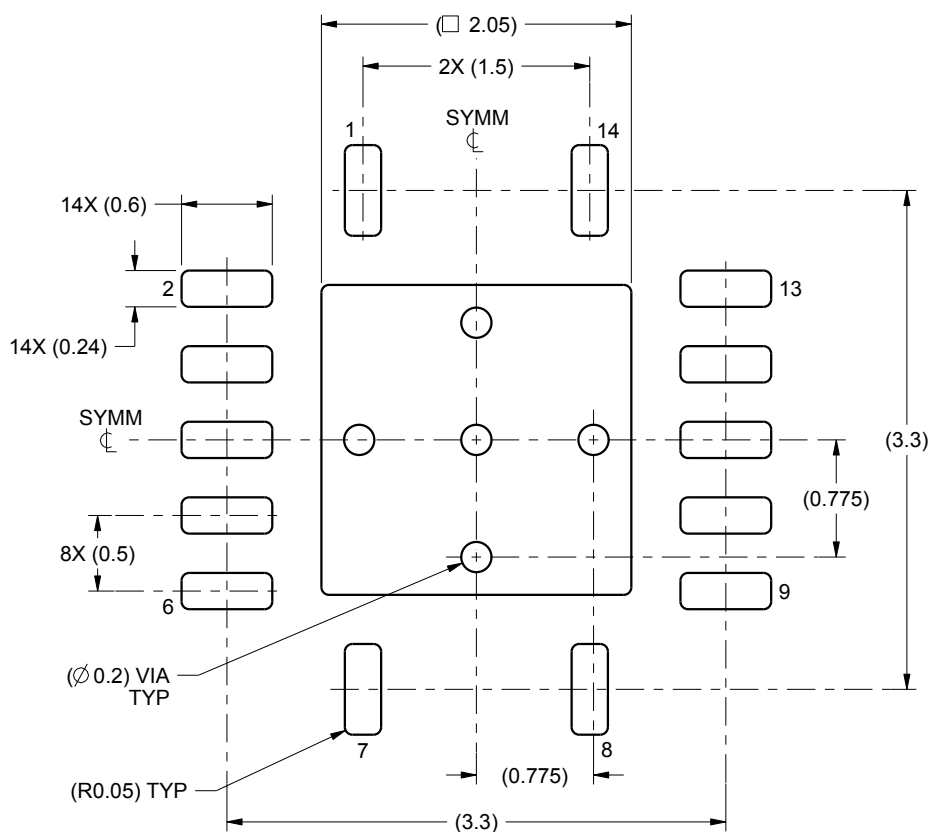0° -8°

DETAIL A
TYPICAL

4220202/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

14X (1.5)

SYMM

1

14X (0.45)

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

SOLDER MASK
DEFINED

4220202/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)

SYMM

1

14X (0.45)

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY 14

3.5 x 3.5, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4231541/A

A

3.65
3.35

B

PIN 1 INDEX AREA

3.65
3.35

1 MAX

0.05
0.00

C

SEATING PLANE

◯ 0.08

☐ 2.05 ± 0.1

2X 1.5

7   8

(0.2) TYP

6   9

2X
2

8X 0.5

2

13

1   14

14X 0.30
0.18

PIN 1 ID
(OPTIONAL)

14X 0.5
0.3

⌖ 0.1 Ⓜ C AⓈ BⓈ
0.05 Ⓜ

4219040/A   09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

RGY0014A

(□ 2.05)

2X (1.5)

SYMM
℄

1   14

14X (0.6)

2

14X (0.24)

13

SYMM
℄

(3.3)

(0.775)

8X (0.5)

6   9

(∅ 0.2) VIA
TYP

7   8

(0.775)

(R0.05) TYP

(3.3)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK
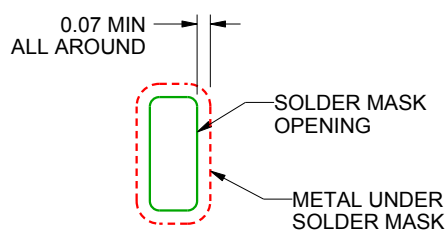
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219040/A   09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).

RGY0014A

2X (1.5)

4X (□ 0.92)

1

14

14X (0.6)

2

14X (0.24)

SYMM

13

(3.3)

(0.56)

8X (0.5)

6

9

METAL
TYP

7

SYMM

8

(R0.05) TYP

(0.56)

(3.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A   09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

7

8

(R0.05)
TYP

(5.4)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.55)

SYMM

1

14X (0.6)

14

12X (1.27)

SYMM

7

8

(5.4)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

　　　　　　　　　　　　　　　　　　　　　PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A　MAX	10,50	10,50	12,90	15,30
A　MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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