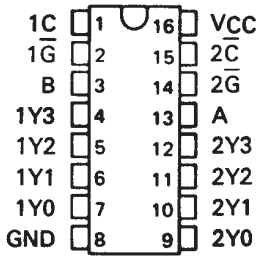
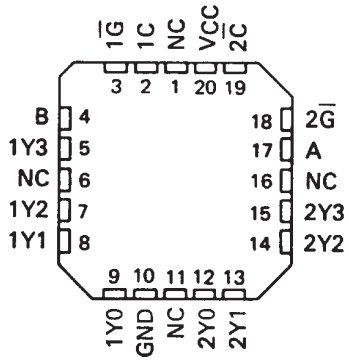
- **Applications:**
  - **Dual 2-to 4-Line Decoder**
  - **Dual 1-to 4-Line Demultiplexer**
  - **3-to 8-Line Decoder**
  - **1-to 8-Line Demultiplexer**
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
  - **Totem Pole ('155, 'LS155A)**
  - **Open-Collector ('156, 'LS156)**

| TYPES | TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS | TYPICAL POWER DISSIPATION |
|---|---|---|
| '155, '156 | 21 ns | 125 mW |
| 'LS155A | 18 ns | 31 mW |
| 'LS156 | 32 ns | 31 mW |

SN54155, SN54156, SN54LS155A,
SN54LS156 . . . J OR W PACKAGE
SN74155, SN74156 . . . N PACKAGE
SN74LS155A, SN74LS156 . . . D OR N PACKAGE
(TOP VIEW)




SN54LS155A, SN54LS156 . . . FK PACKAGE
(TOP VIEW)



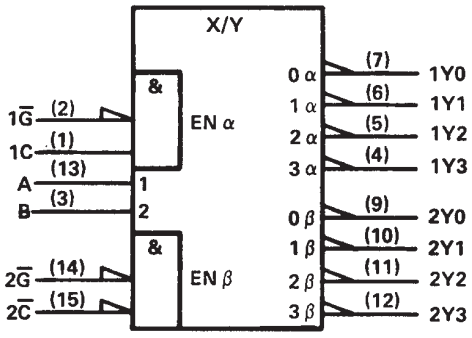

NC - No internal connection

## description

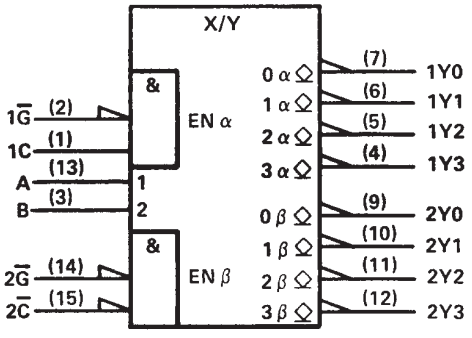
These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at $\overline{2C}$ is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

## logic symbols (2-line to 4-line decoder)†

'155, 'LS155A




'156, 'LS156



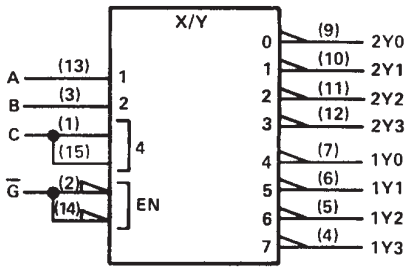

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. For alternative symbols for other applications, see the following page.

Pin numbers shown are for D, J, N, and W packages.

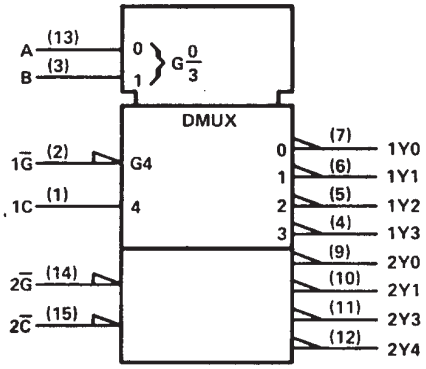
### additional logic symbols (alternatives)†

'155, 'LS155A

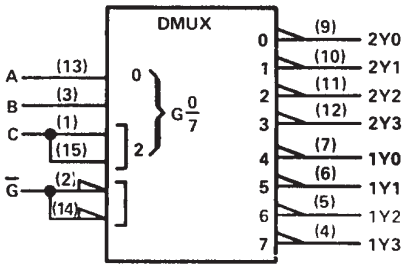
3-line to 8-line Decoder




1-line to 4-line DMUX

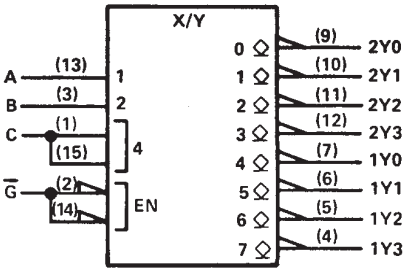



1-line to 8-line DMUX

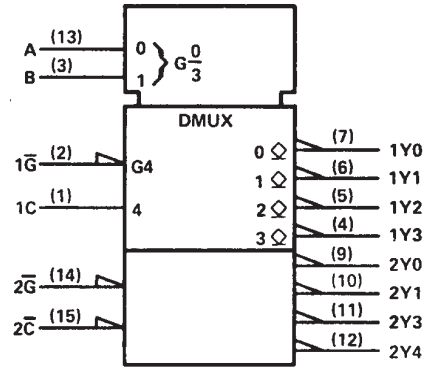



'156, 'LS156

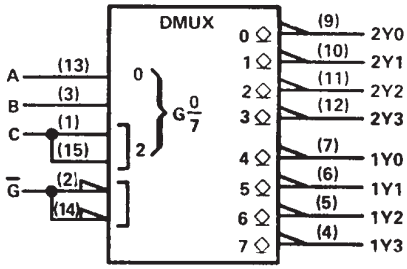
3-line to 8-line Decoder




1-line to 4-line DMUX




1-line to 8-line DMUX

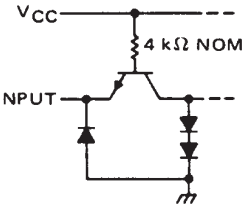



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

### schematics of inputs and outputs

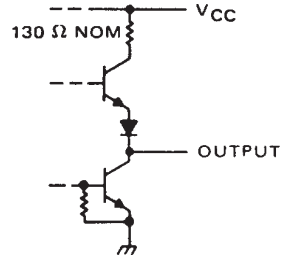
'155, '156

EQUIVALENT OF EACH INPUT



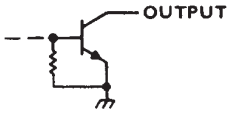

'155

TYPICAL OF ALL OUTPUTS




'156

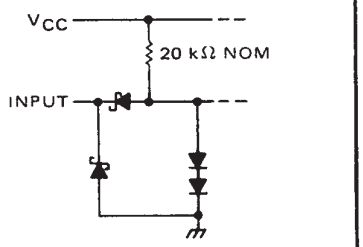
TYPICAL OF ALL OUTPUTS



## schematics of inputs and outputs (continued)

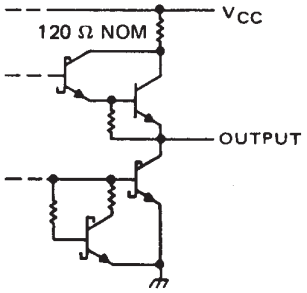
'LS155A, 'LS156

EQUIVALENT OF EACH INPUT



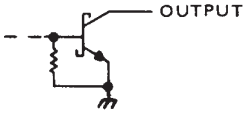

'LS155A

TYPICAL OF ALL OUTPUTS

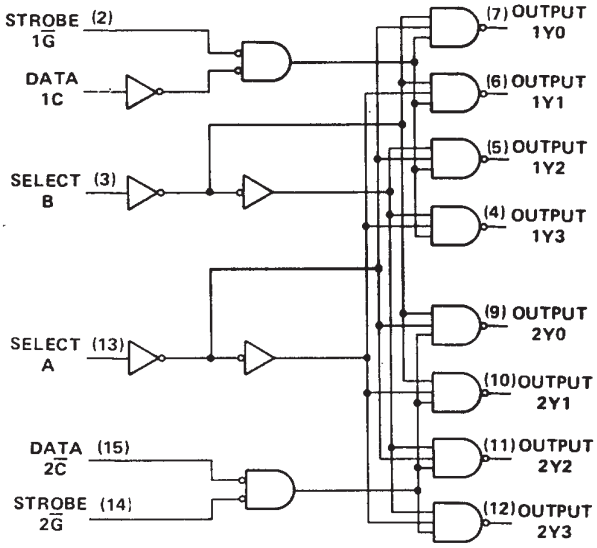



'LS156

TYPICAL OF ALL OUTPUTS




## logic diagram (positive logic)




FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| SELECT | | STROBE | DATA | | | | |
| B | A | $1\overline{G}$ | 1C | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | H | L | H | H | H |
| L | H | L | H | H | L | H | H |
| H | L | L | H | H | H | L | H |
| H | H | L | H | H | H | H | L |
| X | X | X | L | H | H | H | H |

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| SELECT | | STROBE | DATA | | | | |
| B | A | $2\overline{G}$ | 2C | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | L | L | H | H | H |
| L | H | L | L | H | L | H | H |
| H | L | L | L | H | H | L | H |
| H | H | L | L | H | H | H | L |
| X | X | X | H | H | H | H | H |

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SELECT | | | STROBE OR DATA | (0) | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| C† | B | A | $\overline{G}$‡ | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | X | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

†C = inputs 1C and $2\overline{C}$ connected together
‡$\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together
H = high level, L = low level, X = irrelevant

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155A, 'LS156 . . . . . 7 V
Off-state output voltage: '156 . . . . . 5.5 V
'LS156 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | SN54155 | | | SN74155 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −800 | | | −800 | μA |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54155 SN74155 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −8 mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | SN54155 | −20 | | −55 | mA |
| | | | SN74155 | −18 | | −57 | |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | SN54155 | | 25 | 35 | mA |
| | | | SN74155 | | 25 | 40 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

### switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54155 SN74155 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 3 | | 13 | 20 | ns |
| $t_{PHL}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | | | 18 | 27 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 21 | 32 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 21 | 32 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 16 | 24 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 20 | 30 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54156 | | | SN74156 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output voltage, $V_{OH}$ | | | 5.5 | | | 5.5 | V |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54156 SN74156 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −8 mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_{OH}$ = 5.5 V | | | | 250 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | SN54156 | | 25 | 35 | mA |
| | | | SN74156 | | 25 | 40 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER§ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54156 SN74156 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 3 | | 15 | 23 | ns |
| $t_{PHL}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | | | 20 | 30 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 23 | 34 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 23 | 34 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 18 | 27 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 22 | 33 | ns |

§$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54LS155A | | | SN74LS155A | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS155A | | | SN74LS155A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL\ max}$, $I_{OH}$ = −400 μA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL\ max}$ | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | | 6.1 | 10 | | 6.1 | 10 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54LS155A SN74LS155A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, 2$\overline{C}$, 1$\overline{G}$, or 2$\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 10 | 15 | ns |
| $t_{PHL}$ | A, B, 2$\overline{C}$, 1$\overline{G}$, or 2$\overline{G}$ | Y | 2 | | | 19 | 30 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 17 | 26 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 19 | 30 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 18 | 27 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 18 | 27 | ns |

¶$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54LS156 | | | SN74LS156 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output voltage, $V_{OH}$ | | | 5.5 | | | 5.5 | V |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS156 | | | SN74LS156 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max, $V_{OH}$ = 5.5 V | | | | 100 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | | 6.1 | 10 | | 6.1 | 10 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER§ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54LS156 SN74LS156 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, $2\overline{C}$ $1\overline{G}$, or $2\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 25 | 40 | ns |
| $t_{PHL}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | | | 34 | 51 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 31 | 46 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 34 | 51 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 32 | 48 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 32 | 48 | ns |

§$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9750801QEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QE A SNJ54LS155AJ |
| 5962-9750801QFA | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW |
| 5962-9750801QFA | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW |
| SN54LS155AJ | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS155AJ |
| SN54LS155AJ | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS155AJ |
| SN54LS155AJ.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS155AJ |
| SN54LS155AJ.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS155AJ |
| SN54LS156J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS156J |
| SN54LS156J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS156J |
| SN54LS156J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS156J |
| SN54LS156J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS156J |
| SN74LS155AD | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | LS155A |
| SN74LS155AD | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | LS155A |
| SN74LS155ADR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A |
| SN74LS155ADR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A |
| SN74LS155ADR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A |
| SN74LS155ADR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A |
| SN74LS155AN | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU \| NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS155AN |
| SN74LS155AN | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU \| NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS155AN |
| SN74LS155AN.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS155AN |
| SN74LS155AN.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS155AN |
| SN74LS155ANE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS155AN |
| SN74LS155ANE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS155AN |
| SN74LS155ANSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS155A |
| SN74LS155ANSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS155A |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LS155ANSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS155A |
| SN74LS155ANSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS155A |
| SN74LS156D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | LS156 |
| SN74LS156D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | LS156 |
| SN74LS156DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 |
| SN74LS156DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 |
| SN74LS156DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 |
| SN74LS156DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 |
| SN74LS156N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS156N |
| SN74LS156N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS156N |
| SN74LS156N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS156N |
| SN74LS156N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS156N |
| SN74LS156NE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS156N |
| SN74LS156NE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS156N |
| SN74LS156NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS156 |
| SN74LS156NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS156 |
| SN74LS156NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS156 |
| SN74LS156NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS156 |
| SNJ54LS155AJ | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QE A SNJ54LS155AJ |
| SNJ54LS155AJ | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QE A SNJ54LS155AJ |
| SNJ54LS155AJ.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QE A SNJ54LS155AJ |
| SNJ54LS155AJ.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QE A SNJ54LS155AJ |
| SNJ54LS155AW | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54LS155AW | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW |
| SNJ54LS155AW.A | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW |
| SNJ54LS155AW.A | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW |
| SNJ54LS156J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS156J |
| SNJ54LS156J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS156J |
| SNJ54LS156J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS156J |
| SNJ54LS156J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54LS156J |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS155A, SN54LS156, SN74LS155A, SN74LS156 :**

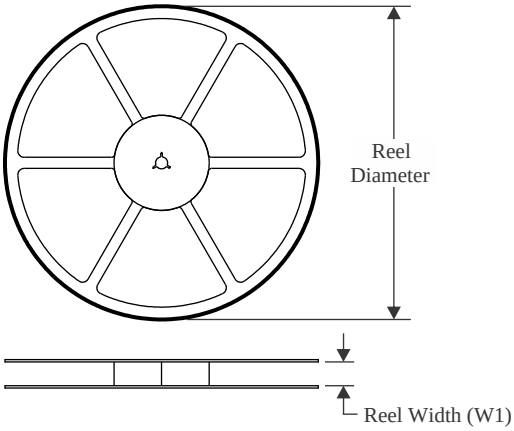
- Catalog : SN74LS155A, SN74LS156
- Military : SN54LS155A, SN54LS156

NOTE: Qualified Version Definitions:

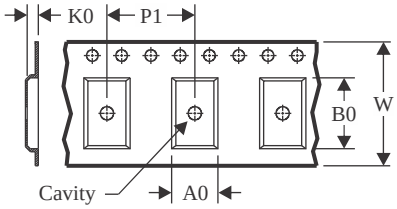
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

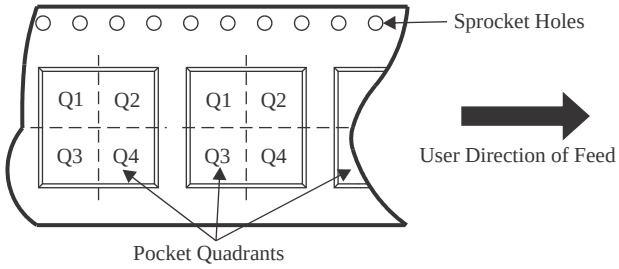



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

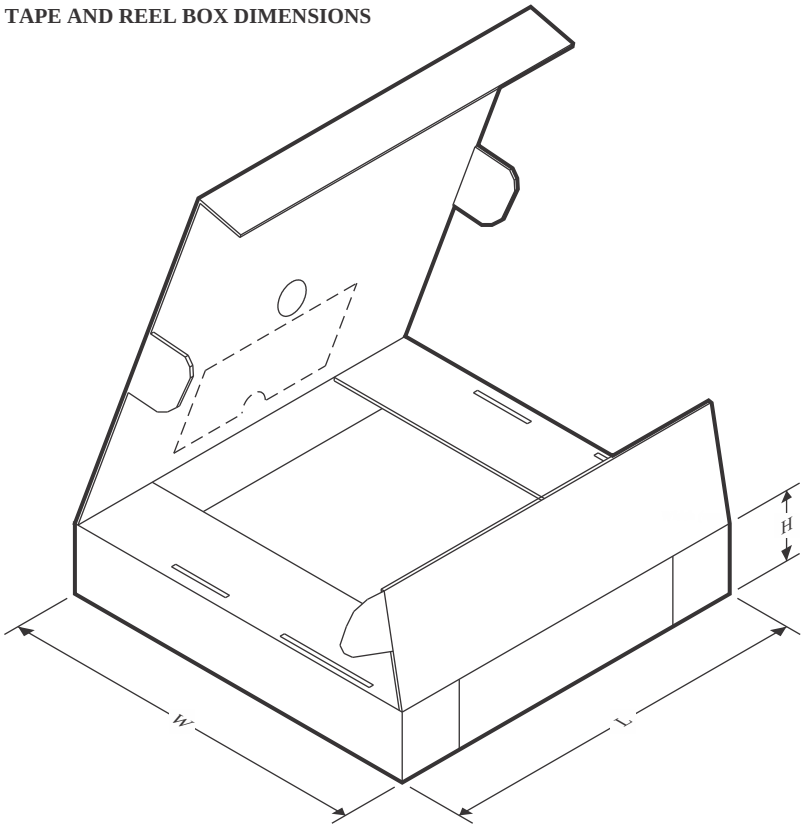
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS155ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS155ANSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS156DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS156NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS156NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

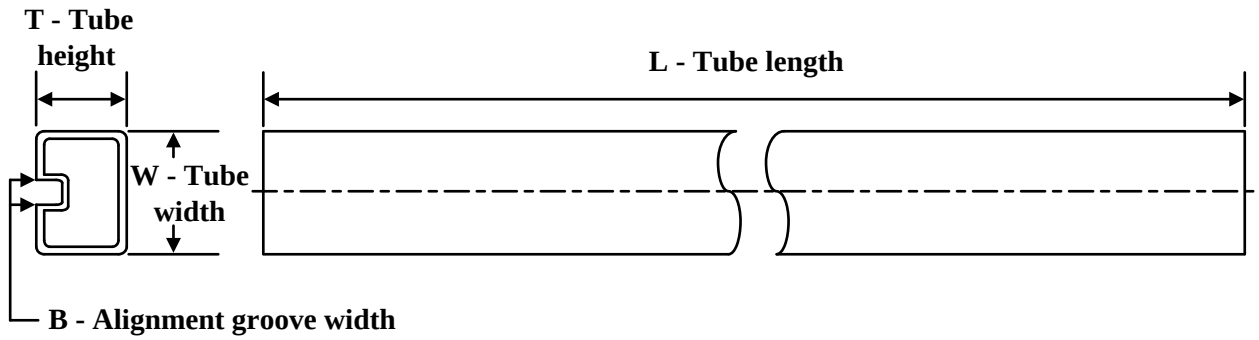
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS155ADR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LS155ANSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS156DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LS156NSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS156NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

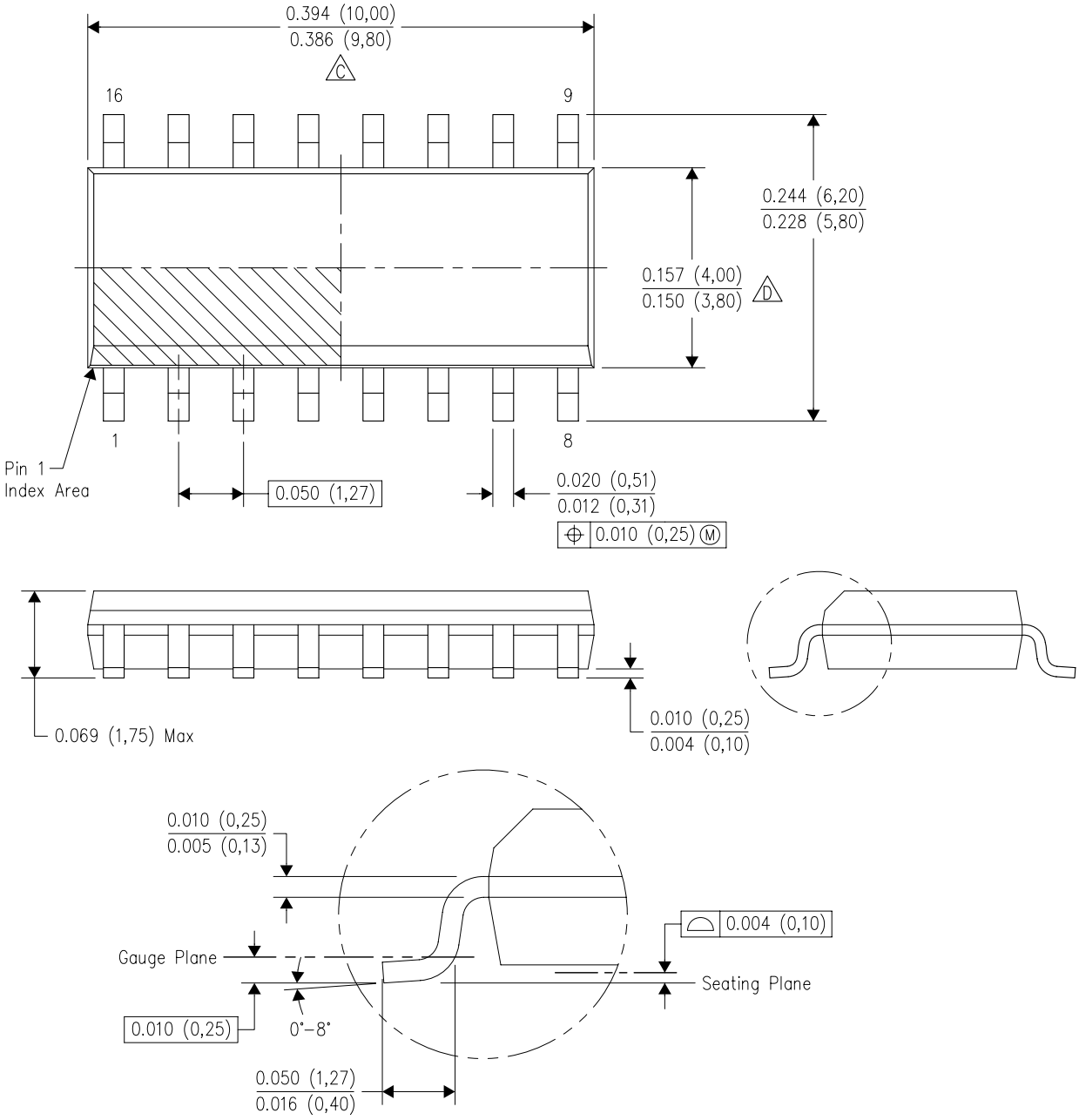
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9750801QFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LS155AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS155AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS155AN.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS155AN.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS155ANE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS155ANE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS156N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS156N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS156N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS156N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS156NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS156NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS155AW | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS155AW.A | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

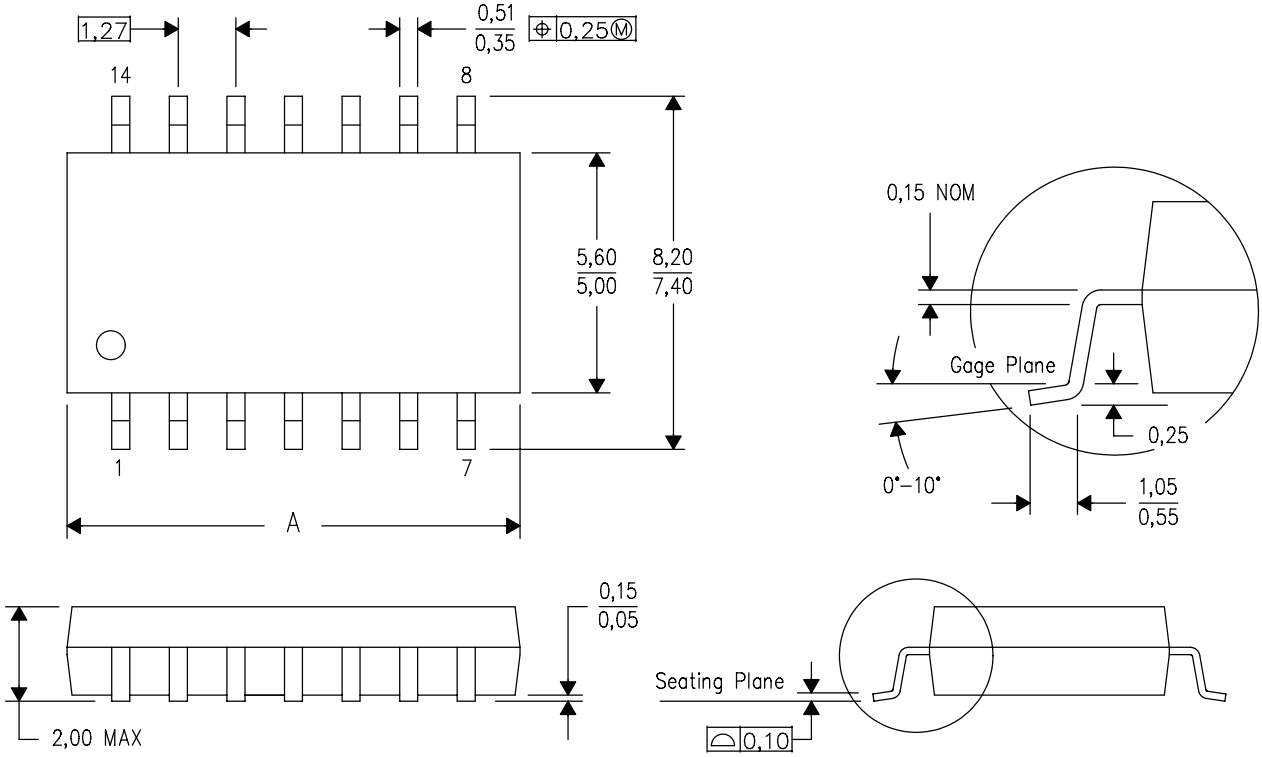



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

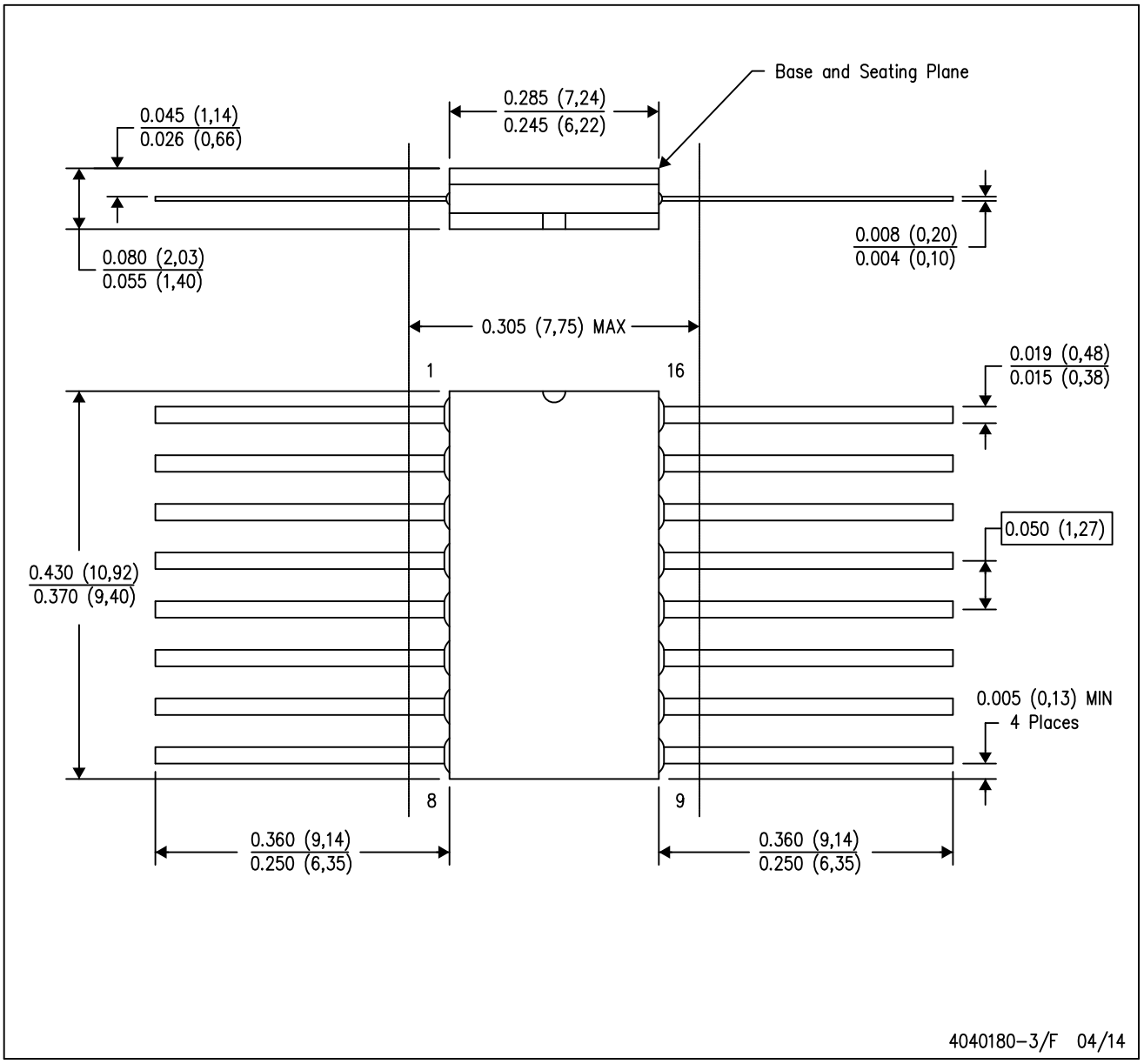



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

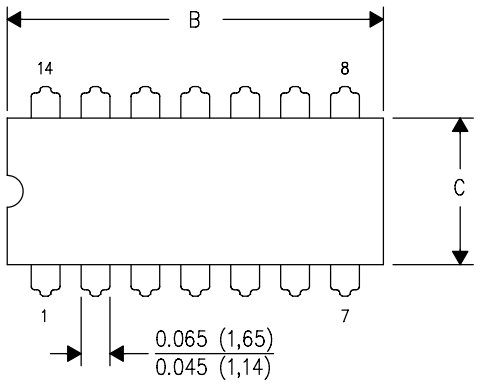



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

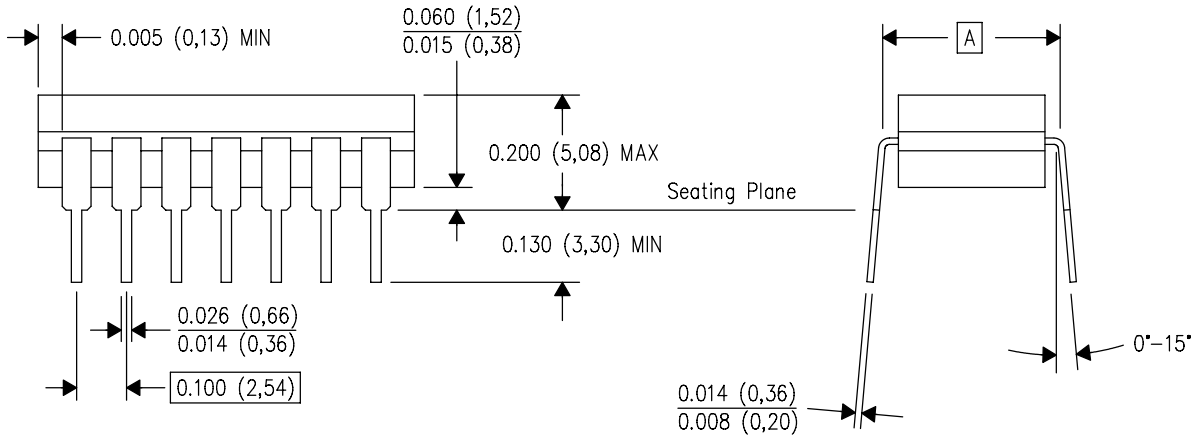
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



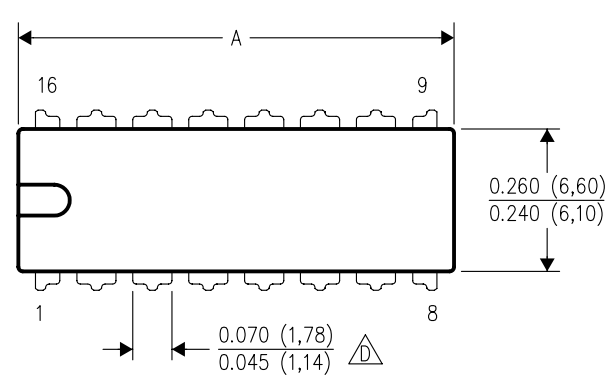

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

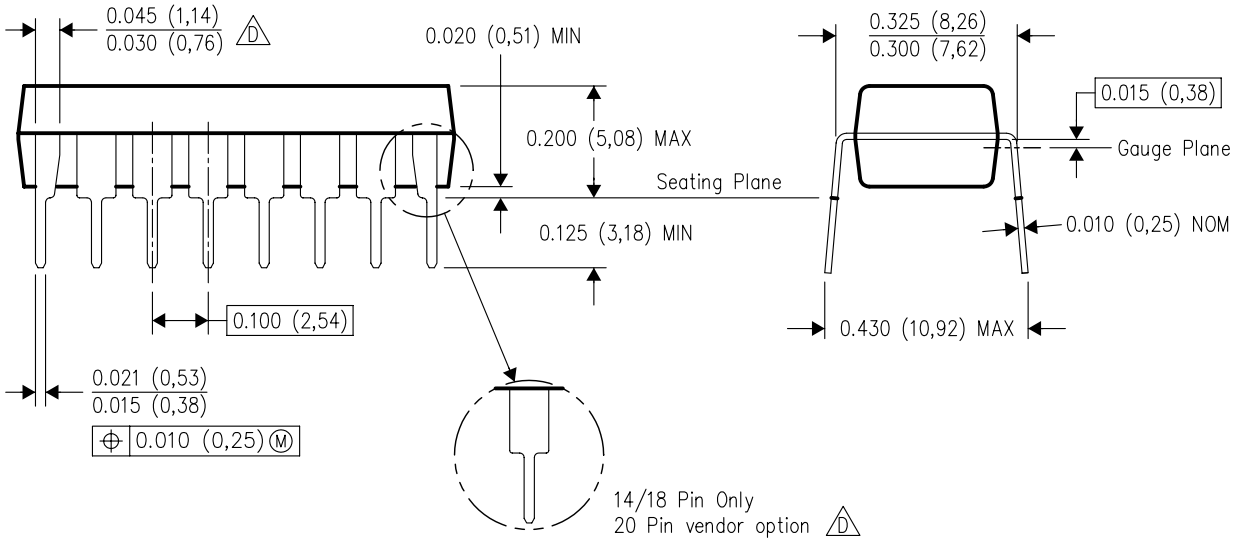
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

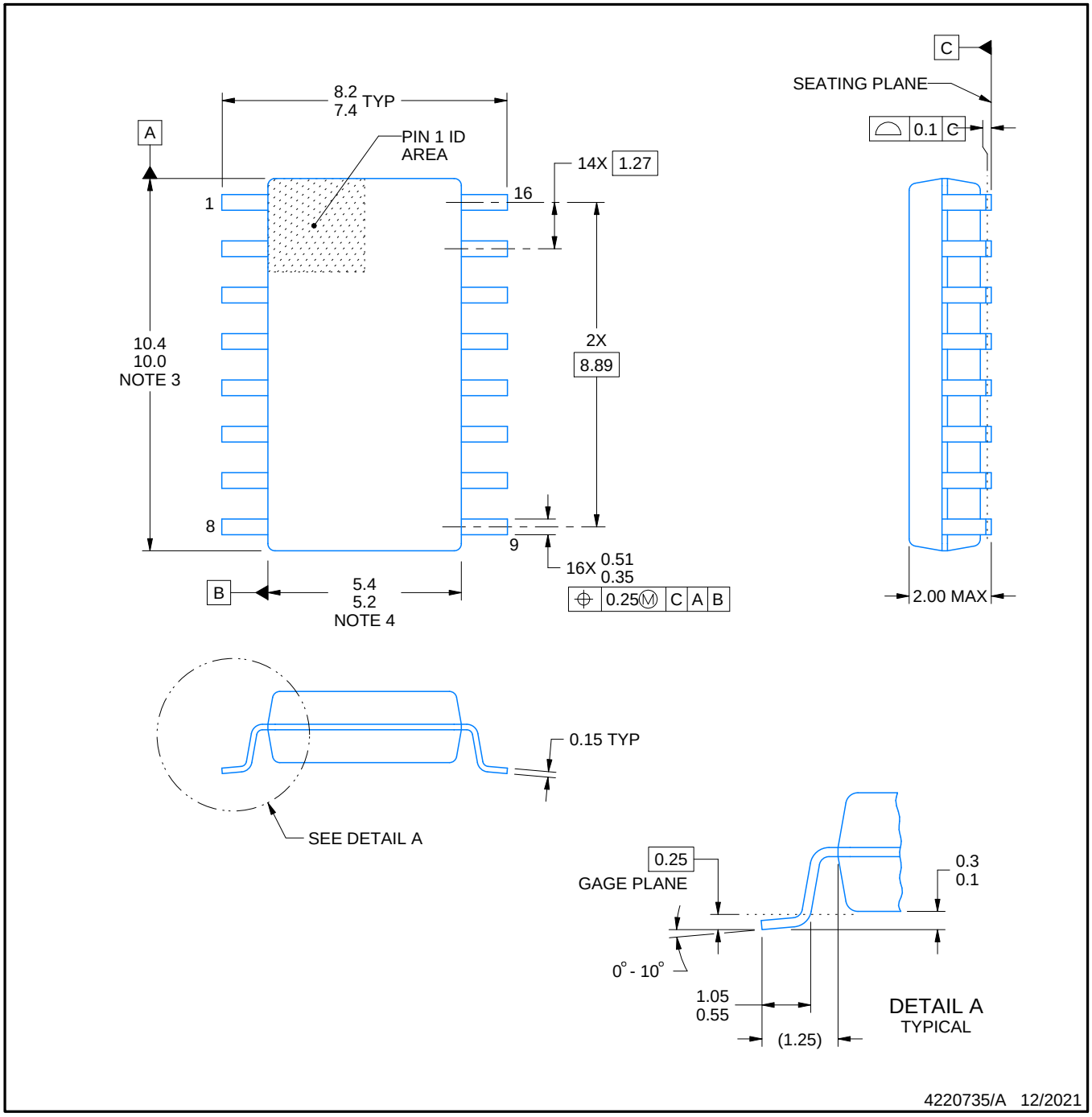



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |



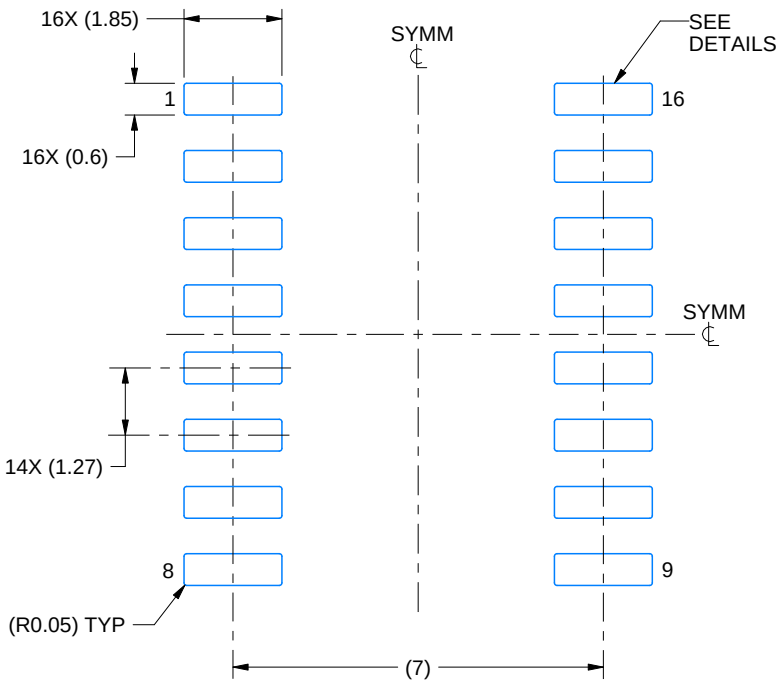

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

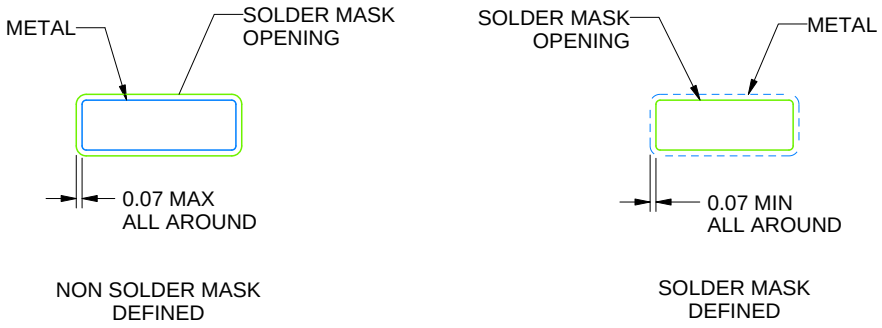



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




SOLDER MASK DETAILS

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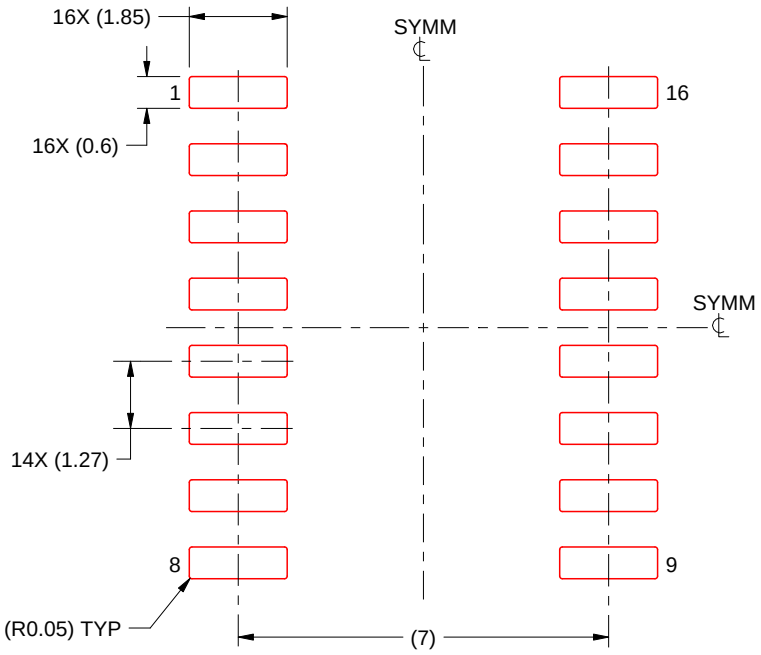
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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