SN74HCS72-Q1 Automotive Qualified Schmitt-Trigger Input Dual D-Type Negative-Edge-Triggered Flip-Flops With Clear and Preset

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classifcation Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 5 V

2 Applications

- Convert a momentary switch to a toggle switch
- Input slow edge-rate signals
- Operate in noisy environments
- Enable CAN Controller Power with wake-up pattern

3 Description

This device contains two independent D-type negative-edge-triggered flip-flops. All inputs include Schmitt-triggers, allowing for slow or noisy input signals. A low level at the preset ($\overline{PRE}$) input sets the output high. A low level at the clear ($\overline{CLR}$) input resets the output low. Preset and clear functions are asynchronous and not dependent on the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs (Q, $\overline{Q}$) on the negative-going edge of the clock ($\overline{CLK}$) pulse. Following the hold-time interval, data at the data (D) input can be changed without affecting the levels at the outputs (Q, $\overline{Q}$).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS72QDRQ1	SOIC (14)	8.70 mm x 3.90 mm
SN74HCS72QPWRQ1	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Benefits of Schmitt-trigger Inputs

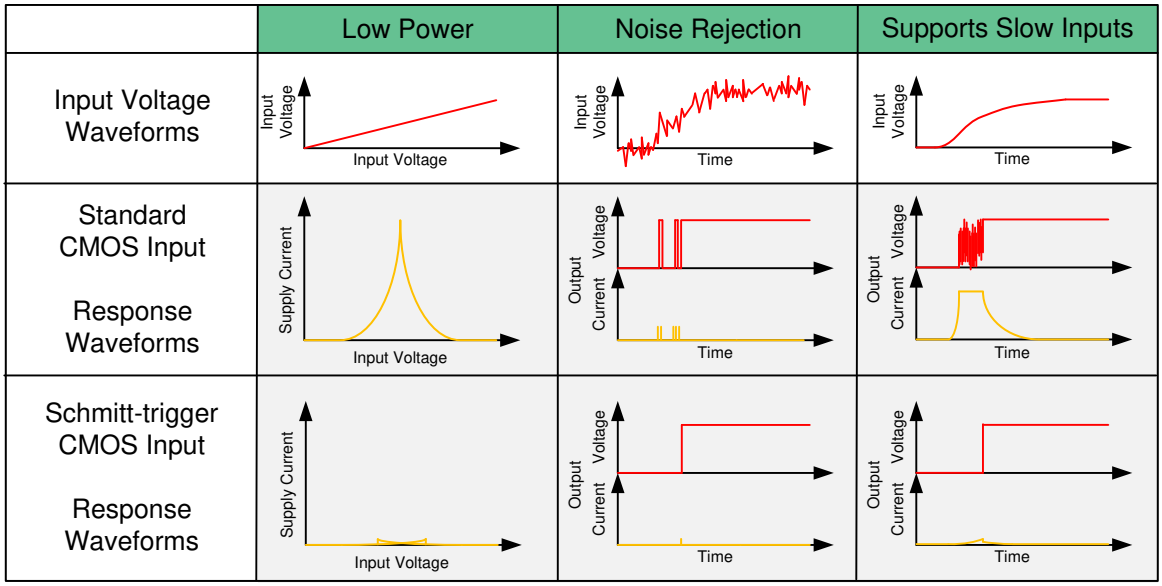


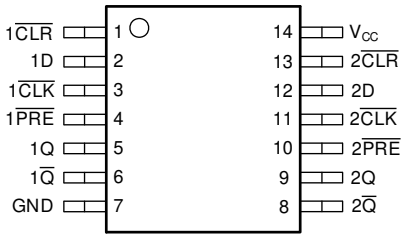
Table of Contents

4 Revision History

DATE	REVISION	NOTES
October 2019	*	Initial release.

5 Pin Configuration and Functions

D and PW Package
14-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1$\overline{CLR}$	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1$\overline{CLK}$	3	Input	Clock for channel 1, falling edge triggered
1$\overline{PRE}$	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1$\overline{Q}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
2$\overline{Q}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2$\overline{PRE}$	10	Input	Preset for channel 2, active low
2$\overline{CLK}$	11	Input	Clock for channel 2, falling edge triggered
2D	12	Input	Data for channel 2
2$\overline{CLR}$	13	Input	Clear for channel 2, active low
V_{CC}	14	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HCS72-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.5	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.1	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})(1)			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1) Guaranteed by design.

6.6 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency			2 V	20	31		MHz
				4.5 V	64	95		
				6 V	74	105		
t_{pd}	Propagation delay	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		$\overline{CLK}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
t_t	Transition-time(1)		Q or $\overline{Q}$	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

(1) t_t = t_r or t_f, whichever is larger

6.7 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		2 V			20	MHz
			4.5 V			64	
			6 V			74	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	8	7		ns
			4.5 V	7	5		
			6 V	7	5		
		$\overline{CLK}$ high or low	2 V	10	5		ns
			4.5 V	9	3		
			6 V	8	2		
t_{su}	Setup time before $\overline{CLK}$ low	Data	2 V	16	11		ns
			4.5 V	6	1		
			6 V	3	1		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	7			ns
			4.5 V	0			
			6 V	0			
t_h	Hold time	Data after CLK ↓	2 V	5			ns
			4.5 V	3			
			6 V	2			

6.8 Typical Characteristics

T_A = 25°C

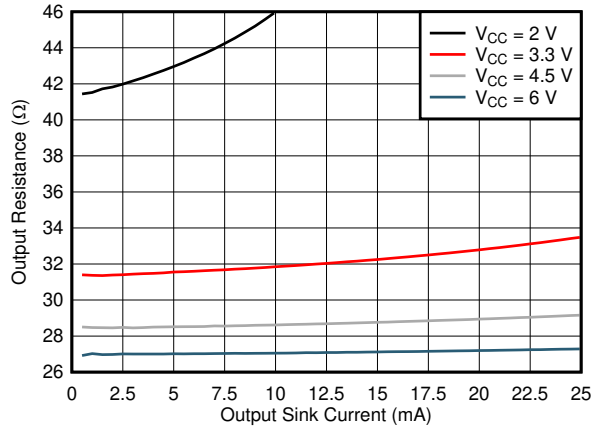


Figure 1. Output driver resistance in LOW state.

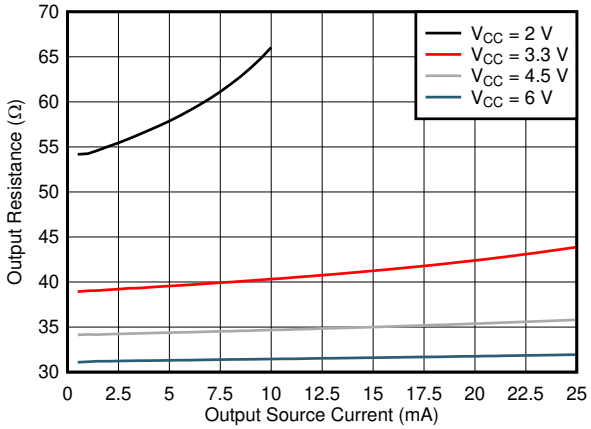


Figure 2. Output driver resistance in HIGH state.

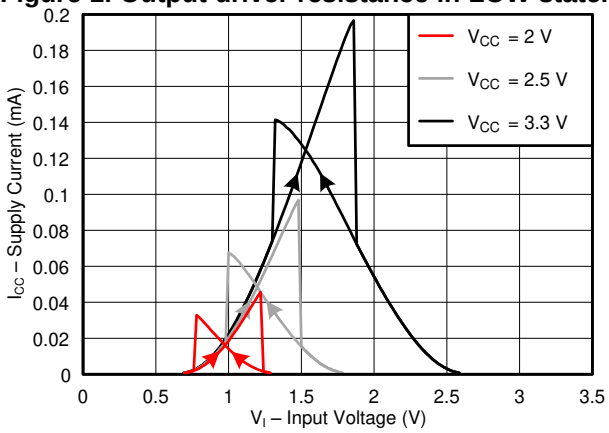


Figure 3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

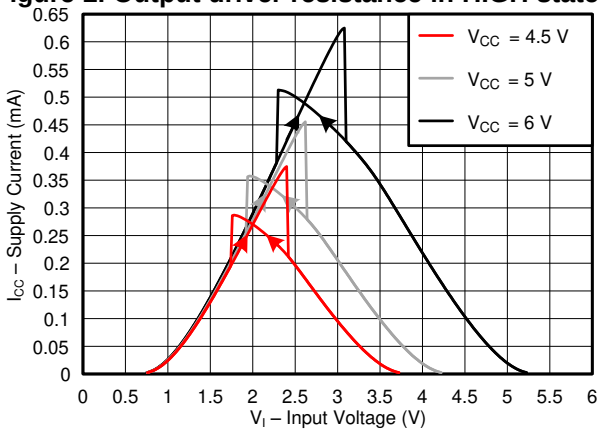


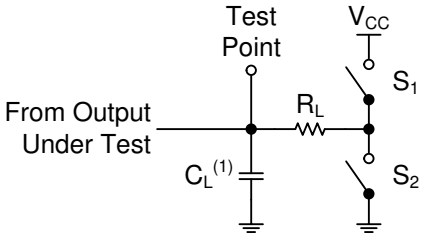
Figure 4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



C_L includes probe and test-fixture capacitance.

Figure 5. Load Circuit

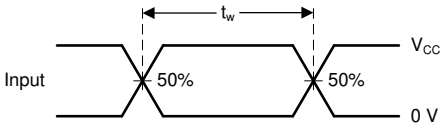


Figure 6. Voltage Waveforms, Pulse Duration

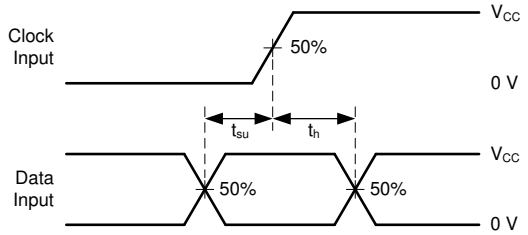
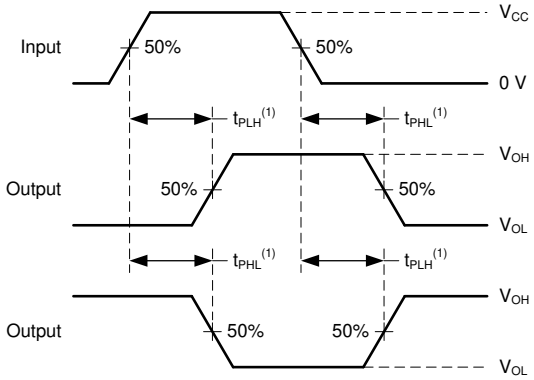


Figure 7. Voltage Waveforms, Setup and Hold Times



Voltage Waveforms, Propagation Delay specifications t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 8. Voltage Waveforms Propagation Delays

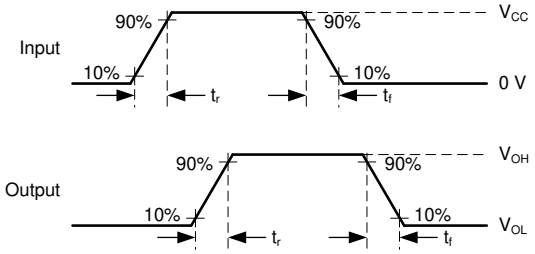


Figure 9. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

Figure 10 describes the SN74HCS72-Q1. As the SN74HCS72-Q1 is a dual D-Type negative-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

8.2 Functional Block Diagram

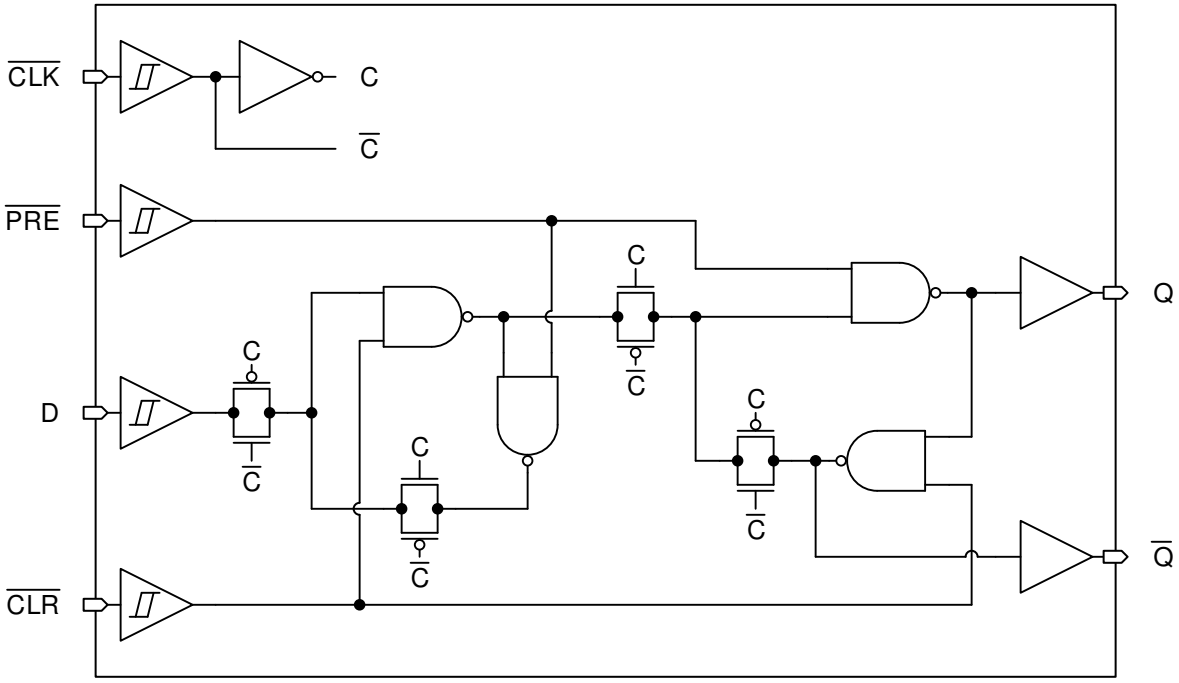


Figure 10. Logic Diagram (Positive Logic) for one channel of SN74HCS72-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Feature Description (continued)

8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 11.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

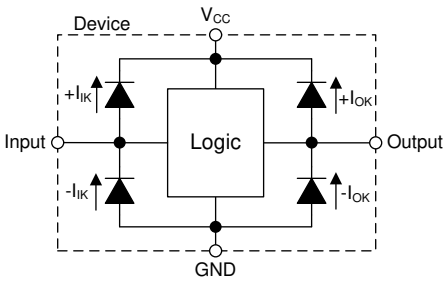


Figure 11. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74HCS72-Q1.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	$\overline{CLK}$	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$
H	H	H	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HCS72-Q1 is an ideal device for taking a CAN wake-up request and converting it to a power supply enable due to its low power consumption and noise rejecting inputs, which eliminate false triggers. CAN communication can occur when the vehicle ignition is off. Therefore, many circuits are designed to work in a standby or low power mode. Because a CAN wake-up request causes the RX pin to pulse LOW, the SN74HCS72-Q1 will trigger off the falling edge enabling the power for the CAN controller. Then the CAN controller powers on for the incoming communication. When communications are finished, the controller sends a reset pulse to the SN74HCS72-Q1 and CAN transceiver putting the circuit back into a standby mode.

9.2 Typical Application

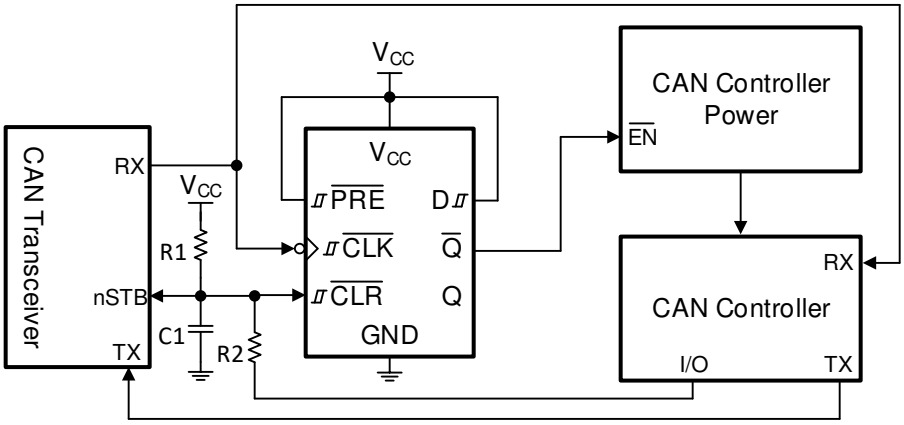


Figure 12. Power Enable Using CAN Wake-up Request

9.2.1 Design Requirements

The SN74HCS72-Q1 device allows flexibility by having complementary outputs for active-high or active-low enables. The supply should be selected such that the device is always powered along with the CAN transceiver. The same supply for both devices is recommended.

With the SN74HCS72-Q1, a power on reset circuit only requires a resistor (R) and capacitor (C) to create a delay. The R and C values create a delay that is approximately 2.2×RC. In this application, it is desired to have the output ($\overline{Q}$) in the HIGH state at startup, so R1 and C1 are connected directly to the $\overline{CLR}$ pin, as shown in Figure 12. A second resistor is needed to limit the current into the CAN controller when it sets the circuit back into standby mode. It is required for the R1 resistor to be at least ten times larger than R2 to avoid a divider circuit (R2 ≤ 10R1).

The D input can be tied either to V_{CC} or ground depending on the desired implementation. In this example, it is tied to V_{CC} to obtain a HIGH signal from $\overline{Q}$ when a wake-up request occurs.

Typical Application (continued)

9.2.1.1 Output Considerations

In general, the load needs to be considered in the design to determine if the device will have the capability to drive it. For this application, we assume that the flip-flop output is transmitting over a relatively short trace (under 10 cm) to a CMOS input.

Primary load factors to consider:

- Load Capacitance: approximately 15 pF
  - See the *Switching Characteristics* section for the capacitive loads tested with this device.
  - Increasing capacitance will proportionally increase output transition times.
  - Decreasing capacitance will proportionally decrease output transition times, and can produce ringing due to very fast transition rates. A 25-Ω resistor can be added in series with the output if ringing needs to be dampened.
- Load Current: expected maximum of 10 µA
  - Leakage current into connected devices.
  - Parasitic current from other components.
  - Resistive load current.
- Output Voltage: see *Electrical Characteristics* for output voltage ratings at a given current.
  - Output HIGH (V_{OH}) and output LOW (V_{OL}) voltage levels affect the input voltage, V_{IH} and V_{IL}, respectively, to subsequent devices.

9.2.1.2 Input Considerations

The SN74HCS72-Q1 has Schmitt-trigger inputs. Schmitt-trigger inputs have no limitation on transition rate, however the input voltage must be larger than $V_{T+(max)}$ to be guaranteed to be read as a logic high, and below $V_{T-(min)}$ to be guaranteed to be read as a logic low, as defined in the *Electrical Characteristics*. Do not exceed the values specified in the *Absolute Maximum Ratings* or the device could be damaged.

9.2.1.3 Timing Considerations

The SN74HCS72-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in *Timing Characteristics* is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Characteristics*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Characteristics*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *Timing Characteristics*.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
   - Input thresholds are listed in the *Electrical Characteristics*.
   - Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the *Absolute Maximum Ratings*. Do not exceed the absolute maximum voltage rating of the device or it could be damaged.
2. Recommended Output Conditions:
   - Load currents should not exceed the value listed in the *Absolute Maximum Ratings*.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the

Typical Application (continued)

output current.

9.2.3 Application Curve

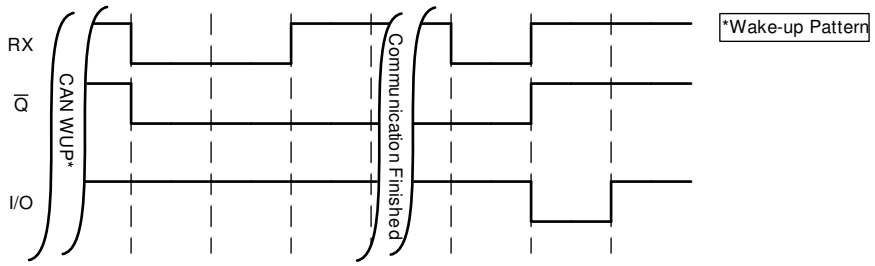


Figure 13. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1-µF capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in Figure 14 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

11.2 Layout Example

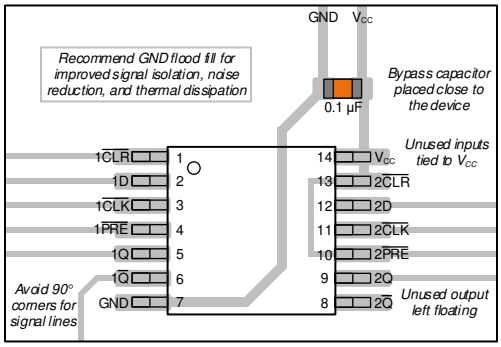


Figure 14. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Reduce Noise and Save Power with the New HCS Logic Family* application report
- Texas Instruments, *Understanding Schmitt Triggers* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS72QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q1
SN74HCS72QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q1
SN74HCS72QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q
SN74HCS72QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74HCS72-Q1 :

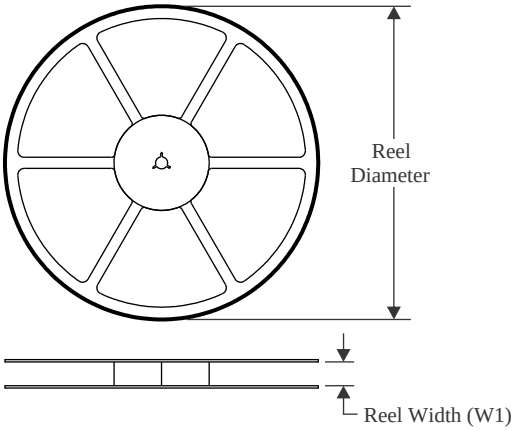
- Catalog : SN74HCS72

NOTE: Qualified Version Definitions:

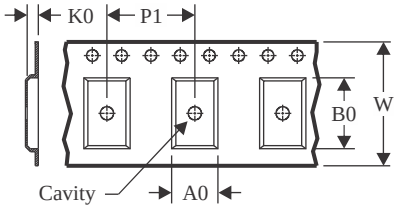
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

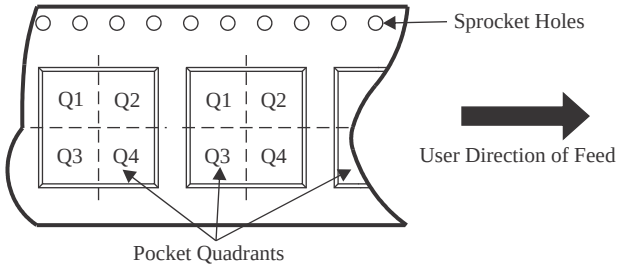


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

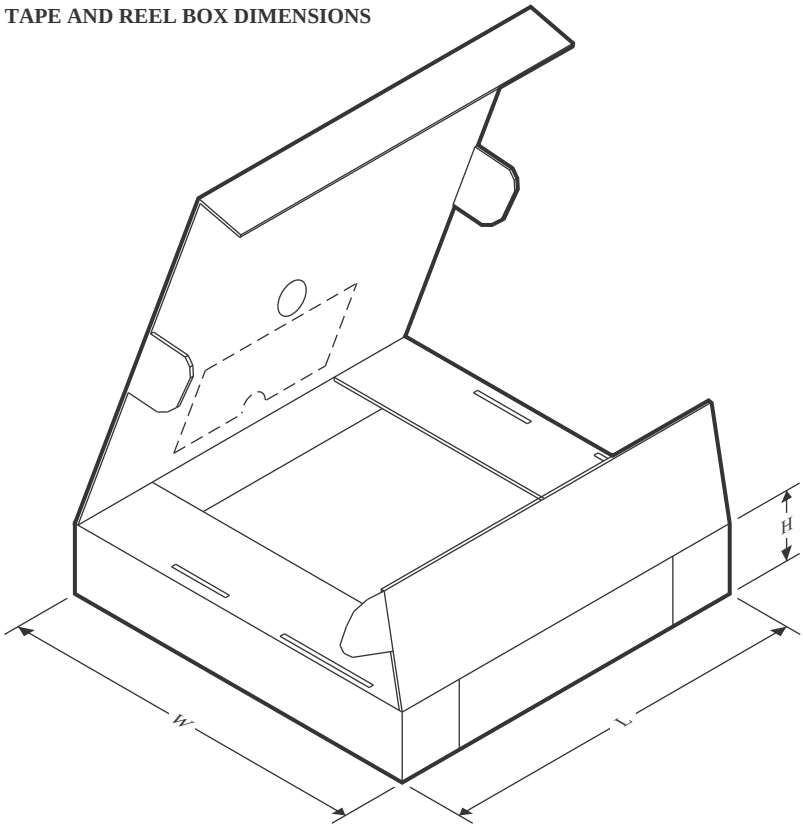
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS72QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS72QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

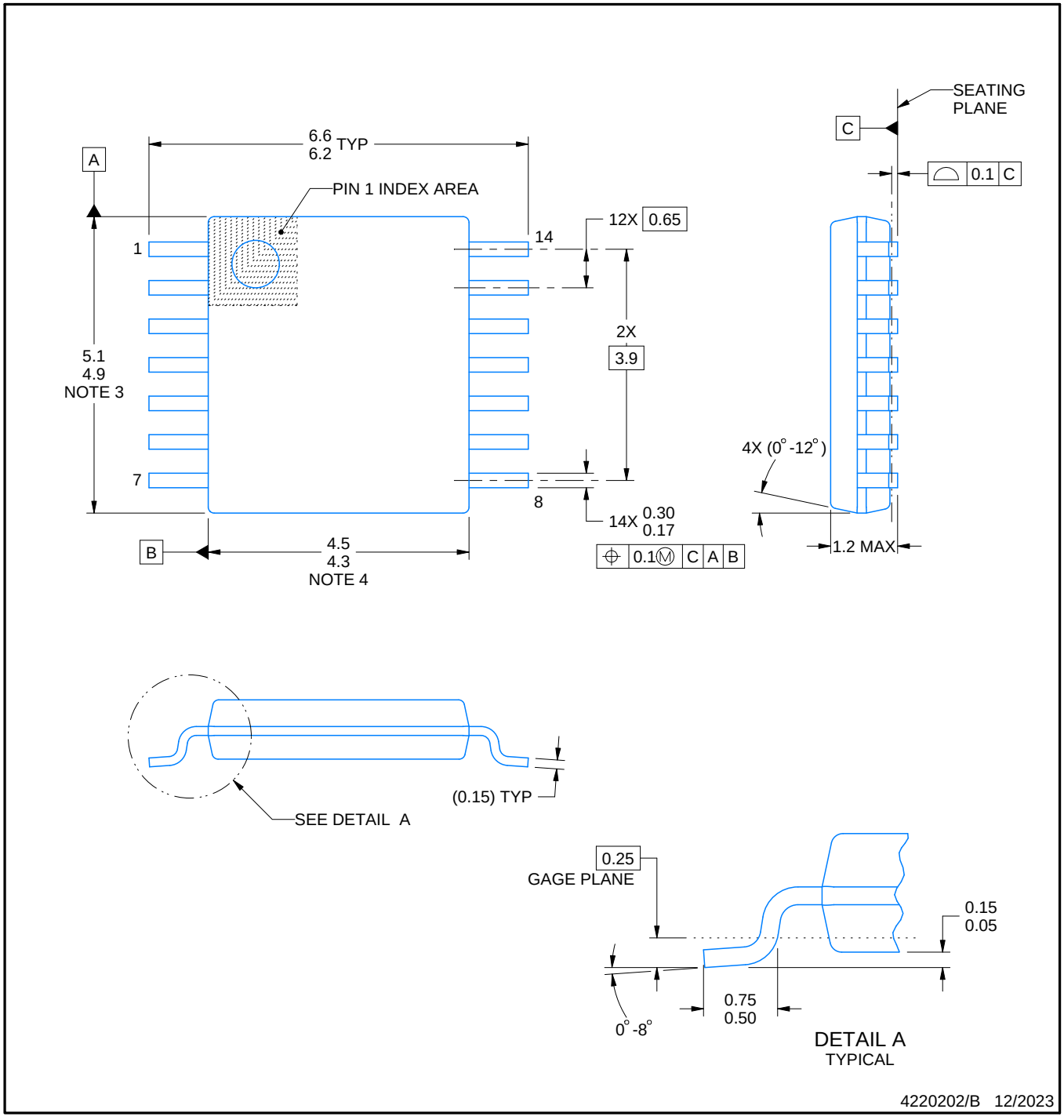
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS72QDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCS72QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0014A

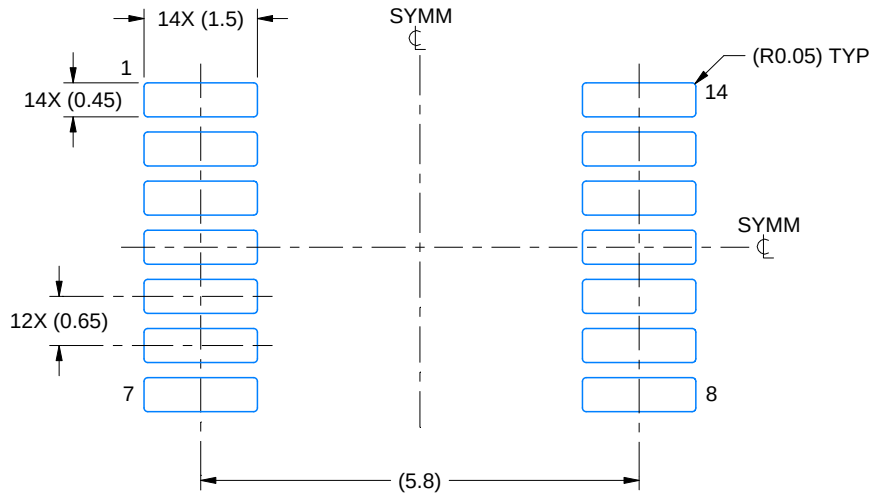
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

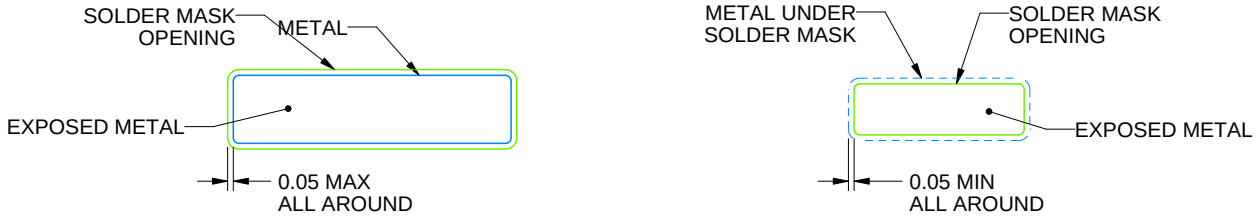


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

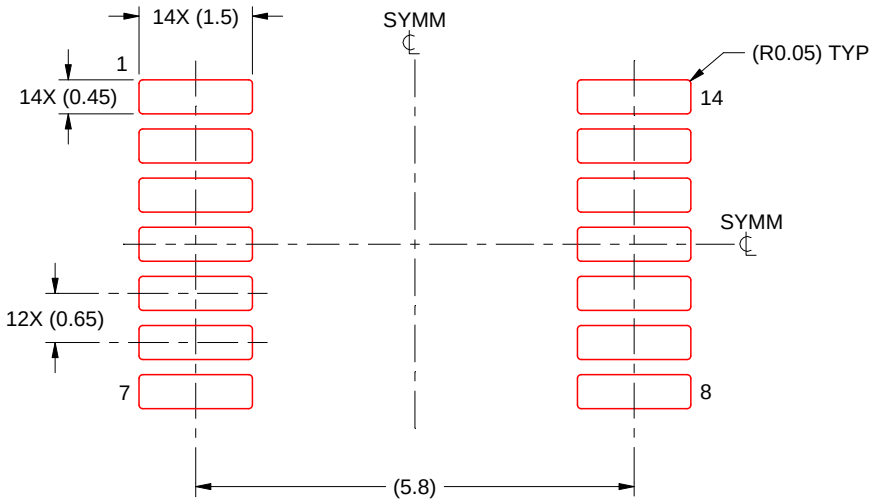


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

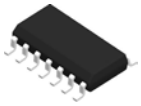


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

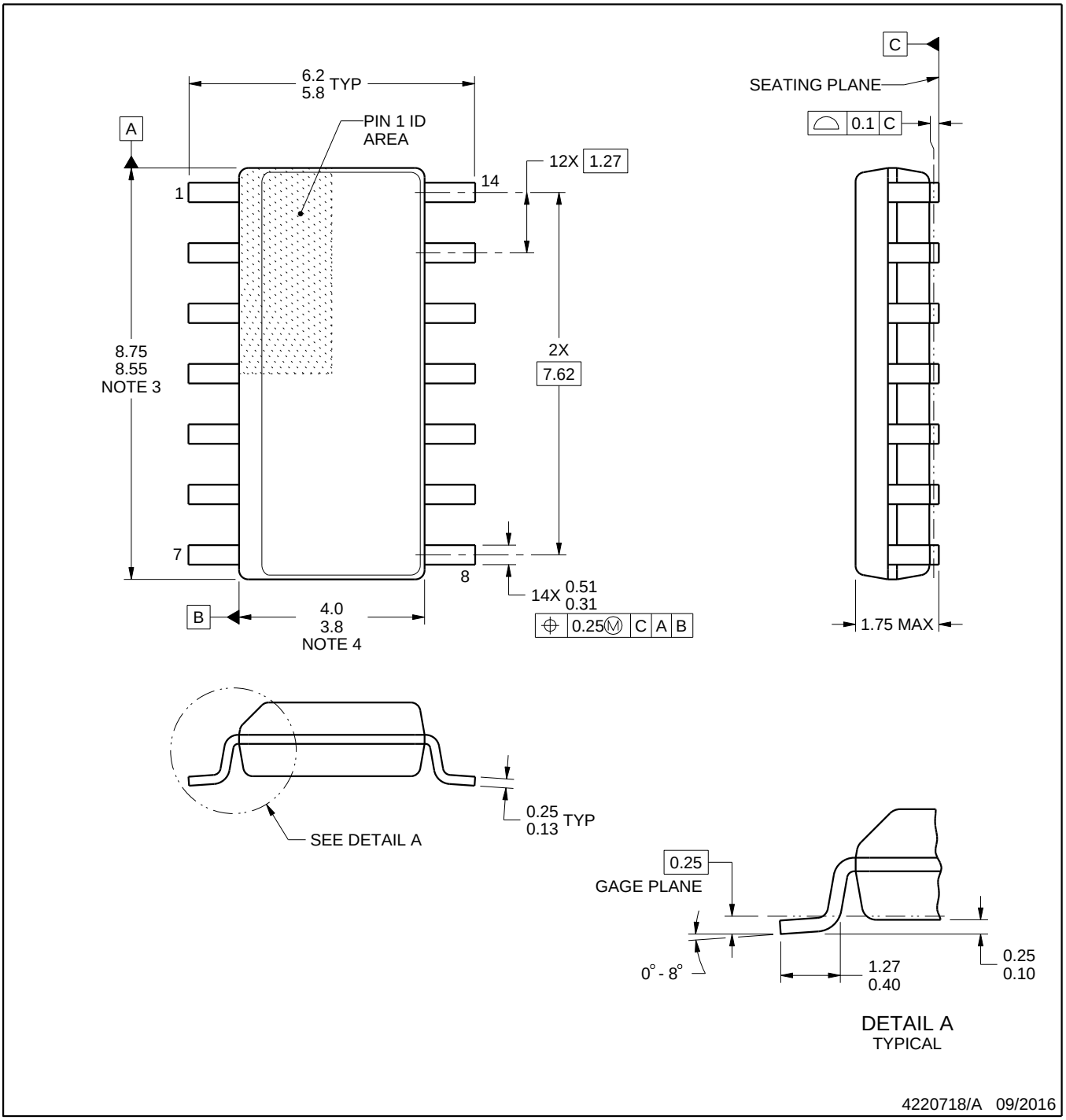


PACKAGE OUTLINE

D0014A

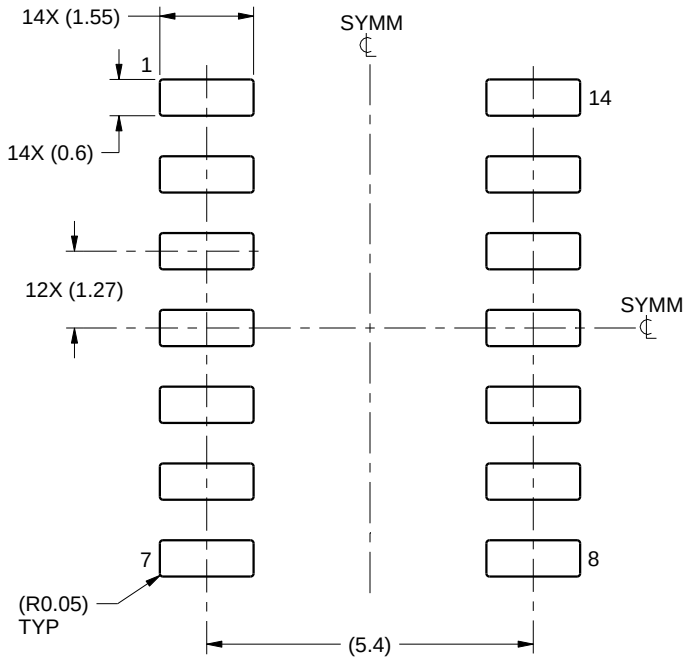
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

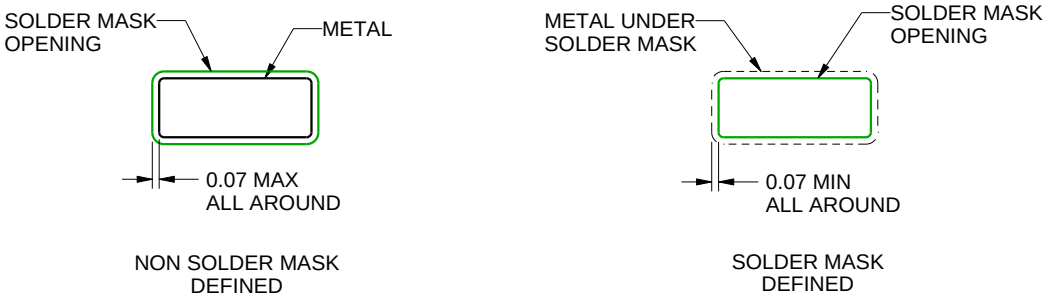


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

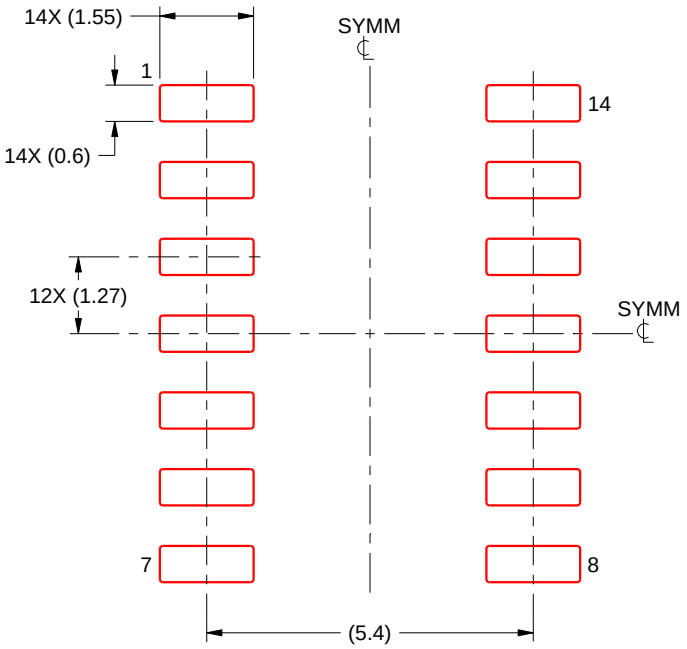
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265