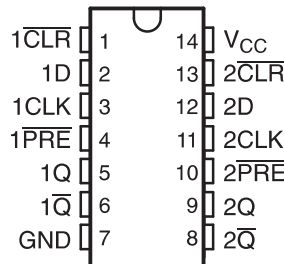


FEATURES

- **Controlled Baseline**
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** ⁽¹⁾
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive up to 10 LSTTL Loads**
- **Low Power Consumption, 80 μ A Max I_{CC}**
- **Typical $t_{pd} = 15$ ns**
- **± 4 mA Output Drive at 5 V**
- **Low Input Current of 1 mA Max**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**D OR PW PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

The SN74HC74 device contains two independent D-type positive edge triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ODERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Reel of 2500	SN74HC74MDREP	HC74MEP
	TSSOP – PW	Reel of 2000	SN74HC74MPWREP	HC74MEP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

- (1) This configuration is nonstable; that is, it does not persist when \overline{PRE} or \overline{CLR} returns to its inactive (high) level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCLS710-MARCH 2008



ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		I _{OH} = –4 mA	4.5 V	3.98	4.3		3.7		
		I _{OH} = –5.2 mA	6 V	5.48	5.8		5.2		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			4		80	µA
C _i			2 V to 6 V		3	10		10	pF

TIMING REQUIREMENTS

			V _{CC}	T _A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f _{clock}	Clock frequency		2 V	6		4.2		MHz
			4.5 V	31		21		
			6 V	0	36	0	25	
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		25		
	CLK high or low	2 V	80		120			
		4.5 V	16		24			
		6 V	14		20			
t _{su}	Setup time before CLK↑	Data	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		25		
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2 V	25		40			
		4.5 V	5		8			
		6 V	4		7			
t _h	Hold time, data after CLK↑		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

SN74HC74-EP

DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET

SCLS710–MARCH 2008

SWITCHING CHARACTERISTICS

over operating free-air temperature range $C_L = 50$ pF, (unless otherwise noted)

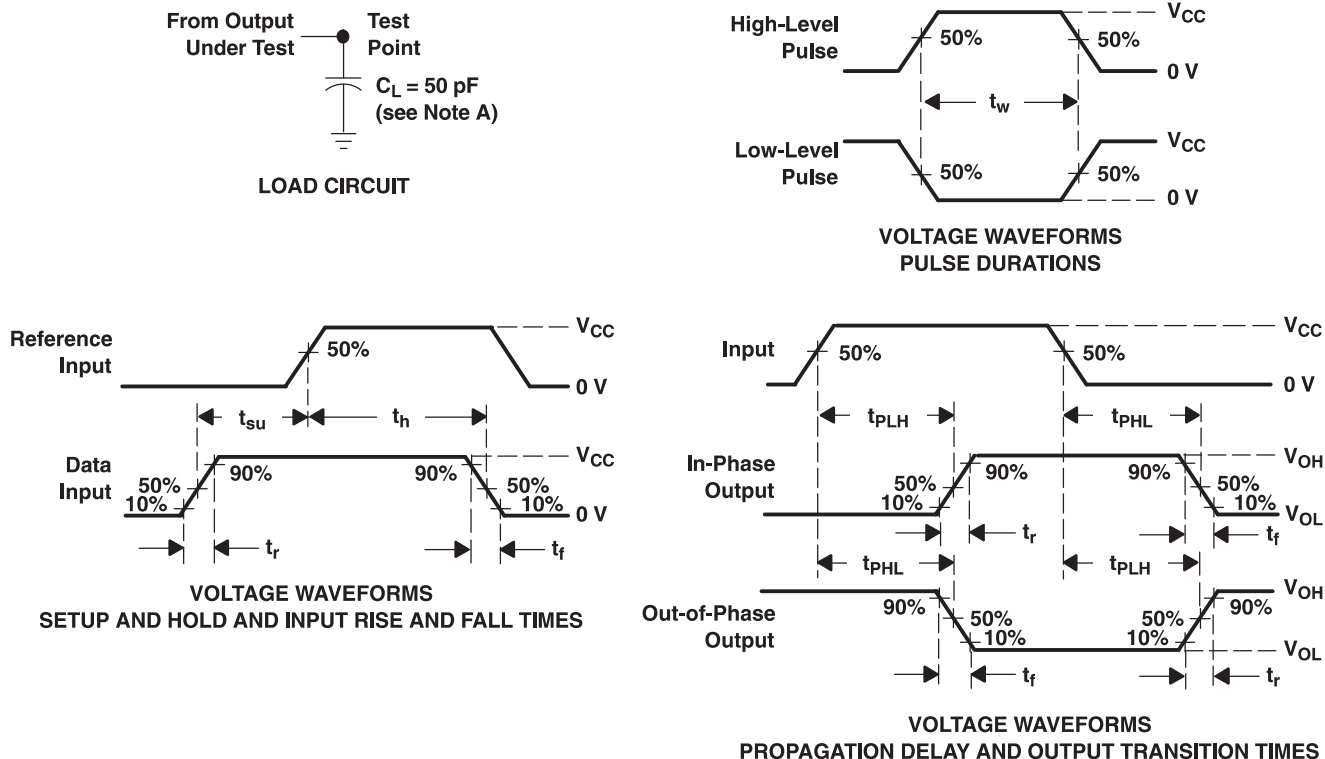
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			2 V	6	10		4.2		MHz
			4.5 V	31	50		21		
			6 V	36	60		25		
t_{pd}	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	2 V		70	230		345	ns
			4.5 V		20	46		69	
			6 V		15	39		59	
	CLK	Q or \overline{Q}	2 V		70	175		250	
			4.5 V		20	35		50	
			6 V		15	30		42	
t_t		Q or \overline{Q}	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC74MPWREP	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74MEP
SN74HC74MPWREP.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74MEP
V62/08613-01XE	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74MEP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74HC74-EP :

- Catalog : [SN74HC74](#)

- Automotive : [SN74HC74-Q1](#)

- Military : [SN54HC74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC74MPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC74MPWREP	TSSOP	PW	14	2000	353.0	353.0	32.0

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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