

SNx4HC682 8-Bit Magnitude Comparators

1 Features

- Wide operating voltage range of 2 V to 6 V
- High-current outputs drive up to 10 LSTTL loads
- Typical $t_{pd} = 22$ ns
- ± 4 -mA output drive at 5 V
- Compare two 8-bit words
- 100-k Ω pullup resistors are on the Q inputs

2 Description

These magnitude comparators perform comparisons of two 8-bit binary or BCD words. The 'HC682 devices feature 100-k Ω pullup termination resistors on the Q inputs for analog or switch data.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74HC682DW	SOIC (20)	12.8 mm × 7.50 mm
SN74HC682N	PDIP (20)	25.40 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

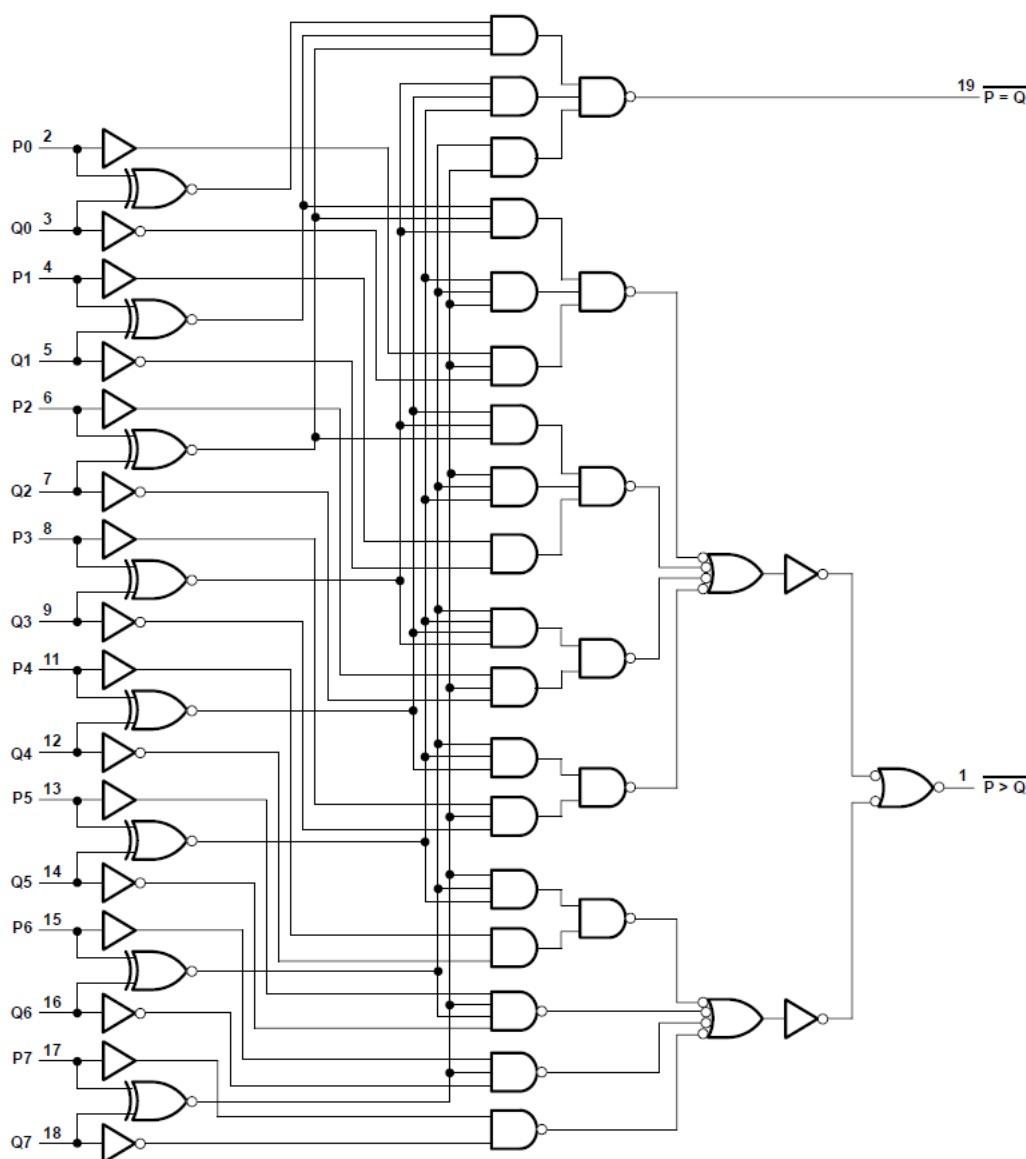


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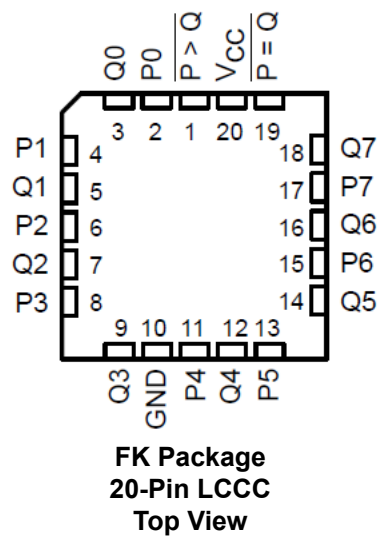
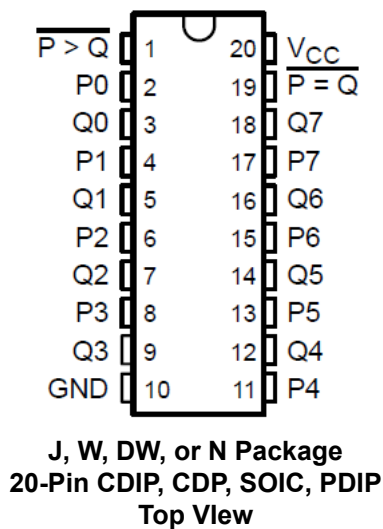
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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2003) to Revision E (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

4 Pin Configuration and Functions



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		–0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HC682 ⁽²⁾			SN74HC682			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5			0.5	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 6 V			1.8			1.8	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V			1000			1000	ns
		V _{CC} = 4.5 V			500			500	
		V _{CC} = 6 V			400			400	
T _A	Operating free-air temperature		–55		125	–40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) SN54HC682 is in product preview.

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	58	69	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC682 ⁽¹⁾		SN74HC682		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I _{IH}	V _I = V _{CC}		6 V		0.1	100		1000		1000	nA
I _{IL}	V _I = 0	Q inputs	6 V		–50	–90		–160		–140	µA
		All other inputs	6 V		–0.1	–100		–1000		–1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V		480	700		1300		1100	µA
C _i			2 V to 6 V		3	10		10		10	pF

(1) SN54HC682 is in product preview.

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC682 ⁽¹⁾		SN74HC682		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	P or Q	Any	2 V		130	275		413		344	ns
			4.5 V		26	55		88		69	
			6 V		22	47		70		58	
t _t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

(1) SN54HC682 is in product preview.

5.6 Operating Characteristics

T_A = 25°C

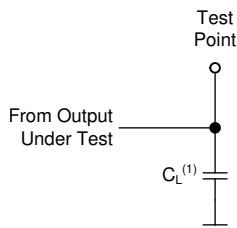
PARAMETER		TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	40	pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

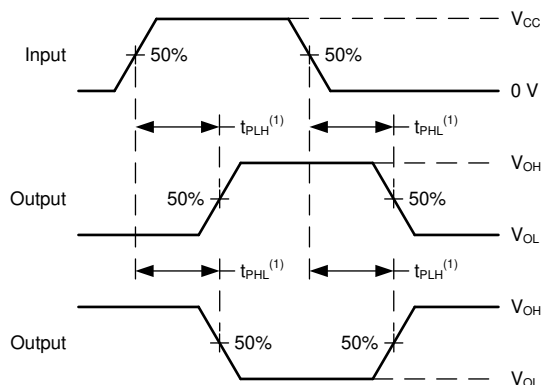
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



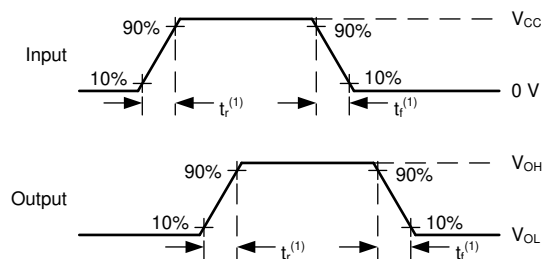
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

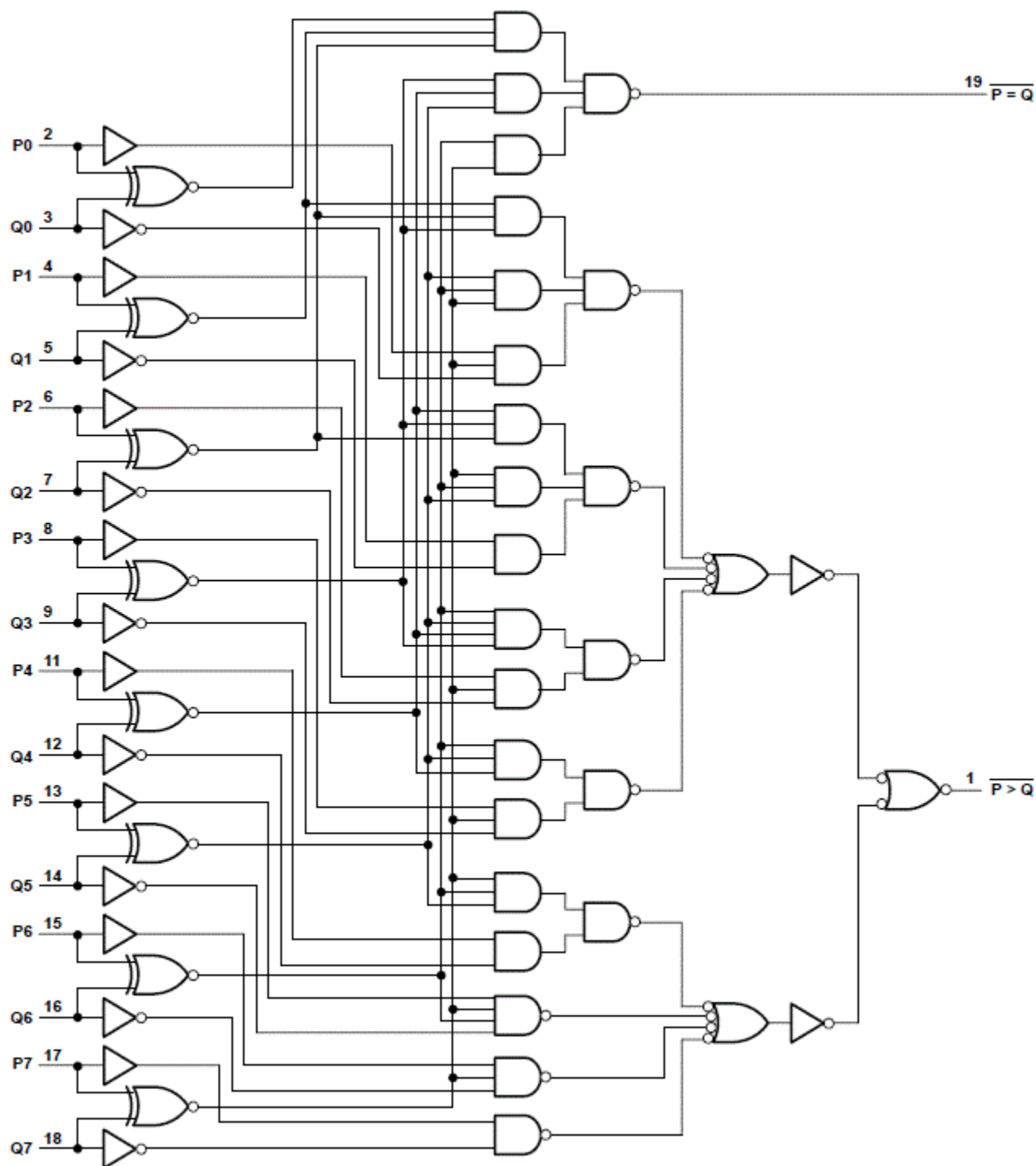
Figure 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

7 Detailed Description

7.1 Overview

These magnitude comparators perform comparisons of two 8-bit binary or BCD words. The 'HC682 devices feature 100-k Ω pullup termination resistors on the Q inputs for analog or switch data.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table⁽¹⁾

DATA INPUTS P, Q	OUTPUTS	
	$P = Q$	$P > Q$
$P = Q$	L	H
$P > Q$	H	L
$P < Q$	H	H

- (1) The $\overline{P} < \overline{Q}$ function can be generated by applying $\overline{P} = \overline{Q}$ and $\overline{P} > \overline{Q}$ to a 2-input NAND gate.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC682DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	HC682
SN74HC682DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC682
SN74HC682DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC682
SN74HC682N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC682N
SN74HC682N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC682N
SN74HC682N.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC682N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC682DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC682DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HC682N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC682N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC682N.B	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



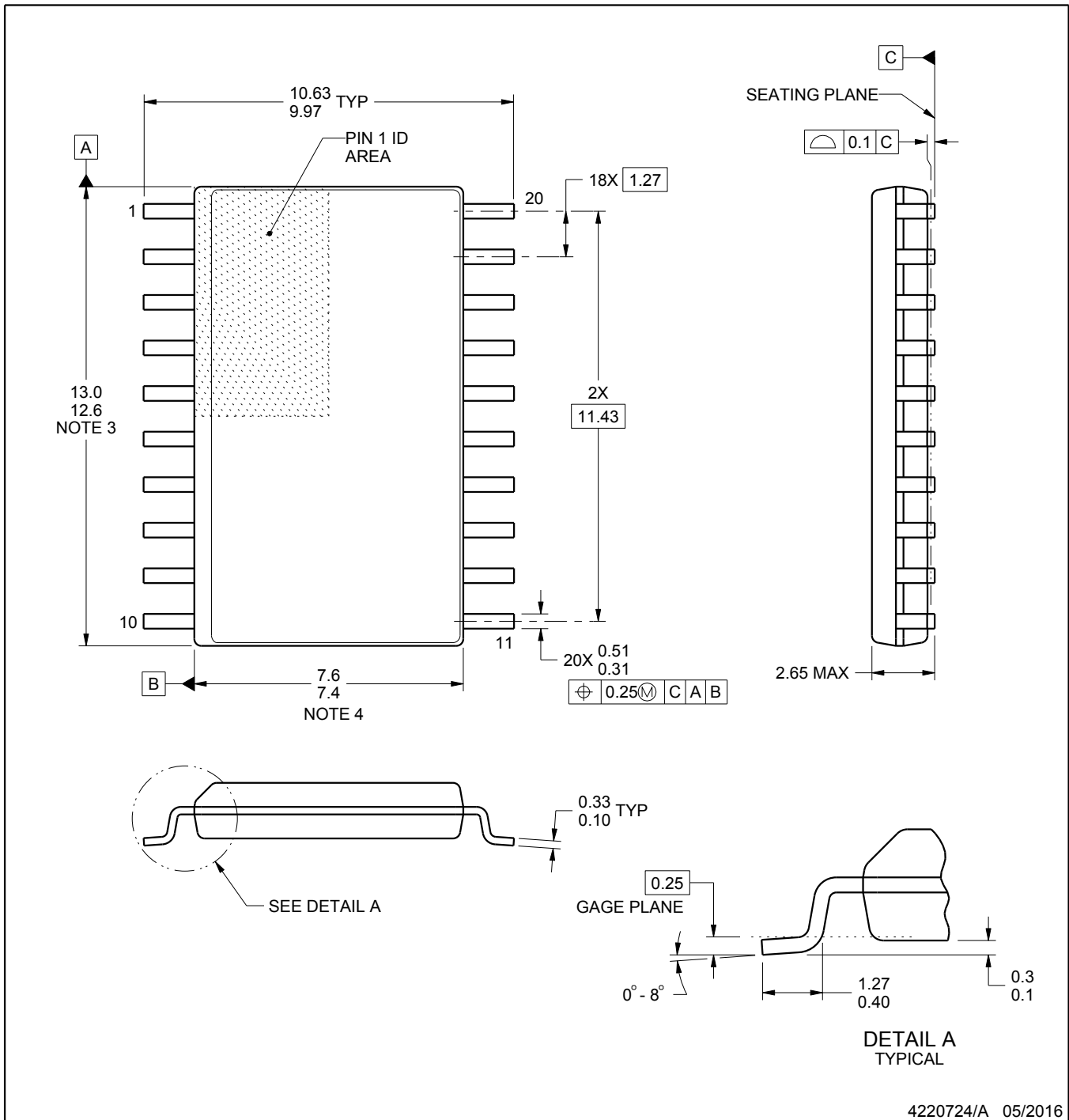
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



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NOTES:

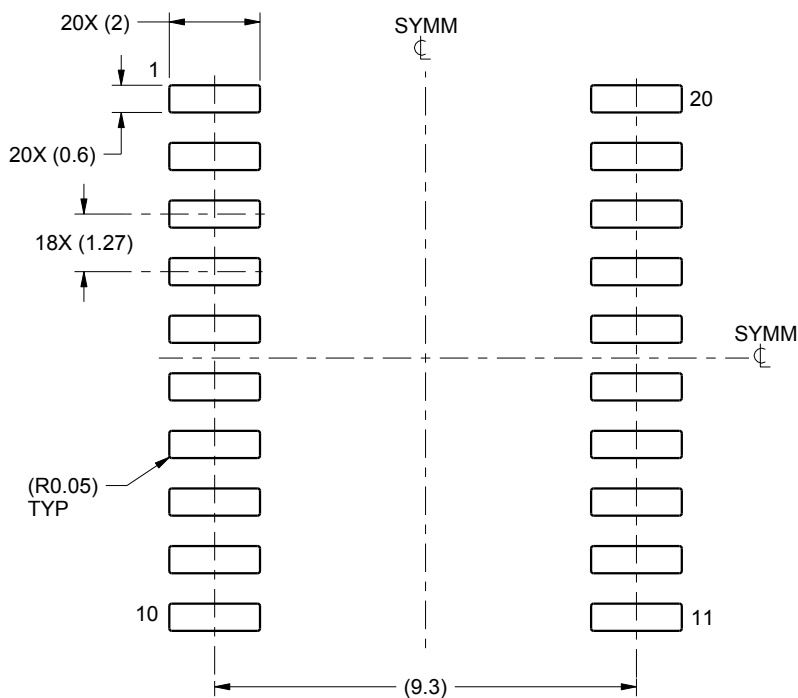
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

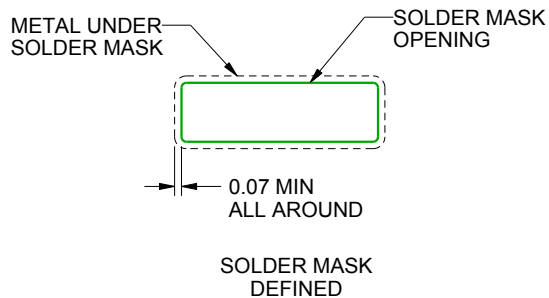
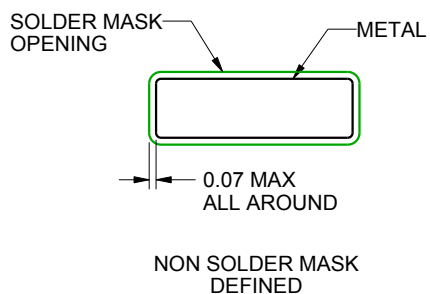
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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