

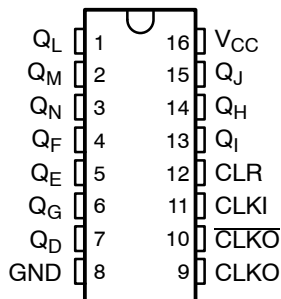
SN74HC4060-Q1

14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

SCLS726 – DECEMBER 2011

- Qualified for Automotive Applications
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Allow Design of Either RC- or Crystal-Oscillator Circuits

SN74HC4060-Q1 . . . D PACKAGE
(TOP VIEW)



description/ordering information

The 'HC4060-Q1 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock (CLKI) input increments the counter. A high level at the clear (CLR) input disables the oscillator (\overline{CLKO} goes high and CLKO goes low) and resets the counter to zero (all Q outputs low).

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74HC4060QDRQ1	HC4060Q

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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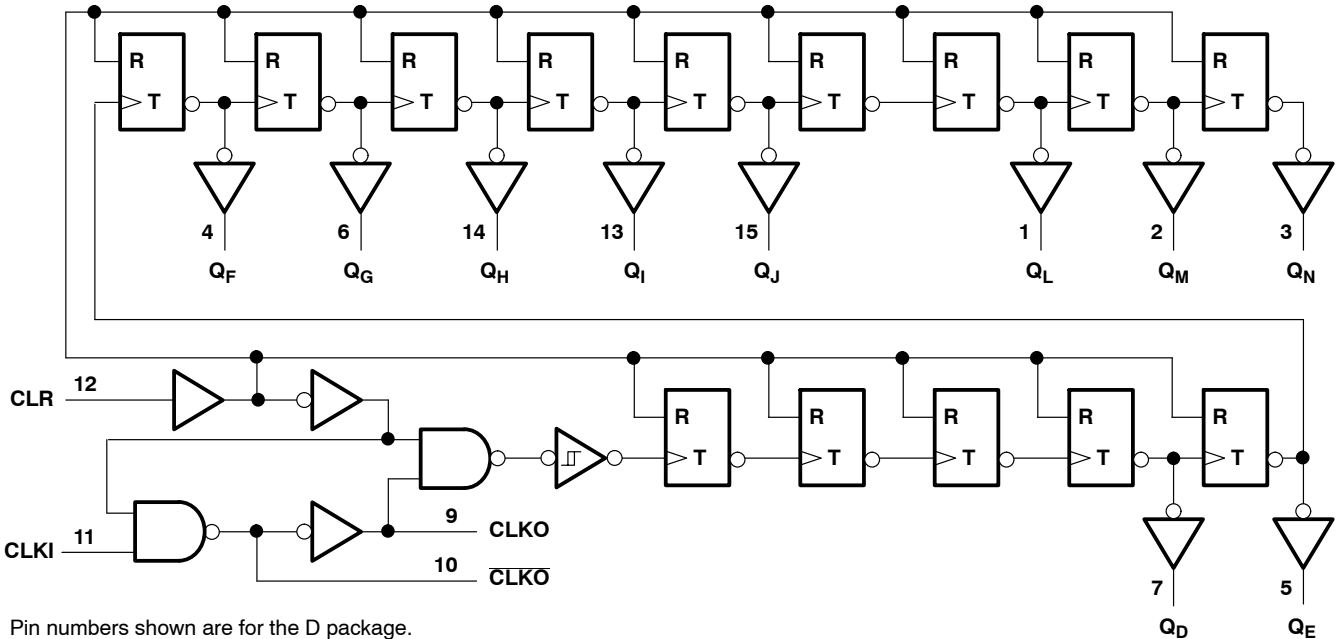
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FUNCTION TABLE
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

Logic diagram (positive logic)



Pin numbers shown are for the D package.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating: Human Body Model (HBM)	2000 V
Charged Device Model (CDM)	1000 V
Machine Model (MM)	200 V

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 6\text{ V}$	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 6\text{ V}$			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$			1000	ns
		$V_{CC} = 4.5\text{ V}$			500	
		$V_{CC} = 6\text{ V}$			400	
T_A	Operating free-air temperature		-40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			'HC4060-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	All outputs	$V_I = V_{IH}\text{ or }V_{IL},$ $I_{OH} = -20\text{ }\mu\text{A}$	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
	Q outputs	$V_I = V_{IH}\text{ or }V_{IL},$ $I_{OH} = -4\text{ mA}$ $I_{OH} = -5.2\text{ mA}$	4.5 V	3.98	4.3		3.7		
			6 V	5.48	5.8		5.2		
V_{OL}	All outputs	$V_I = V_{IH}\text{ or }V_{IL},$ $I_{OL} = 20\text{ }\mu\text{A}$	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
	Q outputs	$V_I = V_{IH}\text{ or }V_{IL},$ $I_{OL} = 4\text{ mA}$ $I_{OL} = 5.2\text{ mA}$	4.5 V		0.17	0.26		0.4	
			6 V		0.15	0.26		0.4	
I_I		$V_I = V_{CC}\text{ or }0$	6 V		± 0.1	± 100		± 1000	nA
I_{CC}		$V_I = V_{CC}\text{ or }0,$ $I_O = 0$	6 V			8		160	μA
C_i			2 V to 6 V		3	10		10	pF



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Timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		'HC4060-Q1		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	5.5		3.7		MHz
		4.5 V	28		19		
		6 V	33		22		
t _w	Pulse duration	CLKI high or low	2 V	90	135		ns
			4.5 V	18	27		
			6 V	15	23		
	CLR high	2 V	90	135			
		4.5 V	18	27			
		6 V	15	23			
t _{su}	Setup time, CLR inactive before CLKI↓	2 V	160	240		ns	
		4.5 V	32	48			
		6 V	27	41			

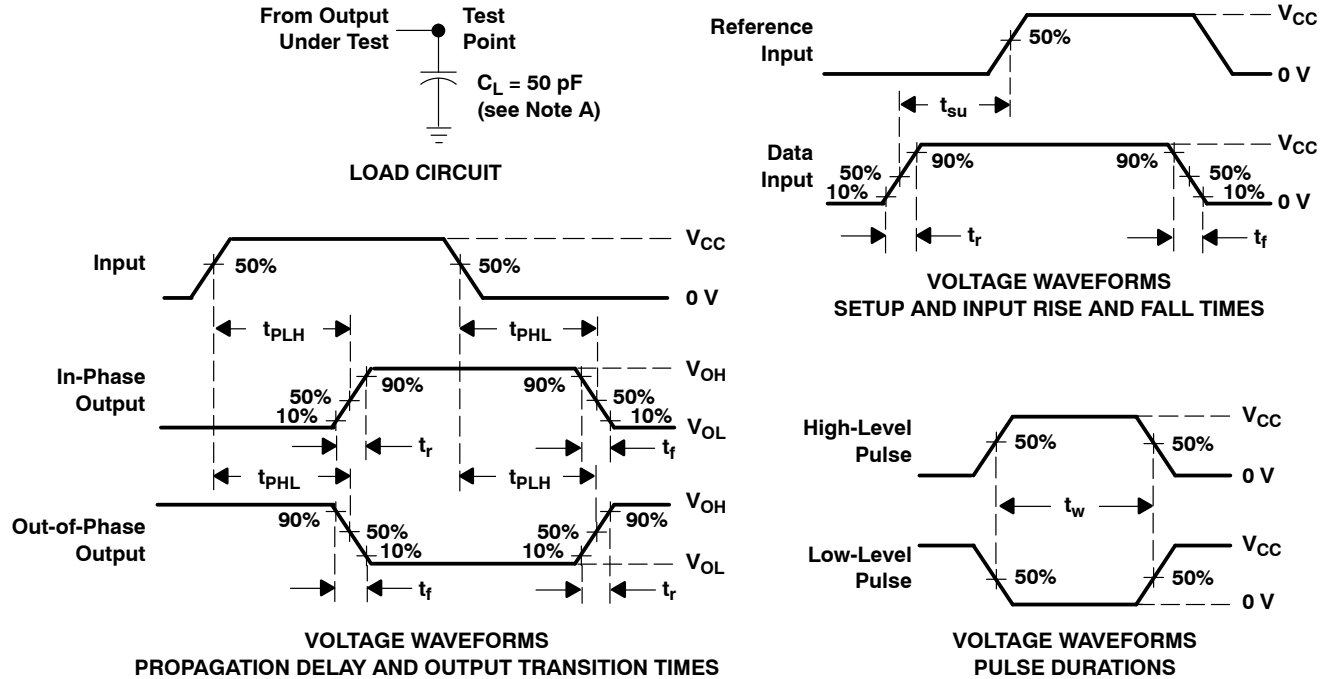
Switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			'HC4060-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
f _{max}			2 V	5.5	10		3.7		MHz
			4.5 V	28	45		19		
			6 V	33	53		22		
t _{pd}	CLKI	Q _D	2 V		240	490		735	ns
			4.5 V		58	98		147	
			6 V		42	83		125	
t _{PHL}	CLR	Any Q	2 V		66	140		210	ns
			4.5 V		18	28		42	
			6 V		14	24		36	
t _t		Any	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	30		19	

Operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	88	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74HC4060-Q1

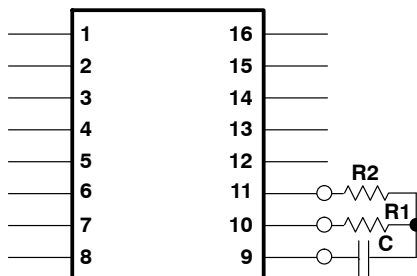
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CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE 'HC4060-Q1 DEVICE

The 'HC4060-Q1 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405 R2}{R1 + R2} + 0.693\right)}$$

If $R2 \gg R1$ (i.e., $R2 = 10R1$), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC4060QDRQ1	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4060Q
SN74HC4060QDRQ1.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4060Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74HC4060-Q1 :

- Catalog : [SN74HC4060](#)

- Military : [SN54HC4060](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4060QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4060QDRQ1	SOIC	D	16	2500	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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