SCLS121D - DECEMBER 1982 - REVISED OCTOBER 2003

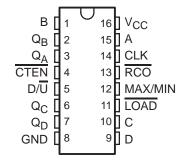
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 13 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Single Down/Up Count-Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable With Load Control

description/ordering information

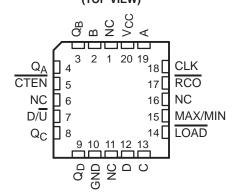
The 'HC191 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low- to high-level transition of the clock (CLK) input if the count-enable (\overline{CTEN}) input is low. A high at \overline{CTEN} inhibits counting. The direction of the count is determined by the level of the down/up (D/ \overline{U}) input. When D/ \overline{U} is low, the counter counts up, and when D/ \overline{U} is high, it counts down.

SN54HC191 . . . J OR W PACKAGE SN74HC191 . . . D, N, OR NS PACKAGE (TOP VIEW)



SN54HC191 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACKAG	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube of 25	SN74HC191N	SN74HC191N		
		Tube of 40	SN74HC191D			
-40°C to 85°C	SOIC - D	Reel of 2500	SN74HC191DR	HC191		
		Reel of 250	SN74HC191DT]		
	SOP - NS	Reel of 2000	SN74HC191NSR	HC191		
	CDIP – J	Tube of 25	SNJ54HC191J	SNJ54HC191J		
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC191W	SNJ54HC191W		
	LCCC – FK	Tube of 55	SNJ54HC191FK	SNJ54HC191FK		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information (continued)

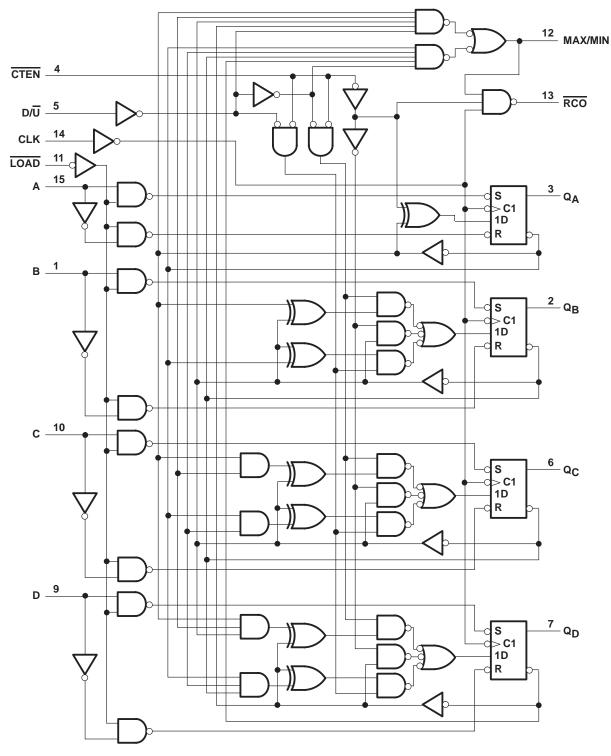
These counters feature a fully independent clock circuit. Change at the control ($\overline{\text{CTEN}}$ and D/\overline{U}) inputs that modifies the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, each of the outputs can be preset to either level by placing a low on the load (LOAD) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of CLK. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock (\overline{RCO}) and maximum/minimum (MAX/MIN) count. MAX/MIN produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down, or maximum (9 or 15) counting up. \overline{RCO} produces a low-level output pulse under those same conditions, but only while CLK is low. The counters can be cascaded easily by feeding \overline{RCO} to \overline{CTEN} of the succeeding counter if parallel clocking is used, or to CLK if parallel enabling is used. MAX/MIN can be used to accomplish look ahead for high-speed operation.



logic diagram (positive logic)

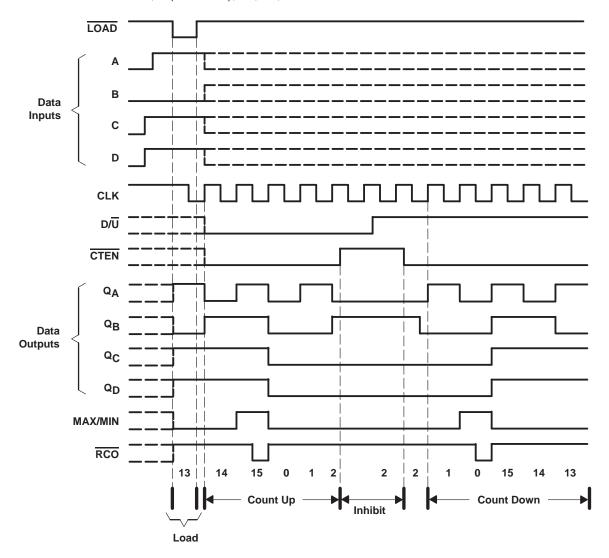


Pin numbers shown are for the D, J, N, NS, and W packages.

typical load, count, and inhibit sequence

The following sequence is illustrated below:

- 1. Load (preset) to binary 13
- 2. Count up to 14, 15 (maximum), 0, 1, and 2
- 3. Inhibit
- 4. Count down to 1, 0 (minimum), 15, 14, and 13



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (9			
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_O$			
Continuous output current, I_O ($V_O = 0$ to V_{CO}			
Continuous current through V _{CC} or GND			
Package thermal impedance, θ _{JA} (see Note 2	2): D package		73°C/W
	N package		67°C/W
	NS package		64°C/W
Storage temperature range, T _{sto}			o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SI	N54HC19	1	SN	174HC19	1	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
VIH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V _{CC} = 2 V			0.5			0.5	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		VCC = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V			1000			1000	
Δt/Δv‡	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns
		V _{CC} = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[‡] If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEOT 0.0	NIDITIONO	vcc	Т	A = 25°C	;	SN54H	IC191	SN74H	C191	LINUT
PARAMETER	TEST CC	EST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
Voн	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		$I_{OL} = 20 \mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1	
VoL	VI = VIH or VIL		6 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V	·	±0.1	±100		±1000		±1000	nA
ICC	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
Ci		_	2 V to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				T _A = 2	25°C	SN54H	IC191	SN74H	IC191	
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		4.2		2.8		3.3	
fclock	Clock frequency		4.5 V		21		14		17	MHz
			6 V		24		16		19	
			2 V	120		180		150		
		LOAD low	4.5 V	24		36		30		
	Dulas dunation		6 V	21		31		26		
t _W	Pulse duration		2 V	120		180		150		ns
		CLK high or low	4.5 V	24		36		30		
			6 V	21		31		26		
			2 V	150		230		188		
		Data before LOAD↑	4.5 V	30		46		38		
			6 V	25		38		32		
			2 V	205		306		255		
		CTEN before CLK↑	4.5 V	41		61		51		
			6 V	35		53		44		
t _{su}	Setup time		2 V	205		306		255		ns
		D/U before CLK↑	4.5 V	41		61		51		
			6 V	35		53		44		
			2 V	150		225		190		
		LOAD inactive before CLK↑	4.5 V	30		45		38		
			6 V	25		38		32		
			2 V	5		5		5		
		Data after LOAD↑	4.5 V	5		5		5		
			6 V	5		5		5		
			2 V	5		5		5		
th	Hold time	CTEN after CLK↑	4.5 V	5		5		5		ns
			6 V	5		5		5		
			2 V	5		5		5		
		D/U after CLK↑	4.5 V	5		5		5		
			6 V	5		5		5		

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

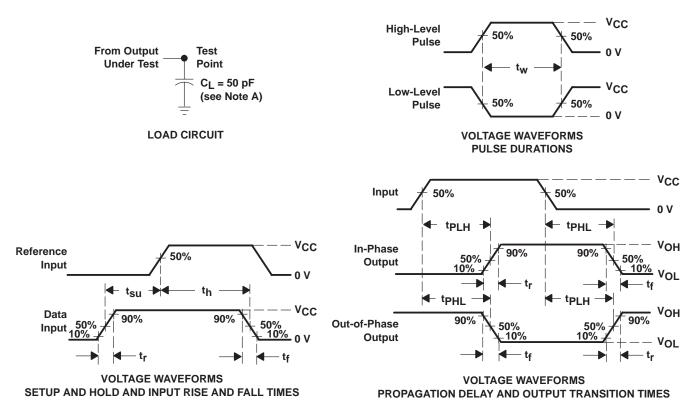
	FROM	то		T,	Δ = 25°C	;	SN54H	IC191	SN74H	C191	
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	4.2	8		2.8		3.3		
fmax			4.5 V	21	42		14		17		MHz
			6 V	24	48		16		19		
			2 V		130	264		396		330	
	LOAD	Any Q	4.5 V		40	53		79		66	
			6 V		33	45		67		56	
			2 V		135	240		360		300	
	A, B, C, or D	Q_A , Q_B , Q_C , or Q_D	4.5 V		36	48		72		60	
		or ap	6 V		30	41		61		51	
			2 V		58	120		180		150	
		RCO	4.5 V		17	24		36		30	
			6 V		14	21		31		26	
			2 V		107	192		288		240	
	CLK	Any Q	4.5 V		31	38		58		48	
			6 V		26	32		49		41	
^t pd			2 V		123	252		378		315	ns
		MAX/MIN	4.5 V		39	50		76		63	
			6 V		32	43		65		54	
			2 V		102	228		342		285	
		RCO	4.5 V		29	46		68		57	
	D/ U		6 V		24	38		59		49	
	D/U		2 V		86	192		288		240	
		MAX/MIN	4.5 V		24	38		58		48	
			6 V		20	32		49		41	
			2 V		50	132		198		165	
	CTEN	RCO	4.5 V		15	26		40		33	
			6 V		13	23		34		28	
			2 V		38	75		110		95	
t _t		Any	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	50	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 6$ ns, $t_f = 6$ ns.
- C. For clock inputs, $f_{\mbox{max}}$ is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-86891012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86891012A SNJ54HC 191FK
5962-8689101EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689101EA SNJ54HC191J
SN54HC191J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC191J
SN54HC191J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC191J
SN74HC191D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC191
SN74HC191DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC191
SN74HC191DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC191
SN74HC191DT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC191
SN74HC191N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC191N
SN74HC191N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC191N
SN74HC191NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC191
SN74HC191NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC191
SN74HC191NSR.B	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC191
SNJ54HC191FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86891012A SNJ54HC 191FK
SNJ54HC191FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86891012A SNJ54HC 191FK
SNJ54HC191J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689101EA SNJ54HC191J
SNJ54HC191J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8689101EA SNJ54HC191J

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54HC191, SN74HC191:

Catalog: SN74HC191

Military: SN54HC191

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC191DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC191NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC191DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC191NSR	SOP	NS	16	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-86891012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC191N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC191N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC191N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC191N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC191FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC191FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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