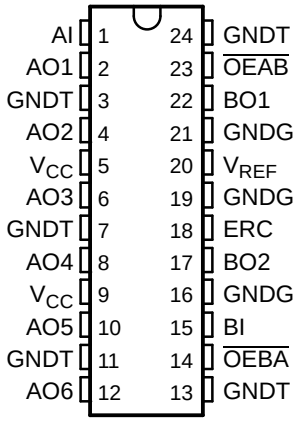
SN74GTLP817
GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E – OCTOBER 1999 – REVISED APRIL 2005

FEATURES

- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTLP 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTLP817 is a medium-drive fanout driver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, and OEC™ circuitry. The improved GTLP OEC circuitry minimizes bus settling time and has been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω. BO1 and BO2 can be tied together to drive an equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP817 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

GNDT is the TTL output ground, while GNDG is the GTLP output ground, and both may be separated from each other for a quieter device.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load. ERC automatically is selected to the same speed as alternate source 1-to-6 fanout drivers that use pin 18 for 3.3-V or 5-V V_{CC}.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP817DW	GTLP817
		Tape and reel	SN74GTLP817DWR	
	TSSOP – PW	Tape and reel	SN74GTLP817PWR	GT817
	TVSOP – DGV	Tape and reel	SN74GTLP817DGVR	GT817

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTLP translation and GTLP-to-LVTTL translation in the same package.

The LVTTL-to-GTLP direction is a 1-to-2 fanout driver with a single output enable ($\overline{OEAB}$).

The GTLP-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable ($\overline{OEBA}$).

Data polarity is inverting for both directions.

FUNCTION TABLES

OUTPUT CONTROL (A TO B)

INPUTS		OUTPUT BOn	MODE
AI	$\overline{OEAB}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

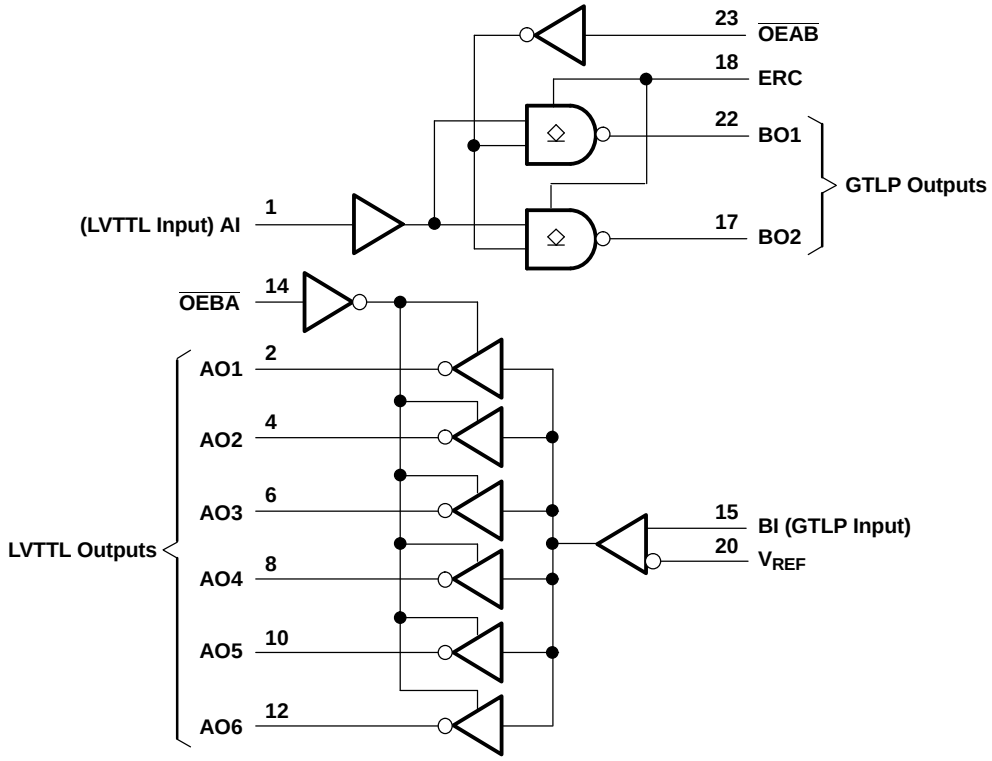
OUTPUT CONTROL (B TO A)

INPUTS		OUTPUT AOn	MODE
BI	$\overline{OEBA}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
$\lvert V_{GNDG} - V_{GNDT} \rvert$	Ground dc voltage difference			0.3	V
V_I	Input voltage range(2)	AI port and control inputs	–0.5	7	V
		BI port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	AO port	–0.5	7	V
		BO port	–0.5	4.6	
I_O	Current into any output in the low state	AO port		24	mA
		BO port		100	
I_O	Current into any A output in the high state(3)			24	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)	DGV package		86	°C/W
		DW package		46	
		PW package		88	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1][2][3][4]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	BI			V_{TT}	V
		AI, $\overline{OE}$		V_{CC}	5.5	
V_{IH}	High-level input voltage	BI	V_{REF} + 0.05			V
		ERC	V_{CC} – 0.6	V_{CC}	5.5	
		AI, $\overline{OE}$	2			
V_{IL}	Low-level input voltage	BI			V_{REF} – 0.05	V
		ERC		GND	0.6	
		AI, $\overline{OE}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–12	mA
I_{OL}	Low-level output current	AO port			12	mA
		BO port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3.15 V	I_{OH} = –100 µA	V_{CC} – 0.2			
			I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2.2			
V_{OL}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 6 mA			0.4	
			I_{OL} = 12 mA			0.5	
	BO port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 40 mA			0.5	
			I_{OL} = 50 mA			0.55	
I_I	BI, AI, $\overline{OE}$, ERC	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±5	µA
I_{OZH}	AO port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	BO port		V_O = 1.5 V			5	
I_{OZL}	AO port	V_{CC} = 3.45 V	V_O = GND			–10	µA
	BO port		V_O = 5.5 V			–5	
I_{CC}	AO or BO port	V_{CC} = 3.45 V, I_O = 0, V_I (AI or control input) = V_{CC} or GND, V_I (BI input) = V_{TT} or GND	Outputs high			10	mA
			Outputs low			10	
			Outputs disabled			10	
ΔI_{CC}(2)	AI, $\overline{OE}$	V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1	mA
C_i	AI, $\overline{OE}$, ERC	V_I = V_{CC} or 0			4	4.4	pF
	BI	V_I = V_{TT} or 0			3.5	3.9	
C_o	AO port	V_O = V_{CC} or 0			4	4.5	pF
	BO port	V_O = V_{TT} or 0			5	5.4	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified LVTTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

Hot-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA

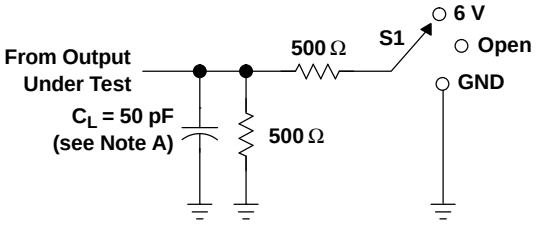
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	MIN	TYP(2)	MAX	UNIT
t_{PLH}	AI	BO	Slow	3		6	ns
t_{PHL}				1.8		4.7	
t_{PLH}	AI	BO	Fast	2		5	ns
t_{PHL}				1.5		4.2	
t_{en}	$\overline{OEAB}$	BO	Slow	3		6.1	ns
t_{dis}				2		4.7	
t_{en}	$\overline{OEAB}$	BO	Fast	2.1		6	ns
t_{dis}				1.5		4.7	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.5		ns
			Fast		1.4		
t_f	Fall time, B outputs (80% to 20%)		Slow		1.7		ns
			Fast		1		
t_{PLH}	BI	AO		2.3		6	ns
t_{PHL}				1.9		4.7	
t_{en}	$\overline{OEBA}$	AO		1.1		6.3	ns
t_{dis}				1.2		5	

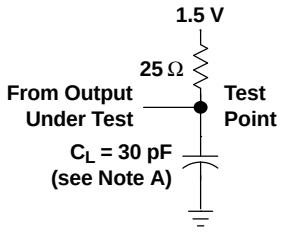
(1) Slow (ERC = V_{CC}) and Fast (ERC = GND)
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

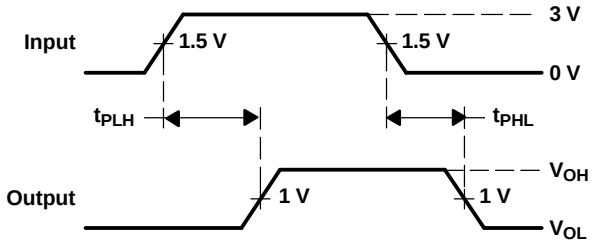


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

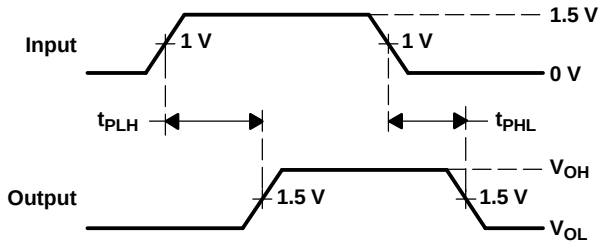
LOAD CIRCUIT FOR AO PORTS



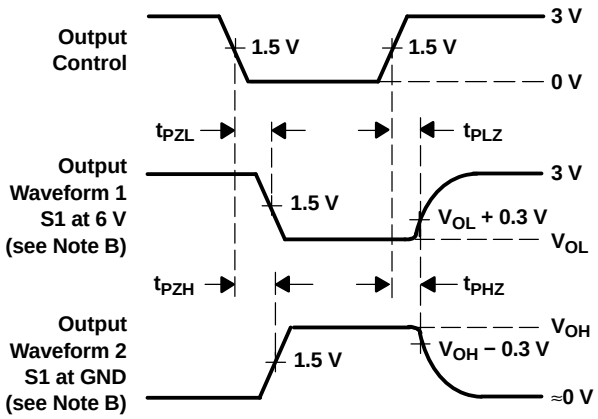
LOAD CIRCUIT FOR BO PORTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to BO port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(BI to AO port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO ports)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

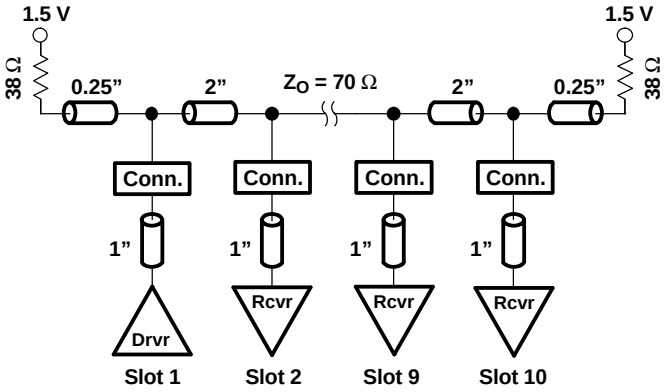


Figure 2. Medium-Drive Test Backplane

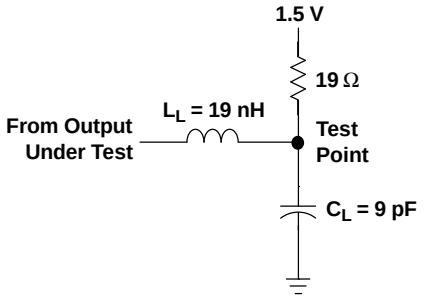


Figure 3. Medium-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	TYP(2)	UNIT
t_{PLH}	AI	BO	Slow	4.4	ns
t_{PHL}				4.4	
t_{PLH}	AI	BO	Fast	3.2	ns
t_{PHL}				3.2	
t_{en}	$\overline{OEAB}$	BO	Slow	4	ns
t_{dis}				4.4	
t_{en}	$\overline{OEAB}$	BO	Fast	2.9	ns
t_{dis}				3.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	1.8	ns
			Fast	1	
t_f	Fall time, B outputs (80% to 20%)		Slow	2	ns
			Fast	1.6	

(1) Slow (ERC = V_{CC}) and Fast (ERC = GND)
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74GTLP817PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GT817
SN74GTLP817PW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GT817

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

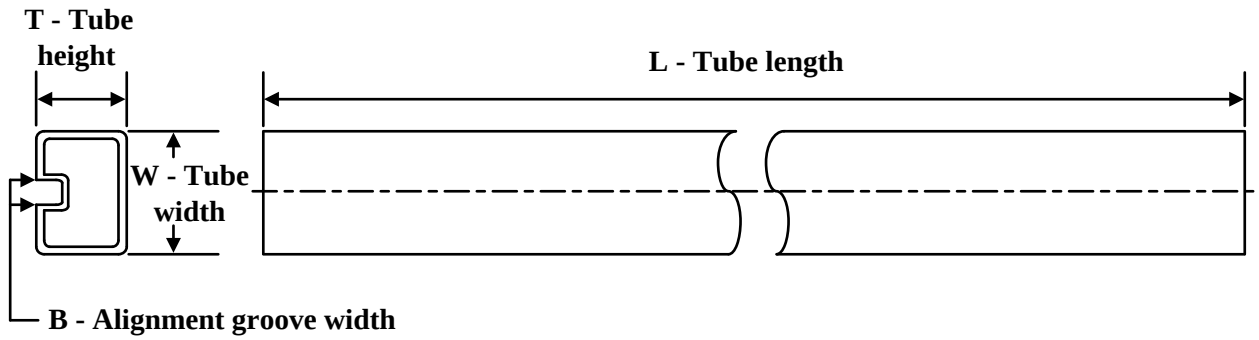
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

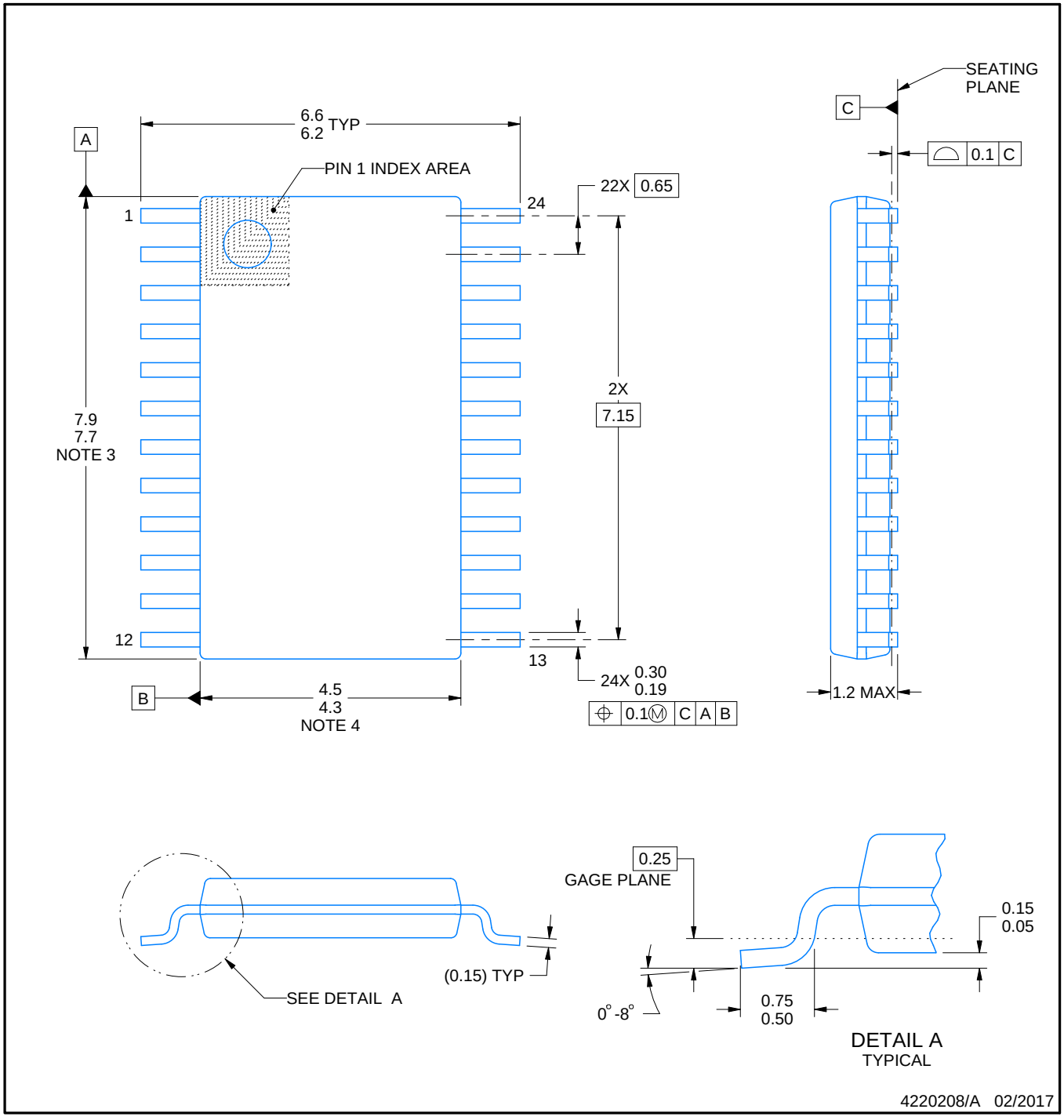
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74GTLP817PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74GTLP817PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

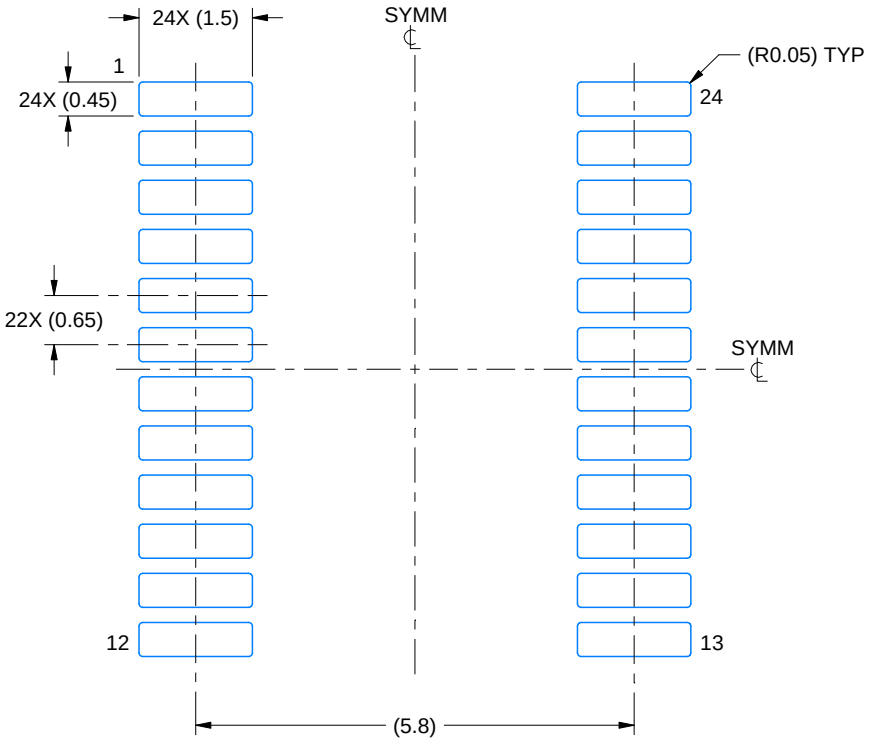
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

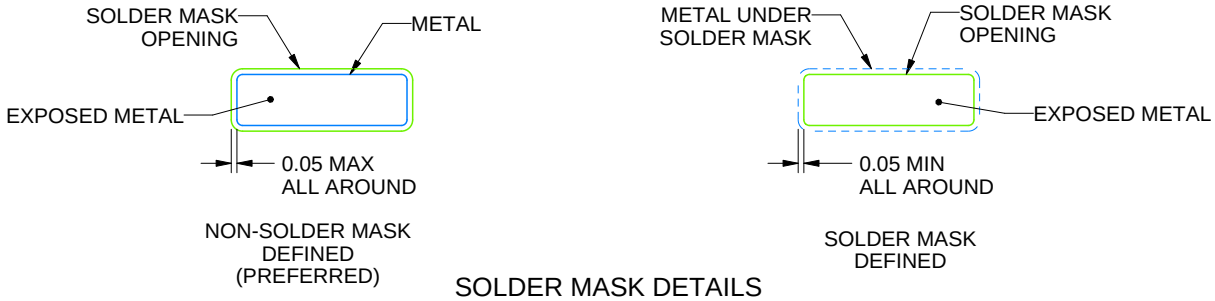


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

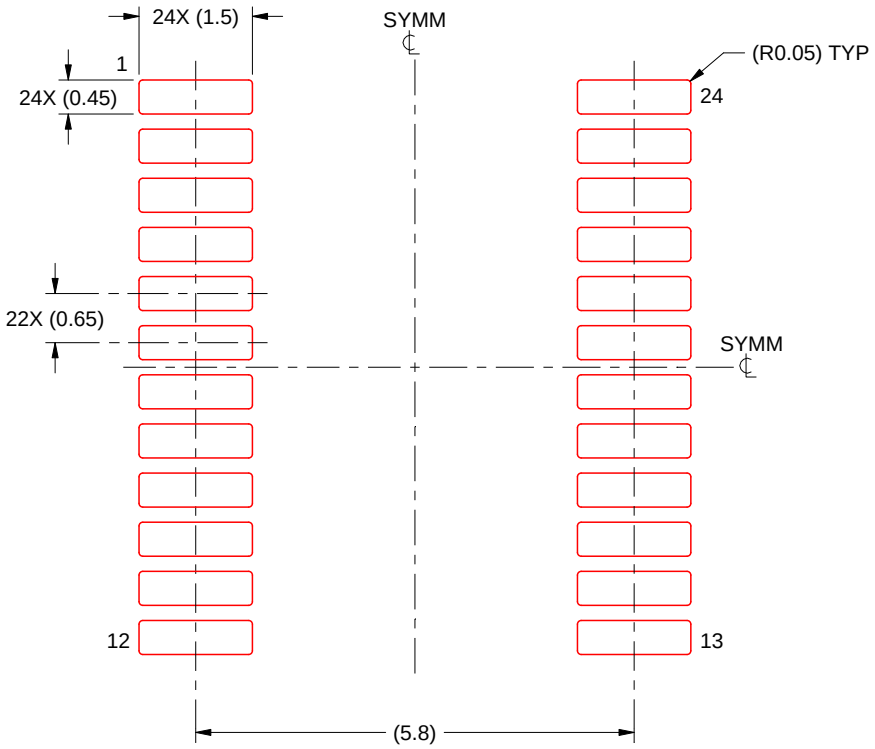


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265