







SN74CBTLV3126

SCDS038L - DECEMBER 1997 - REVISED AUGUST 2022

SN74CBTLV3126 Low-Voltage Quadruple FET Bus Switch

1 Features

- Standard 126-type pinout
- $5-\Omega$ switch connection between two ports
- Rail-to-rail switching on data I/O ports
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II

2 Applications

- Datacenter and enterprise computing
- Broadband fixed line access
- **Building automation**
- Wired networking
- Motor drives

3 Description

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

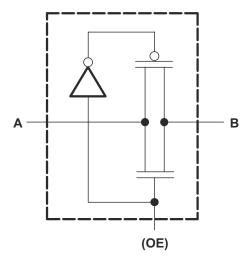
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CBTLV3126 device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Package Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)				
	SOIC (D, 14)	8.65 mm × 3.91 mm				
	TVSOP (DGV, 14)	3.60 mm × 4.40 mm				
SN74CBTLV3126	TSSOP (PW, 14)	5.00 mm × 4.40 mm				
	VQFN (RGY, 14)	4.00 mm × 3.50 mm				
	SSOP (DBQ, 16)	4.90 mm × 3.90 mm				

For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic, Each FET Switch

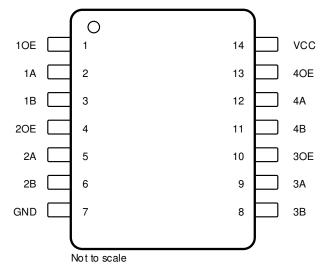


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5 Pin Configuration and Functions



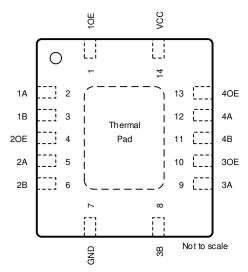


Figure 5-1. D, DGV, and PW Package, 14 Pin SOIC, TVSOP, and TSSOP (Top View)

Figure 5-2. RGY Package, 14 Pin VQFN (Top View)

Table 5-1. Pin Functions, D. DGV, PW, RGY

ı	PIN	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	I TPE(")	DESCRIPTION
1A	2	I/O	Channel 1 input or output
1B	3	I/O	Channel 1 input or output
10E	1	I	Output enable, active high
2A	5	I/O	Channel 2 input or output
2B	6	I/O	Channel 2 input or output
20E	4	I	Output enable, active high
3A	9	I/O	Channel 3 input or output
3B	8	I/O	Channel 3 input or output
30E	10	I	Output enable, active high
4A	12	I/O	Channel 4 input or output
4B	11	I/O	Channel 4 input or output
40E	13	I	Output enable, active high
GND	7	_	Ground
V _{CC}	14	Р	Power supply
Thermal Pac	l	_	Exposed thermal pad. There is no requirement to solder this pad; if connected, it should be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power



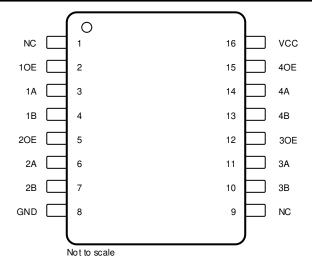


Figure 5-3. DBQ Package, 16 Pin SSOP (Top View)

Table 5-2. Pin Functions, DBQ

Р	IN	TYPE ⁽¹⁾	DESCRIPTION			
NAME	NO.	1115.				
1A	3	I/O	Channel 1 input or output			
1B	4	I/O	Channel 1 input or output			
10E	2	I	Output enable, active high			
2A	6	I/O	Channel 2 input or output			
2B	7	I/O	Channel 2 input or output			
20E	5	I	Output enable, active high			
3A	11	I/O	Channel 3 input or output			
3B	10	I/O	Channel 3 input or output			
3OE	12	I	Output enable, active high			
4A	14	I/O	Channel 4 input or output			
4B	13	I/O	Channel 4 input or output			
40E	15	I	Output enable, active high			
GND	8	_	Ground			
NC	9	_	No internal connection			
V _{CC}	16	Р	Power supply			

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
I _{I/O}	Continuous channel current			128	mA
I _{IK}	Input clamp current	V _{I/O} < 0		-50	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2000	V
V _(ESD)	Lieurostano disoriarge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		2.3	3.6	V	
V	High lovel control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	V _{CC}	V	
V _{IH}	High-level control input voltage	V _{CC} = 2.7 V to 3.6 V	2	V _{CC}	V	
.,	Lauriana antesi innutrationa	V _{CC} = 2.3 V to 2.7 V		0.7	V	
V _{IL}	Low-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	V	
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

		SN74CBTLV3126					
THERMAL METRIC(1)		D (SOIC)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DBQ (SSOP)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	16 Pins	
R _{0JA}	Junction-to-ambient thermal resistance	100.6	154.8	123.3	59.6	118.7	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	55.5	64.5	53.0	71.3	66.4	°C/W
R _{0JB}	Junction-to-board thermal resistance	56.8	88.4	66.3	35.6	62.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.0	11.1	9.3	4.2	20.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.4	87.4	65.7	35.7	61.7	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	16.1	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER		TEST CONDITION	S	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}		V _{CC} = 3 V,	I _I = -18 mA				-1.2	V
I		V _{CC} = 3.6 V,	V _I = V _{CC} or GND				±1	μA
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 3.6 V				10	μΑ
I _{CC}		V _{CC} = 3.6 V,	I _O = 0,	V _I = V _{CC} or GND			10	μΑ
ΔI _{CC} (2)	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V _{CC} or GND			300	μΑ
Ci	Control inputs	V _I = 3 V or 0				2.5		pF
C _{io(OFF)}		V _O = 3 V or 0,	OE = GND			7		pF
			V = 0	I _I = 64 mA		5	8	
		$V_{CC} = 2.3 \text{ V},$ TYP at $V_{CC} = 2.5 \text{ V}$	V _I = 0	I _I = 24 mA		5	8	
r _{on} (3)			V _I = 1.7 V,	I _I = 15 mA		27	40	Ω
I on W			V = 0	I _I = 64 mA		5	7	Ω
		V _{CC} = 3 V	V _I = 0	I _I = 24 mA		5	7	
			V _I = 2.4 V,	I _I = 15 mA		10	15	

- (1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
- (2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
- (3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

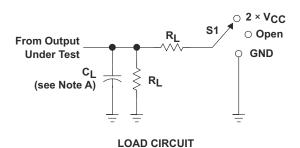
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 ± 0.2 V	V	$V_{CC} = 3.3 V$ $\pm 0.3 V$		UNIT	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX		
t _{pd} (1)	A or B	B or A		0.15		0.25	ns	
t _{en}	OE	A or B	1.6	4.5	1.9	4.2	ns	
t _{dis}	OE	A or B	1.3	4.7	1	4.8	ns	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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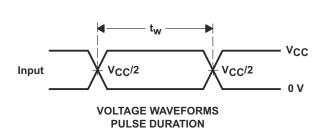
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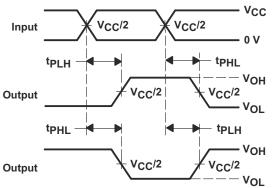
7 Parameter Measurement Information

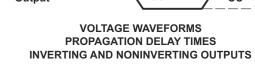


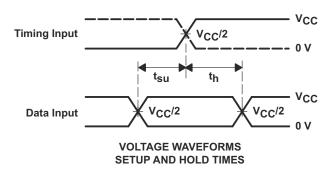
TEST	S 1
t _{PLH} /t _{PHL}	Open
tPLZ/tPZL	2 × V _{CC}
tPHZ/tPZH	GND

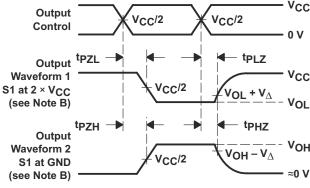
VCC	CL	R_{L}	${f v}_{\!\Delta}$
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V











VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2 ns, $t_r \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

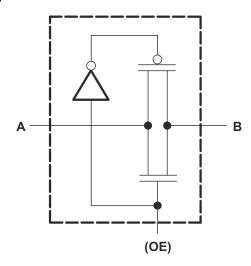
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low. This device is fully specified for partial-power-down applications using loff. The loff feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CBTLV3126 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74CBTLV3126 features $5-\Omega$ switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. I_{off} supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

8.4 Device Functional Modes

8.4.1 Function Table (Each Bus Switch)

Table 8-1 provides the truth table for the SN74CBTLV3126.

Table 8-1. Truth Table

INPUT OE	FUNCTION
L	Disconnect
Н	A port = B port



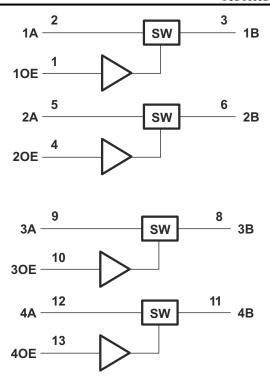


Figure 8-1. Logic Diagram (Positive Logic)

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

One useful application to take advantage of the SN74CBTLV3126 features is isolating various protocols from a possessor or MCU such as JTAG, SPI, or standard GPIO signals. The device provides excellent isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications.

9.2 Typical Application

9.2.1 Protocol and Signal Isolation

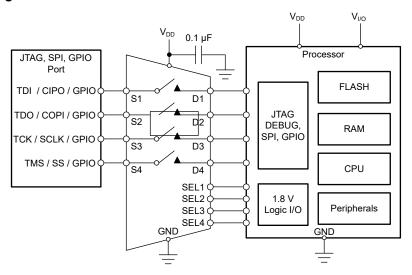


Figure 9-1. Typical Appliction

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V _{DD})	3.3 V
Input or output signal range	0 V to 3.3 V
Control logic thresholds	1.8 V compatible

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9.2.1.2 Detailed Design Procedure

The SN74CBTLV3126 can operate without any external components except for the supply decoupling capacitors. TI recommends that the digital control pins (OE) be pulled up to V_{CC} or down to GND to avoid an undesired switch state that could result from the floating pin. All input signals passing through the switch must fall within the *Recommend Operating Conditions* of the SN74CBTLV3126 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off Protection feature, and the inputs can range from 0 V to 3.3 V when $V_{DD} = 0$ V.

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners. Figure 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

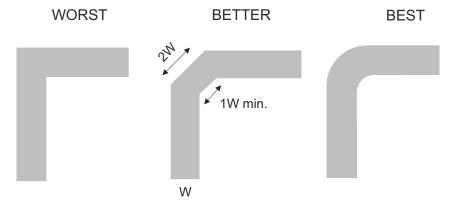


Figure 11-1. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

- Avoid stubs on the high-speed signals traces because they cause signal reflections.
- Route all high-speed signal traces over continuous GND planes, with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane splits.

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• When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 11-2.

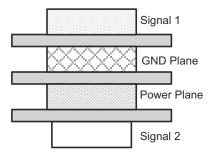


Figure 11-2. Example Layout

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

Figure 11-3 shows an example of a PCB layout with the SN74CBTLV3126. Some key considerations are:

Decouple the V_{DD} pin with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

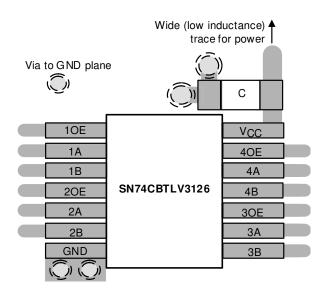


Figure 11-3. Example Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
74CBTLV3126DBQRG4	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
74CBTLV3126DBQRG4.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
74CBTLV3126DBQRG4.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
74CBTLV3126DGVRG4	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
74CBTLV3126DGVRG4.B	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126D	Obsolete	Production	SOIC (D) 14	-	=	Call TI	Call TI	-40 to 85	CBTLV3126
SN74CBTLV3126DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
SN74CBTLV3126DBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
SN74CBTLV3126DBQR.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
SN74CBTLV3126DGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126DGVR.B	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126
SN74CBTLV3126DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126
SN74CBTLV3126DR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126
SN74CBTLV3126PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	CL126
SN74CBTLV3126PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126PWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126PWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126
SN74CBTLV3126RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
SN74CBTLV3126RGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126
SN74CBTLV3126RGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS KO P1 BO BO Cavity AO

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3126DBQRG4	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
74CBTLV3126DGVRG4	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3126PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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*All dimensions are nominal

Device	Dookses Type	Bookens Drowing	Pins	SPQ	Langth (mm)	\A/idth /mama\	Llaimht (mana)
Device	Package Type	Package Drawing	Pins	SPU	Length (mm)	Width (mm)	Height (mm)
74CBTLV3126DBQRG4	SSOP	DBQ	16	2500	353.0	353.0	32.0
74CBTLV3126DGVRG4	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74CBTLV3126DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74CBTLV3126PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74CBTLV3126PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SHRINK SMALL-OUTLINE PACKAGE



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- 4. This dimension does not include interlead flash.5. Reference JEDEC registration MO-137, variation AB.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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