SCDS044I - DECEMBER 1997 - REVISED OCTOBER 2003

- **Member of the Texas Instruments** Widebus™ Family
- 4- Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- Ioff Supports Partial-Power-Down Mode Operation
- **Break-Before-Make Feature**
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

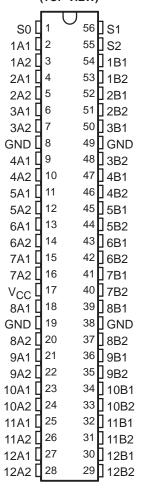
The SN74CBTLV16212 provides 24 bits of high-speed bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

This device is fully specified partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

The SN74CBTLV16212 is specified by the break-before-make feature to have no through current when switching between B ports.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



ORDERING INFORMATION

| TA | PACK | AGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|--------------------------|---------------------|
| | CCOD DI | Tube | SN74CBTLV16212DL | CDTI VACOAO |
| 40°C to 95°C | SSOP – DL | Tape and reel | SN74CBTLV16212DLR | CBTLV16212 |
| −40°C to 85°C | TSSOP - DGG | Tape and reel | SN74CBTLV16212GR | CBTLV16212 |
| | TVSOP - DGV | Tape and reel | SN74CBTLV16212VR | CN212 |

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.



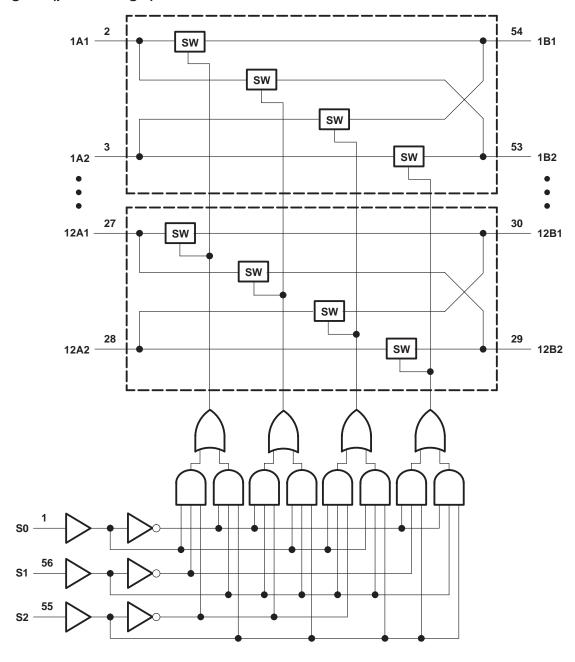
SN74CBTLV16212 LOW-VOLTAGE 24-BIT FET BUS-EXCHANGE SWITCH

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FUNCTION TABLE

| | INPUTS | | INPUTS/ | OUTPUTS | FUNCTION |
|----|--------|----|---------|---------|--|
| S2 | S1 | S0 | A1 | A2 | FUNCTION |
| L | L | L | Z | Z | Disconnect |
| L | L | Н | B1 | Z | A1 port = B1 port |
| L | Н | L | B2 | Z | A1 port = B2 port |
| L | Н | Н | Z | B1 | A2 port = B1 port |
| Н | L | L | Z | B2 | A2 port = B2 port |
| Н | L | Н | Z | Z | Disconnect |
| Н | Н | L | B1 | B2 | A1 port = B1 port A2 port = B2 port |
| Н | Н | Н | B2 | B1 | A1 port = B2 port A2 port = B1 port |

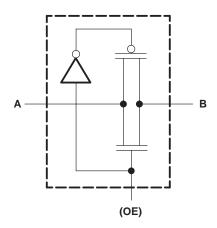
logic diagram (positive logic)





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simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V _{CC} | | -0.5 V to 4.6 V |
|---|-------------|-----------------|
| Input voltage range, V _I (see Note 1) | | |
| Continuous channel current | | 128 mA |
| Input clamp current, I _{IK} (V _I < 0) | | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | DGG package | 64°C/W |
| • | DGV package | 48°C/W |
| | DL package | 56°C/W |
| Storage temperature range, T _{stg} | | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| VCC | Supply voltage | 2.3 | 3.6 | V |
| ., | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | | ., |
| VIH | High-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2 | | V |
| ., | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | | 0.7 | V |
| VIL | Low-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | | | V |
| TA | Operating free-air temperature | -40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

SN74CBTLV16212 LOW-VOLTAGE 24-BIT FET BUS-EXCHANGE SWITCH

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PAI | RAMETER | | TEST CONDITION | ONS | MIN | TYP [†] | MAX | UNIT |
|---------------------|----------------|--|---------------------------------|--|-----|------------------|------|------|
| VIK | | $V_{CC} = 3 V$, | I _I = -18 mA | | | | -1.2 | V |
| II | | V _{CC} = 3.6 V, | $V_I = V_{CC}$ or GND | | | | ±1 | μΑ |
| l _{off} | | $V_{CC} = 0$, | V_I or $V_O = 0$ to 3.6 V | | | | 10 | μΑ |
| Icc | | V _{CC} = 3.6 V, | I _O = 0, | $V_I = V_{CC}$ or GND | | | 10 | μΑ |
| ΔICC [‡] | Control inputs | V _{CC} = 3.6 V, | One input at 3 V, | Other inputs at V _{CC} or GND | | | 300 | μΑ |
| Ci | Control inputs | V _I = 3 V or 0 | | | | 5 | | pF |
| C _{io(OFF} | =) | $V_0 = 3 \text{ V or } 0,$ | S_1 , S_2 , and $S_3 = GN$ | D | | 8 | | pF |
| | | | ., . | I _I = 64 mA | | 5 | 8 | |
| | | $V_{CC} = 2.3 \text{ V},$ TYP at $V_{CC} = 2.5 \text{ V}$ | $V_I = 0$ $I_I = 24 \text{ mA}$ | | | 5 | 8 | |
| . 8 | | | V _I = 1.7 V, | I _I = 15 mA | | 27 | 40 | 0 |
| r _{on} § | | | V 0 | I _I = 64 mA | | 5 | 7 | Ω |
| | | V _{CC} = 3 V | V _I = 0 | I _I = 24 mA | 5 7 | | 7 | |
| | | | V _I = 2.4 V, | I _I = 15 mA | | 10 | 15 | |

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

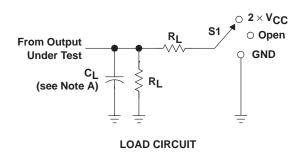
| PARAMETER | FROM | TO | V _{CC} = | 2.5 V 2 V | V _{CC} = | | UNIT |
|------------------|---------|----------|-------------------|--------------|-------------------|------|------|
| | (INPUT) | (OUTPUT) | MIN | MAX | MIN | MAX | |
| $t_{pd}\P$ | A or B | B or A | | 0.15 | | 0.25 | ns |
| ^t pd | S | B or A | 3 | 11.1 | 3 | 8.8 | ns |
| t _{en} | S | A or B | 3 | 10.9 | 3 | 8.6 | ns |
| ^t dis | S | A or B | 1 | 8.7 | 2 | 8.8 | ns |

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

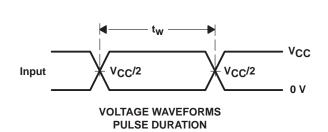
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

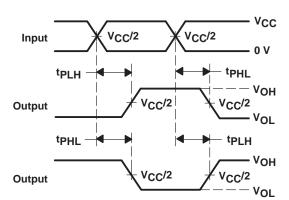
PARAMETER MEASUREMENT INFORMATION



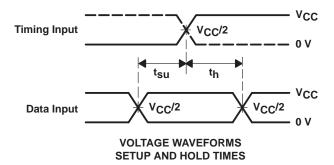
| TEST | S1 |
|------------------------------------|-------------------|
| tPLH/tPHL | Open |
| t _{PLZ} /t _{PZL} | 2×V _{CC} |
| tPHZ/tPZH | GND |

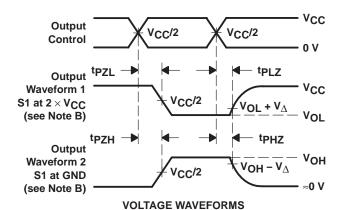
| VCC | CL | RL | $v_{\scriptscriptstyle\Delta}$ |
|--------------|-------|-------|--------------------------------|
| 2.5 V ±0.2 V | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ±0.3 V | 50 pF | 500 Ω | 0.3 V |





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS





ENABLE AND DISABLE TIMES

LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpZL and tpZH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ | MSL rating/ | Op temp (°C) | Part marking |
|-----------------------|--------|---------------|------------------|-----------------------|------|---------------|--------------------|--------------|--------------|
| | (1) | (2) | | | (3) | Ball material | Peak reflow | | (6) |
| | | | | | | (4) | (5) | | |
| SN74CBTLV16212DL | Active | Production | SSOP (DL) 56 | 20 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212DL.B | Active | Production | SSOP (DL) 56 | 20 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212DLR | Active | Production | SSOP (DL) 56 | 1000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212DLR.B | Active | Production | SSOP (DL) 56 | 1000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212GR | Active | Production | TSSOP (DGG) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212GR.B | Active | Production | TSSOP (DGG) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212GRG4 | Active | Production | TSSOP (DGG) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212GRG4.B | Active | Production | TSSOP (DGG) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV16212 |
| SN74CBTLV16212VR | Active | Production | TVSOP (DGV) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CN212 |
| SN74CBTLV16212VR.B | Active | Production | TVSOP (DGV) 56 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CN212 |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|-----------------|--------------------|------|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| SN74CBTLV16212DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74CBTLV16212GR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.9 | 14.7 | 1.4 | 12.0 | 24.0 | Q1 |
| SN74CBTLV16212GRG4 | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.9 | 14.7 | 1.4 | 12.0 | 24.0 | Q1 |
| SN74CBTLV16212VR | TVSOP | DGV | 56 | 2000 | 330.0 | 24.4 | 6.8 | 11.7 | 1.6 | 12.0 | 24.0 | Q1 |



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*All dimensions are nominal

| 7 til dillionoro dio monimiai | | | | | | | |
|-------------------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
| SN74CBTLV16212DLR | SSOP | DL | 56 | 1000 | 356.0 | 356.0 | 53.0 |
| SN74CBTLV16212GR | TSSOP | DGG | 56 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74CBTLV16212GRG4 | TSSOP | DGG | 56 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74CBTLV16212VR | TVSOP | DGV | 56 | 2000 | 356.0 | 356.0 | 45.0 |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74CBTLV16212DL | DL | SSOP | 56 | 20 | 473.7 | 14.24 | 5110 | 7.87 |
| SN74CBTLV16212DL.B | DL | SSOP | 56 | 20 | 473.7 | 14.24 | 5110 | 7.87 |

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194







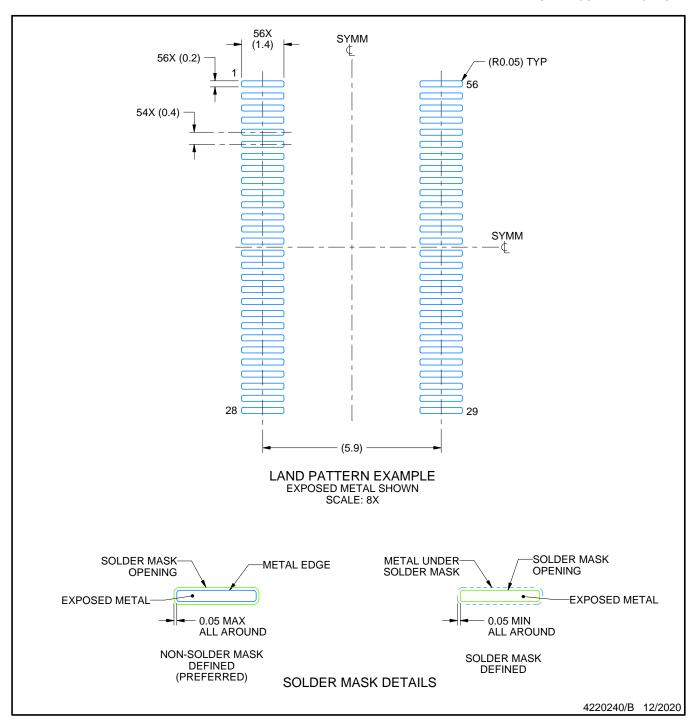
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-194.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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