SCDS084G - JULY 1998 - REVISED JULY 2002

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

description/ordering information

The SN74CBTD3861 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as one 10-bit switch with a single output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)

NC[1	\bigcup_{24}] v _{cc}
A1 [2	23] OE
A2[3	22] B1
А3[4	21	B2
A4 [5	20	B 3
A5 [6	19] B4
A6 [7	18] B5
A7 [8	17] B6
A8 🗌	9	16	B7
A9 🗌	10	15	B8
A10	11	14	B9
GND [12	13	B10

NC - No internal connection

ORDERING INFORMATION

TA	PACKAG	ΕŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC - DW	Tube	SN74CBTD3861DW	CBTD3861
	301C - DW	Tape and reel	SN74CBTD3861DWR	CB1D3661
-40°C to 85°C	SSOP – DB	Tape and reel	SN74CBTD3861DBR	CC861
-40 C to 65 C	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTD3861DBQR	CBTD3861
	TSSOP – PW	Tape and reel	SN74CBTD3861PWR	CC861
	TVSOP – DGV	Tape and reel	SN74CBTD3861DGVR	CC861

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect

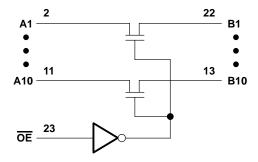


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SCDS084G - JULY 1998 - REVISED JULY 2002

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		
Package thermal impedance, θ _{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

SCDS084G - JULY 1998 - REVISED JULY 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITION	ONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA				-1.2	V
Vон		See Figure 2						
II		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$				±1	μΑ
Icc		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			1.5	mA
Δl _{CC} ‡	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				2.5		pF
C _{io(OFF}	=)	$V_0 = 3 \text{ V or } 0,$	OE = V _{CC}			4		pF
			V: - 0	I _I = 64 mA		5	7	
r _{on} §		V _{CC} = 4.5 V	V _I = 0	I _I = 30 mA		5	7	Ω
			V _I = 2.4 V,	I _I = 15 mA		20	50	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pd} ¶	A or B	B or A		0.35	ns
^t en	ŌĒ	A or B	2.6	10	ns
^t dis	ŌĒ	A or B	1	6	ns

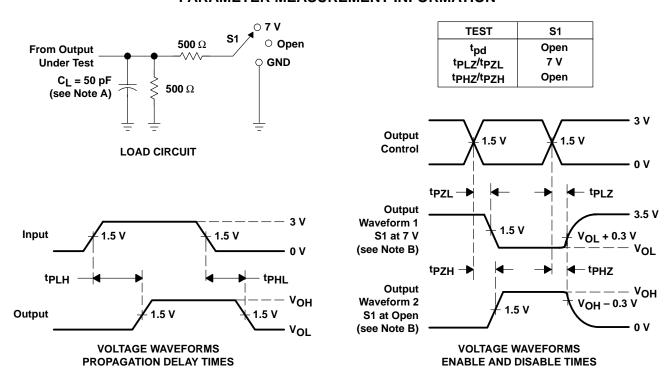
The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

PARAMETER MEASUREMENT INFORMATION



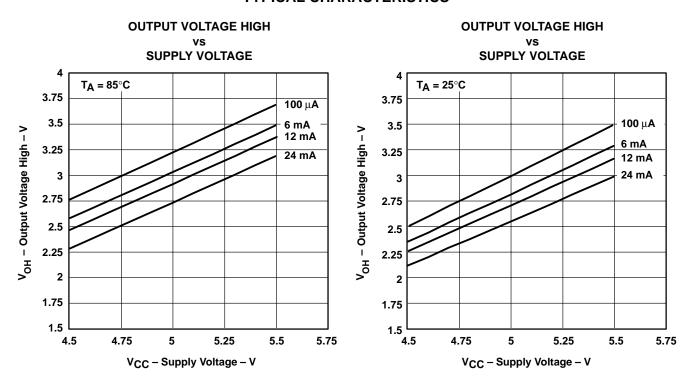
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS



OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE

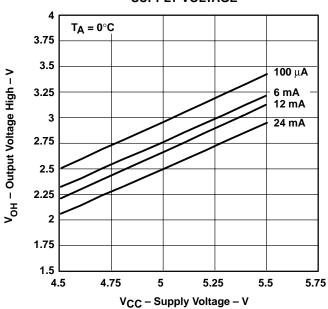


Figure 2. V_{OH} Values



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	` ,	.,			. ,	(4)	(5)		
SN74CBTD3861DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTD3861
SN74CBTD3861DBQR.A	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTD3861
SN74CBTD3861DBR	NRND	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861DBR.A	NRND	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861DGVR	NRND	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861DGVR.A	NRND	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861DW	NRND	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTD3861
SN74CBTD3861DW.A	NRND	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTD3861
SN74CBTD3861DWR	NRND	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTD3861
SN74CBTD3861DWR.A	NRND	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTD3861
SN74CBTD3861PW	NRND	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861PW.A	NRND	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861PWE4	NRND	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861PWG4	NRND	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861
SN74CBTD3861PWR.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC861

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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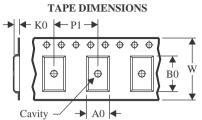
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTD3861DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTD3861DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74CBTD3861DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTD3861DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTD3861PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTD3861DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CBTD3861DBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74CBTD3861DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74CBTD3861DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBTD3861PWR	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBTD3861DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTD3861DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTD3861PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CBTD3861PW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CBTD3861PWE4	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CBTD3861PWG4	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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