SCDS030L - JANUARY 1996 - REVISED JANUARY 2004

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

#### description/ordering information

The SN74CBTD3306 features two independent line switches. Each switch is disabled when the associated output-enable  $(\overline{OE})$  input is high. A diode to  $V_{CC}$  is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

#### 

#### ORDERING INFORMATION

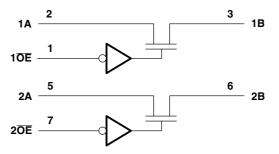
T <sub>A</sub>	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
−40°C to 85°C	0010 B	Tube	SN74CBTD3306D	00000	
	SOIC - D	Tape and reel	SN74CBTD3306DR	CC306	
	TSSOP – PW	Tube	SN74CBTD3306PW	CC306	
	1330P - PW	Tape and reel	SN74CBTD3306PWR	CC306	

<sup>&</sup>lt;sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION				
L	A port = B port				
Н	Disconnect				

## logic diagram (positive logic)





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	$-0.5\;V$ to 7 $V$
Input voltage range, V <sub>I</sub> (see Note 1)	$\dots$ –0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{ K }(V_{ /O} < 0)$	–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): D package	97°C/W
PW package	149°C/W
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level control input voltage	2		٧
$V_{IL}$	Low-level control input voltage		0.8	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER		TEST CONDI	MIN	TYP‡	MAX	UNIT	
$V_{IK}$		$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA				-1.2	V
V <sub>OH</sub>		See Figure 2						
II		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$				±1	μΑ
I <sub>CC</sub>		$V_{CC} = 5.5 \text{ V},$	$I_{O} = 0,$	$V_I = V_{CC}$ or GND			1.5	mA
$\Delta I_{CC}$ §	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at $V_{CC}$ or GND			2.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0				3		pF
C <sub>io(OFF</sub>	)	$V_{O} = 3 \text{ V or } 0,$	OE = V <sub>CC</sub>			4		pF
				I <sub>I</sub> = 64 mA		5	7	
$r_{on}^\P$		$V_{CC} = 4.5 \text{ V}$	V <sub>1</sub> = 0	$I_I = 30 \text{ mA}$		5	7	Ω
			$V_1 = 2.4 V$ ,	I <sub>I</sub> = 15 mA	35 50			

<sup>&</sup>lt;sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

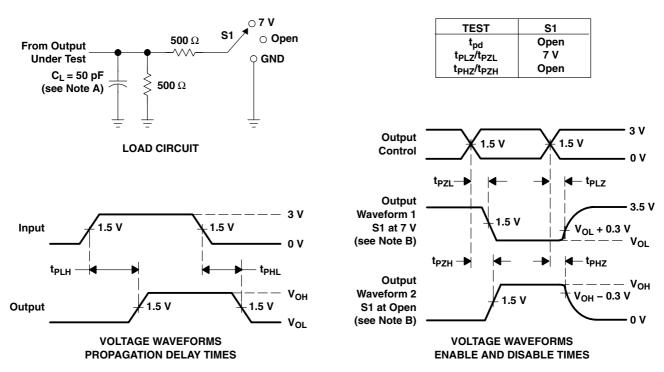
<sup>¶</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> †	A or B	B or A		0.25	ns
t <sub>en</sub>	ŌE	A or B	2.1	5.4	ns
t <sub>dis</sub>	ŌĒ	A or B	1	4.7	ns

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

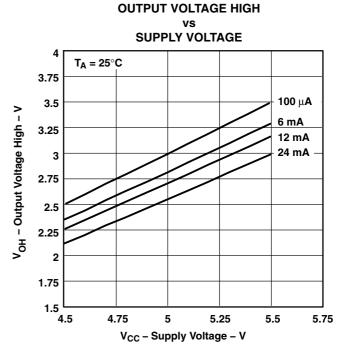
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



### **TYPICAL CHARACTERISTICS**

#### **OUTPUT VOLTAGE HIGH SUPPLY VOLTAGE** $T_A = 85^{\circ}C$ 3.75 **100** μ**A** 3.5 6 mA V<sub>OH</sub> - Output Voltage High - V 12 mA 3.25 24 mA 3 2.75 2.5 2.25 2 1.75 1.5 4.5 4.75 5 5.25 5.5 5.75 V<sub>CC</sub> - Supply Voltage - V



#### **OUTPUT VOLTAGE HIGH**

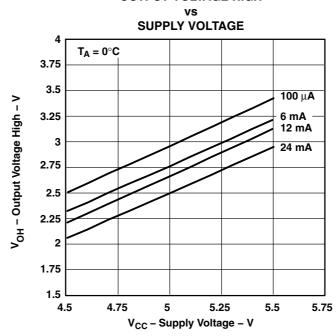


Figure 2. V<sub>OH</sub> Values



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
						(4)	(5)		
SN74CBTD3306D	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 85	CC306
SN74CBTD3306DR	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 85	CC306
SN74CBTD3306PW	Obsolete	Production	TSSOP (PW)   8	-	-	Call TI	Call TI	-40 to 85	CC306
SN74CBTD3306PWR	Obsolete	Production	TSSOP (PW)   8	-	-	Call TI	Call TI	-40 to 85	CC306
SN74CBTD3306PWRG3	Preview	Production	TSSOP (PW)   8	2000   null	-	Call TI	Call TI	-40 to 85	
SN74CBTD3306PWRG4	Obsolete	Production	TSSOP (PW)   8	-	-	Call TI	Call TI	-40 to 85	CC306

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



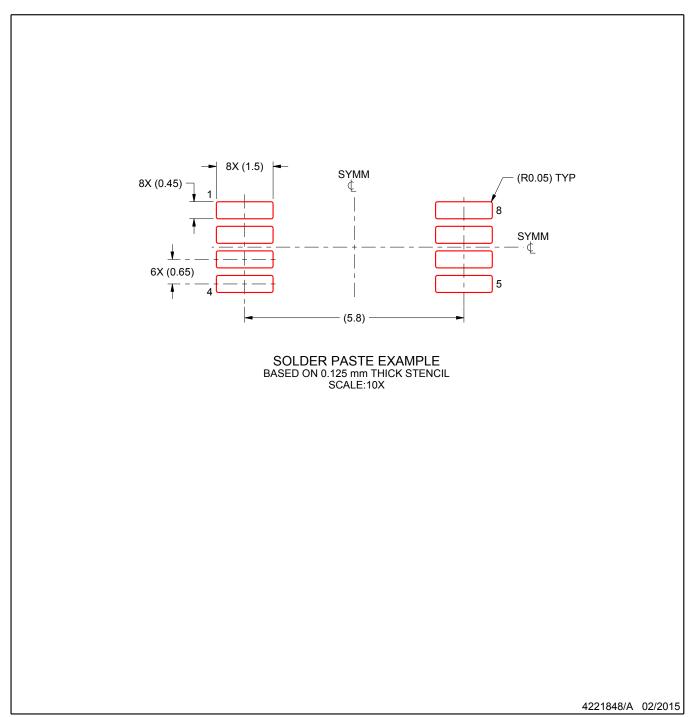
NOTES: (continued)

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SMALL OUTLINE PACKAGE



NOTES: (continued)

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