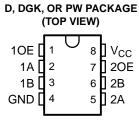
# SN74CBT3305C DUAL FET BUS SWITCH 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS125B-SEPTEMBER 2003-REVISED AUGUST 2005

#### **FEATURES**

- Undershoot Protection for OFF Isolation on A and B Ports up to -2 V
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance  $(r_{on})$  Characteristics  $(r_{on} = 3 \Omega \text{ Typ})$
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C<sub>io(OFF)</sub> = 5 pF Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I<sub>CC</sub> = 3 μA Max)
- V<sub>CC</sub> Operating Range From 4 V to 5.5 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)

- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, ClassII
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating



## **DESCRIPTION/ORDERING INFORMATION**

The SN74CBT3305C is a high-speed TTL-compatible FET bus switch with low ON-state resistance  $(r_{on})$ , allowing for minimal propagation delay. Active undershoot-protection circuitry on the A and B ports of the device provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3305C is organized as two 1-bit bus switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON, and the A port is conncected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

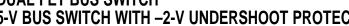
# **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SOIC - D	Tube	SN74CBT3305CD	- CU305C	
	30IC - D	Tape and reel	SN74CBT3305CDR	C0305C	
–40°C to 85°C	VSSOP - DGK	Tape and reel	SN74CBT3305CDGKR	SNR	
	TSSOP – PW	Tube	SN74CBT3305CPW	CLISOFC	
		Tape and reel	SN74CBT3305CPWR	CU305C	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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# **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

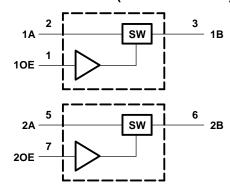
This device is fully specified for partial-power-down application using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

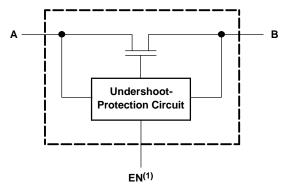
## **FUNCTION TABLE** (EACH BUS SWITCH)

INPUT OE	INPUT/OUTPUT A	FUNCTION
Н	В	A port = B port
L	Z	Disconnect

## **LOGIC DIAGRAM (POSITIVE LOGIC)**



## SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.



# SN74CBT3305C DUAL FET BUS SWITCH 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

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# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	TINU
$V_{CC}$	Supply voltage		-0.5	7	V
$V_{IN}$	Control input voltage range (2)(3)		-0.5	7	V
$V_{I/O}$	Switch I/O voltage range (2)(3)(4)		-0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0		-50	mA
I <sub>I/OK</sub>	I/O port clamp current	V <sub>I/O</sub> < 0		-50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>			±128	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		D package		97	
$\theta_{JA}$	Package thermal impedance (6)	DGK package		179	°C/W
		PW package		149	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_1$  and  $V_2$  are used to denote specific conditions for  $V_{1/2}$ .
- (5)  $I_1$  and  $I_0$  are used to denote specific conditions for  $I_{1/0}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

# Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4	5.5	V
V <sub>IH</sub>	High-level control input voltage	2	5.5	V
$V_{IL}$	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

<sup>(1)</sup> All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# SN74CBT3305C **DUAL FET BUS SWITCH** 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

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## Electrical Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

P.A	ARAMETER		TEST CONDITION	IS	MIN TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IK</sub>	Control inputs	V <sub>CC</sub> = 4.5 V,	$I_{IN} = -18 \text{ mA}$			-1.8	V
V <sub>IKU</sub>	Data inputs	V <sub>CC</sub> = 5 V,	0 mA > $I_I \ge -50$ mA, $V_{IN} = V_{CC}$ or GND,	Switch OFF		-2	V
I <sub>IN</sub>	Control inputs	$V_{CC} = 5.5 V,$	$V_{IN} = V_{CC}$ or GND			±1	μΑ
I <sub>OZ</sub> (3)		V <sub>CC</sub> = 5.5 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND		±10	μΑ
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_0 = 0 \text{ to } 5.5 \text{ V},$	$V_I = 0$		10	μΑ
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	$I_{I/O} = 0,$ $V_{IN} = V_{CC}$ or GND,	Switch ON or OFF		3	μΑ
$\Delta I_{CC}^{(4)}$	Control inputs	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND		2.5	mA
C <sub>in</sub>	Control inputs	V <sub>IN</sub> = 3 V or 0			3		pF
C <sub>io(OFF)</sub>		$V_{I/O} = 3 \text{ V or } 0,$	Switch OFF,	$V_{IN} = V_{CC}$ or GND	5		pF
C <sub>io(ON)</sub>		$V_{I/O} = 3 \text{ V or } 0,$	Switch ON,	$V_{IN} = V_{CC}$ or GND	12.5		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V <sub>I</sub> = 2.4 V,	I <sub>O</sub> = -15 mA	8	12	
r <sub>on</sub> <sup>(5)</sup>			V = 0	I <sub>O</sub> = 64 mA	3	6	Ω
3		V <sub>CC</sub> = 4.5 V	$V_I = 0$	I <sub>O</sub> = 30 mA	3 6		
			$V_1 = 2.4 V,$	$I_O = -15 \text{ mA}$	5	10	

- $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_{I},\ V_{O},\ I_{I},$  and  $I_{O}$  refer to data pins. All typical values are at  $V_{CC}$  = 5 V (unless otherwise noted),  $T_{A}$  = 25°C. For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.
- This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND
- Measured by the voltage drop between the A and B terminals at the indicate current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

#### **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V	$V_{CC}$ = 5 V $\pm$ 0.5 V		UNIT
	(INFOT)	(001F01)	MIN MAX	MIN	MAX	
t <sub>pd</sub> <sup>(1)</sup>	A or B	B or A	0.24		0.15	ns
t <sub>en</sub>	OE	A or B	4.4	1.5	4.1	ns
t <sub>dis</sub>	OE	A or B	5.1	1.5	4.8	ns

<sup>(1)</sup> The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

#### **Undershoot Characteristics**

See Figure 1 and Figure 2

PARAMETER		TEST CONDITION	NS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OUTU</sub>	$V_{CC} = 5.5 \text{ V},$	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

(1) All typical values are at  $V_{CC}$  = 5 V (unless otherwise noted),  $T_A$  = 25°C.



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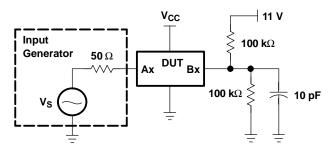


Figure 1. Device Test Setup

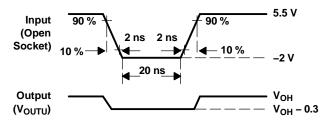
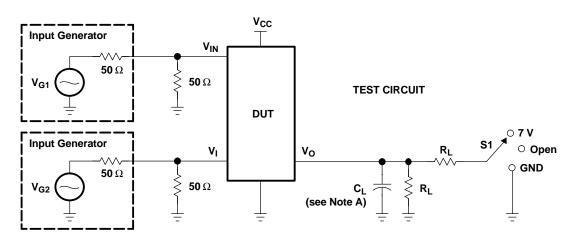


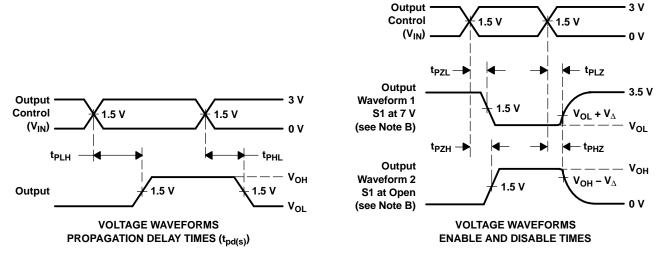
Figure 2. Transient Input Voltage (V<sub>I</sub>) and Output Voltage (V<sub>OUTU</sub>) Waveforms (Switch OFF)



#### PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	VI	CL	$\mathbf{V}_{\Delta}$
t <sub>pd(s)</sub>	5 V ± 0.5 V 4 V	Open Open	<b>500</b> Ω <b>500</b> Ω	V <sub>CC</sub> or GND V <sub>CC</sub> or GND	50 pF 50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V 4 V	7 V 7 V	<b>500</b> Ω <b>500</b> Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V 4 V	Open Open	<b>500</b> Ω <b>500</b> Ω	V <sub>CC</sub>	50 pF 50 pF	0.3 V 0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  2.5 ns.  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd(s)}$ . The  $t_{pd}$  propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74CBT3305CD	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CD.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CPW	Active	Production	TSSOP (PW)   8	150   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CPW.B	Active	Production	TSSOP (PW)   8	150   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CPWR	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CPWR.B	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C
SN74CBT3305CPWRG4	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# PACKAGE OPTION ADDENDUM

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# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION



# TAPE DIMENSIONS KO P1 BO W Cavity A0

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3305CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3305CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3305CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3305CDR	SOIC	D	8	2500	353.0	353.0	32.0
SN74CBT3305CDR	SOIC	D	8	2500	340.5	336.1	25.0
SN74CBT3305CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3305CD	D	SOIC	8	75	507	8	3940	4.32
SN74CBT3305CD	D	SOIC	8	75	506.6	8	3940	4.32
SN74CBT3305CD.B	D	SOIC	8	75	506.6	8	3940	4.32
SN74CBT3305CD.B	D	SOIC	8	75	507	8	3940	4.32
SN74CBT3305CPW	PW	TSSOP	8	150	530	10.2	3600	3.5
SN74CBT3305CPW.B	PW	TSSOP	8	150	530	10.2	3600	3.5



SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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