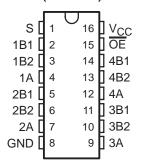
## SN74CBT3257C 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

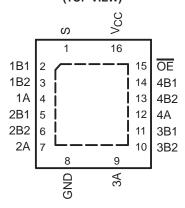
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- Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r<sub>on</sub>)
   Characteristics (r<sub>on</sub> = 3 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C<sub>io(OFF)</sub> = 5.5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I<sub>CC</sub> = 3 μA Max)
- V<sub>CC</sub> Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports I<sup>2</sup>C Bus Expansion
- Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating

# D, DB, DBQ, OR PW PACKAGE (TOP VIEW)



#### RGY PACKAGE (TOP VIEW)



## description/ordering information

#### ORDERING INFORMATION

TA	PACKAG	ΕŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	QFN – RGY	Tape and reel	SN74CBT3257CRGYR	CU257C		
	colo p	Tube	SN74CBT3257CD	ODT20570		
	SOIC - D	Tape and reel	SN74CBT3257CDR	CBT3257C		
-40°C to 85°C	SSOP - DB	Tape and reel	SN74CBT3257CDBR	CU257C		
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3257CDBQR	CU257C		
	TSSOP – PW	Tube	SN74CBT3257CPW	CU257C		
	1330F - FW	Tape and reel	SN74CBT3257CPWR	C0237C		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



## SN74CBT3257C 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

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## description/ordering information (continued)

The SN74CBT3257C is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3257C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3257C is a 4-bit 1-of-2 multiplexer/demultiplexer with a single output-enable  $(\overline{OE})$  input. The select (S) input controls the data path of the multiplexer/demultiplexer. When  $\overline{OE}$  is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

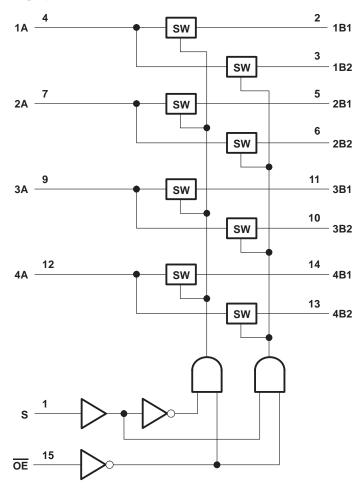
#### **FUNCTION TABLE**

INP	JTS	INPUT/OUTPUT	FUNCTION				
OE	S1	Α	FUNCTION				
L	L	B1	A port = B1 port				
L	Н	B2	A port = B2 port				
Н	X	Z	Disconnect				

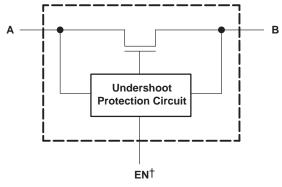


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## logic diagram (positive logic)



# simplified schematic, each FET switch (SW)



 $\ensuremath{^\dagger}\text{EN}$  is the internal enable signal applied to the switch.



## SN74CBT3257C 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Control input voltage range, V <sub>IN</sub> (see Notes 1 and 2)	0.5 V to 7 V
Switch I/O voltage range, V <sub>I/O</sub> (see Notes 1, 2, and 3)	0.5 V to 7 V
Control input clamp current, I <sub>IK</sub> (V <sub>IN</sub> < 0)	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O}$ < 0)	
ON-state switch current, I <sub>I/O</sub> (see Note 4)	±128 mA
Continuous current through V <sub>CC</sub> or GND terminals	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 5): D package	73°C/W
(see Note 5): DB package	82°C/W
(see Note 5): DBQ package	90°C/W
(see Note 5): PW package	108°C/W
(see Note 6): RGY package	39°C/W
Storage temperature range, T <sub>stq</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
  - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 3. V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
  - 4. II and IO are used to denote specific conditions for II/O.
  - 5. The package thermal impedance is calculated in accordance with JESD 51-7.
  - 6. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2	5.5	V
VIL	Low-level control input voltage	0	8.0	V
V <sub>I/O</sub>	Data input/output voltage	0	5.5	V
TA	Operating free-air temperature	-40	85	°C

NOTE 7: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



## SN74CBT3257C 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITION	CONDITIONS MIN TYPT MAX		UNIT		
VIK	Control inputs	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$				-1.8	V
VIKU	Data inputs	V <sub>CC</sub> = 5 V,	$0 \text{ mA} > I_{I} \ge -50 \text{ mA},$ $V_{IN} = V_{CC} \text{ or GND},$	Switch OFF			-2	V
I <sub>IN</sub>	Control inputs	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$ or GND				±1	μΑ
loz‡		V <sub>CC</sub> = 5.5 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±10	μΑ
l <sub>off</sub>		$V_{CC} = 0$ ,	$V_0 = 0 \text{ to } 5.5 \text{ V},$	V <sub>I</sub> = 0			10	μΑ
ICC		V <sub>CC</sub> = 5.5 V,	$I_{I/O} = 0,$ $V_{IN} = V_{CC}$ or GND,	Switch ON or OFF			3	μΑ
∆l <sub>CC</sub> §	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>in</sub>	Control inputs	V <sub>IN</sub> = 3 V or 0				3.5		pF
C	A port	V 2 V or 0	Switch OFF	V V or CND		8.5		pF
C <sub>io(OFF)</sub>	B port	$V_{I/O} = 3 \text{ V or } 0,$	Switch OFF,	$V_{IN} = V_{CC}$ or GND		5.5		pF
C <sub>io(ON)</sub>		$V_{I/O} = 3 \text{ V or } 0,$	Switch ON,	$V_{IN} = V_{CC}$ or GND		16.5		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V <sub>I</sub> = 2.4 V,	I <sub>O</sub> = -15 mA		8	12	
$_{ron}\P$				I <sub>O</sub> = 64 mA		3	6	Ω
	V <sub>CC</sub> = 4.5 V		V <sub>I</sub> = 0	I <sub>O</sub> = 30 mA		3	6	
			V <sub>I</sub> = 2.4 V,	I <sub>O</sub> = -15 mA		5	10	

 $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	TO	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t <sub>pd</sub> #	A or B	B or A		0.24		0.15	ns
t <sub>pd(s)</sub>	S	А		6	1.5	5.6	ns
	S	В		6.3	1.5	5.8	
<sup>t</sup> en	ŌĒ	A or B		6.3	1.5	5.8	ns
4	S	В		6.5	1.5	6	
<sup>t</sup> dis	ŌĒ	A or B		5.9	1.5	5.9	ns

<sup>#</sup>The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 5 V (unless otherwise noted),  $T_A$  = 25°C.

<sup>‡</sup> For I/O ports, the parameter IO7 includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at the specified voltage level, rather than VCC or GND.

<sup>¶</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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## undershoot characteristics (see Figures 1 and 2)

PARAMETER		TEST CONDITION	MIN	TYP†	MAX	UNIT	
Vоити	$V_{CC} = 5.5 \text{ V},$	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	V <sub>OH</sub> -0.3		V

 $<sup>\</sup>overline{\dagger}$  All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

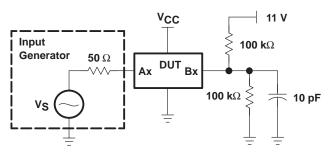


Figure 1. Device Test Setup

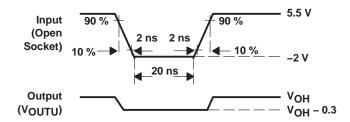
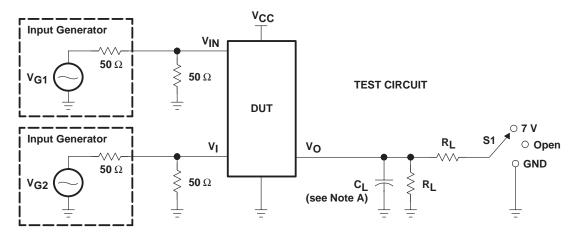


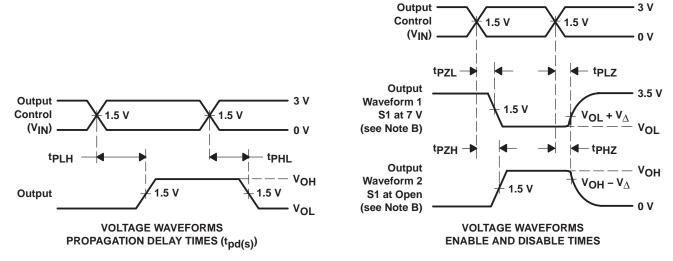
Figure 2. Transient Input Voltage (V<sub>I</sub>) and Output Voltage (V<sub>OUTU</sub>) Waveforms (Switch OFF)

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#### PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	$v_{\!\scriptscriptstyle\Delta}$
tpd(s)	$\begin{array}{c} \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{4 V} \end{array}$	Open Open	<b>500</b> Ω <b>500</b> Ω	V <sub>CC</sub> or GND V <sub>CC</sub> or GND	50 pF 50 pF	
tPLZ/tPZL	5 V ± 0.5 V 4 V	7 V 7 V	<b>500</b> Ω <b>500</b> Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
tPHZ/tPZH	5 V ± 0.5 V 4 V	Open Open	<b>500</b> Ω <b>500</b> Ω	V <sub>CC</sub>	50 pF 50 pF	0.3 V 0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{O} = 50 \Omega$ ,  $t_{f} \leq$  2.5 ns,  $t_{f} \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms



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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74CBT3257CD	Active	Production	SOIC (D)   16	40   TUBE	Yes	(4) NIPDAU	(5) Level-1-260C-UNLIM	-40 to 85	CBT3257C
SN74CBT3257CD.B	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3257C
SN74CBT3257CDBQR	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CDBQR.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CDBQRG4	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CDBQRG4.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CDBR	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CDBR.B	Active	Production	SSOP (DB)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CDR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3257C
SN74CBT3257CDR.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3257C
SN74CBT3257CDRG4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3257C
SN74CBT3257CPW	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CPW.B	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CPWR	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CPWR.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CPWRE4	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CPWRG4	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CPWRG4.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU257C
SN74CBT3257CRGYR	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CRGYR.B	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CRGYRG4	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C
SN74CBT3257CRGYRG4.B	Active	Production	VQFN (RGY)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU257C

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.



## **PACKAGE OPTION ADDENDUM**

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3257CDBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3257CDBQRG4	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3257CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74CBT3257CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBT3257CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3257CPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3257CRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74CBT3257CRGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3257CDBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBT3257CDBQRG4	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBT3257CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74CBT3257CDR	SOIC	D	16	2500	353.0	353.0	32.0
SN74CBT3257CPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74CBT3257CPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CBT3257CRGYR	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74CBT3257CRGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3257CD	D	SOIC	16	40	507	8	3940	4.32
SN74CBT3257CD.B	D	SOIC	16	40	507	8	3940	4.32
SN74CBT3257CPW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74CBT3257CPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



# RGY (R-PVQFN-N16)

## PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



# RGY (R-PVQFN-N16)

# PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



# D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SHRINK SMALL-OUTLINE PACKAGE



- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- 4. This dimension does not include interlead flash.5. Reference JEDEC registration MO-137, variation AB.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SHRINK SMALL-OUTLINE PACKAGE



- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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