SCDS131A - SEPTEMBER 2003 - REVISED OCTOBER 2003

- Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r<sub>on</sub>)
   Characteristics (r<sub>on</sub> = 3 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C<sub>io(OFF)</sub> = 5.5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I<sub>CC</sub> = 3 μA Max)
- V<sub>CC</sub> Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

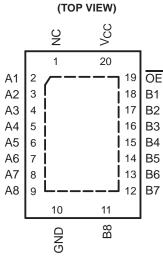
DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)

		т		1
ис [	1	$\cup$	20	] ∨ <sub>cc</sub>
A1 [	2		19	] OE
A2 [	3		18	] B1
АЗ [	4		17	] B2
A4 [	5		16	] B3
A5 [	6		15	] B4
A6 [	7		14	] B5
A7 [	8		13	] B6
A8 [	9		12	] B7
GND [	10		11	] B8

NC - No internal connection

- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

**RGY PACKAGE** 



NC - No internal connection

### description/ordering information

The SN74CBT3245C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3245C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3245C is organized as an 8-bit bus switch with a single output-enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the bus switch is OFF, and the high-impedance state exists between the A and B ports.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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# description/ordering information (continued)

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### **ORDERING INFORMATION**

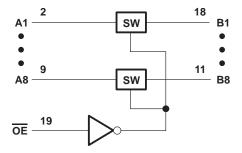
TA	PACKAGI	dž	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Tape and reel	SN74CBT3245CRGYR	CU245C
	0010 014	Tube	SN74CBT3245CDW	00700450
	SOIC - DW	Tape and reel	SN74CBT3245CDWR	CBT3245C
	0000 00	Tube SN74CBT3245CDB		
-40°C to 85°C	SSOP – DB	Tape and reel	SN74CBT3245CDBR	CU245C
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3245CDBQR	CBT3245C
	TOOOD DW	Tube	SN74CBT3245CPW	0110450
	TSSOP – PW	Tape and reel	SN74CBT3245CPWR	CU245C
	TVSOP - DGV	Tape and reel	SN74CBT3245CDGVR	CU245C

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect

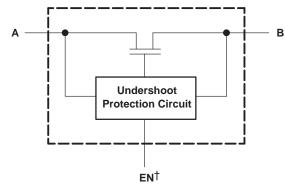
# logic diagram (positive logic)





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# simplified schematic, each FET switch (SW)



†EN is the internal enable signal applied to the switch.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

upply voltage range, V <sub>CC</sub>	
witch I/O voltage range, V <sub>I/O</sub> (see Notes 1, 2, and 3)	
control input clamp current, I <sub>IK</sub> (V <sub>IN</sub> < 0)	–50 mA
O port clamp current, I <sub>I/OK</sub> (V <sub>I/O</sub> < 0)	–50 mA
N-state switch current, I <sub>I/O</sub> (see Note 4)	±128 mA
continuous current through V <sub>CC</sub> or GND terminals	±100 mA
ackage thermal impedance, $\theta_{JA}$ (see Note 5): DB package	70°C/W
(see Note 5): DBQ package	68°C/W
(see Note 5): DGV package	92°C/W
(see Note 5): DW package	58°C/W
(see Note 5): PW package	83°C/W
(see Note 6): RGY package	37°C/W
torage temperature range, T <sub>stg</sub>	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.

- 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 3. V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- 4. II and IO are used to denote specific conditions for II/O.
- 5. The package thermal impedance is calculated in accordance with JESD 51-7.
- 6. The package thermal impedance is calculated in accordance with JESD 51-5.

# recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2	5.5	V
VIL	Low-level control input voltage	0	8.0	V
V <sub>I/O</sub>	Data input/output voltage	0	5.5	V
TA	Operating free-air temperature	-40	85	°C

NOTE 7: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER		TEST CONDITIO	NS	MIN	TYP	MAX	UNIT
VIK	Control inputs	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$				-1.8	V
VIKU	Data inputs	V <sub>CC</sub> = 5 V,	$0 \text{ mA} > I_{I} \ge -50 \text{ mA},$ $V_{IN} = V_{CC} \text{ or GND},$	Switch OFF			-2	V
I <sub>IN</sub>	Control inputs	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$ or GND				±1	μΑ
loz‡		V <sub>CC</sub> = 5.5 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±10	μА
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_0 = 0 \text{ to } 5.5 \text{ V},$	V <sub>I</sub> = 0			10	μΑ
ICC		V <sub>CC</sub> = 5.5 V,	$I_{I/O} = 0,$ $V_{IN} = V_{CC} \text{ or GND},$	Switch ON or OFF			3	μА
∆ICC§	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>in</sub>	Control inputs	$V_{IN} = 3 V \text{ or } 0$				4		pF
C <sub>io(OFF)</sub>		$V_{I/O} = 3 \text{ V or } 0,$	Switch OFF,	$V_{IN} = V_{CC}$ or GND		5.5		pF
C <sub>io(ON)</sub>		$V_{I/O} = 3 \text{ V or } 0,$	Switch ON,	$V_{IN} = V_{CC}$ or GND		14		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V <sub>I</sub> = 2.4 V,	I <sub>O</sub> = -15 mA		8	12	
$r_{on}\P$	r <sub>on</sub> ¶		V 0	I <sub>O</sub> = 64 mA		3	6	Ω
0		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>O</sub> = 30 mA		3	6	
			V <sub>I</sub> = 2.4 V,	$I_O = -15 \text{ mA}$		5	10	

 $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_{I}$ ,  $V_{O}$ ,  $I_{I}$ , and  $I_{O}$  refer to data pins. † All typical values are at  $V_{CC}$  = 5 V (unless otherwise noted),  $T_{A}$  = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V	V <sub>CC</sub> =	= 5 V 5 V	UNIT
	(INPOT)	(001701)	MIN MAX	MIN	MAX	
t <sub>pd</sub> #	A or B	B or A	0.24		0.15	ns
t <sub>en</sub>	ŌE	A or B	5.1	1.5	4.7	ns
t <sub>dis</sub>	ŌĒ	A or B	4.9	1.5	5.3	ns

<sup>#</sup>The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

For I/O ports, the parameter IOZ includes the input leakage current.

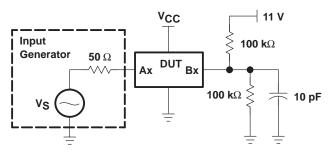
<sup>§</sup> This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

<sup>¶</sup>Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

# undershoot characteristics (see Figures 1 and 2)

PARAMETER		TEST CONDI	TIONS	MIN	TYP†	MAX	UNIT
VOUTU	$V_{CC} = 5.5 \text{ V},$	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	V <sub>OH</sub> -0.3		V

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.





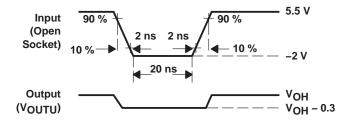
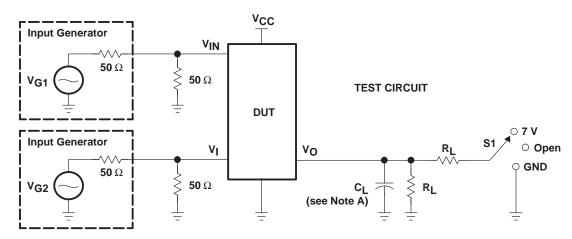


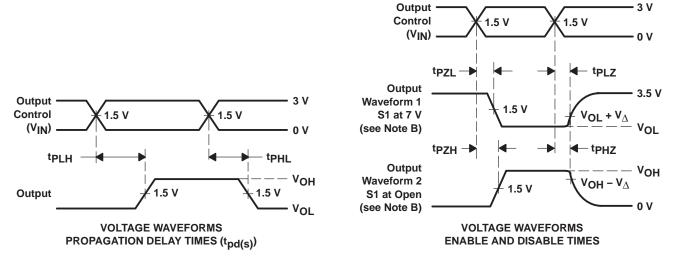
Figure 2. Transient Input Voltage (V<sub>I</sub>) and Output Voltage (V<sub>OUTU</sub>) Waveforms (Switch OFF)

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### PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	${f v}_{\!\Delta}$
<sup>t</sup> pd(s)	$\begin{array}{c} \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{4 V} \end{array}$	Open Open	<b>500</b> Ω <b>500</b> Ω	V <sub>CC</sub> or GND V <sub>CC</sub> or GND	50 pF 50 pF	
tPLZ/tPZL	5 V ± 0.5 V 4 V	7 V 7 V	<b>500</b> Ω <b>500</b> Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
tPHZ/tPZH	5 V ± 0.5 V 4 V	Open Open	<b>500</b> Ω <b>500</b> Ω	V <sub>CC</sub>	50 pF 50 pF	0.3 V 0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd(s)}$ . The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms



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### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74CBT3245CDBQR	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3245C
SN74CBT3245CDBQR.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3245C
SN74CBT3245CDBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CDBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CDGVR	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CDGVR.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CDGVRG4	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CDGVRG4.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CDW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3245C
SN74CBT3245CDW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3245C
SN74CBT3245CDWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3245C
SN74CBT3245CDWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3245C
SN74CBT3245CPW	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CPW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CPWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CPWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245C
SN74CBT3245CRGYR	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU245C
SN74CBT3245CRGYR.B	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU245C

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



# **PACKAGE OPTION ADDENDUM**

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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# TAPE AND REEL INFORMATION



# TAPE DIMENSIONS WHO WE PI WHO WE PI WHO WE BO WE Cavity AO WE Cavity AO WE Cavity

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3245CDBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3245CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74CBT3245CDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3245CDGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3245CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CBT3245CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CBT3245CRGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3245CDBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74CBT3245CDBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74CBT3245CDGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CBT3245CDGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CBT3245CDWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74CBT3245CPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74CBT3245CRGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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# **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3245CDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBT3245CDW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBT3245CPW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74CBT3245CPW.B	PW	TSSOP	20	70	530	10.2	3600	3.5





### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DBQ (R-PDSO-G20)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AD.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# DGV (R-PDSO-G\*\*)

# 24 PINS SHOWN

### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SOIC



### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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