SCDS053E - MARCH 1998 - REVISED OCTOBER 2000

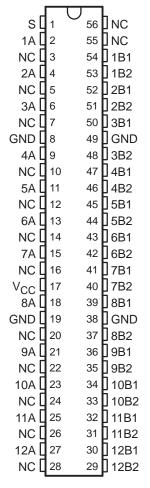
- Member of Texas Instruments' Widebus™ **Family**
- 4- Ω Switch Connection Between Two Ports
- **TTL-Compatible Control Input Levels**
- Make-Before-Break Feature
- Internal 500- Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**

description

The SN74CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and RINT is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	SSOP – DL	Tube	SN74CBT16292DL	CBT16292		
-40°C to 85°C	330F - DL	Tape and reel	SN74CBT16292DLR	CB110292		
-40°C to 85°C	TSSOP – DGG Tape and reel		SN74CBT16292DGGR	CBT16292		
	TVSOP – DGV	Tape and reel	SN74CBT16292DGVR	CY292		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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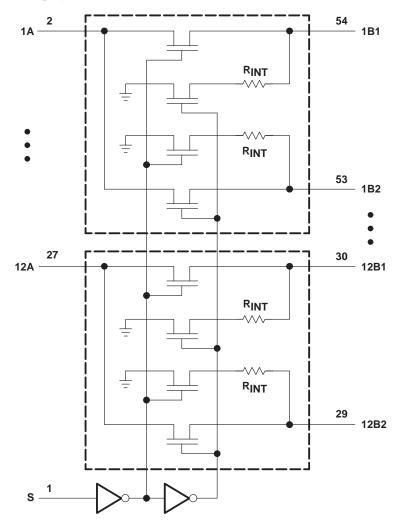
SN74CBT16292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
Н	A port = B2 port R _{INT} = B1 port

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
V _{IL}	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2	V
II		$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$ or GND				±5	μΑ
Icc		$V_{CC} = 5.5 V,$	$I_{O} = 0,$	$V_I = V_{CC}$ or GND			3	μΑ
Δlcc§	Control input	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
Ci	Control input	V _I = 3 V or 0				3		pF
Cio		$V_{CC} = 0$,	$V_O = 3 V \text{ or } 0$			8		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _I = 15 mA		10	20	
$r_{on}\P$			\/ı = 0	I _I = 64 mA		3	7	Ω
		V _{CC} = 4.5 V	V _I = 0	I _I = 30 mA		3	7	
			V _I = 2.4 V,	I _I = 15 mA		5	15	

[‡] All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^{\circ}C$.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN74CBT16292 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V	V _{CC} =	= 5 V 5 V	UNIT
	(INFOT)	(001701)	MIN MAX	MIN	MAX	
_{tpd} †	A or B	B or A	0.5		0.25	ns
t _{en}	S	A or B	6.8	1	6	ns
t _{dis}	S	A or B	7	1	6.3	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

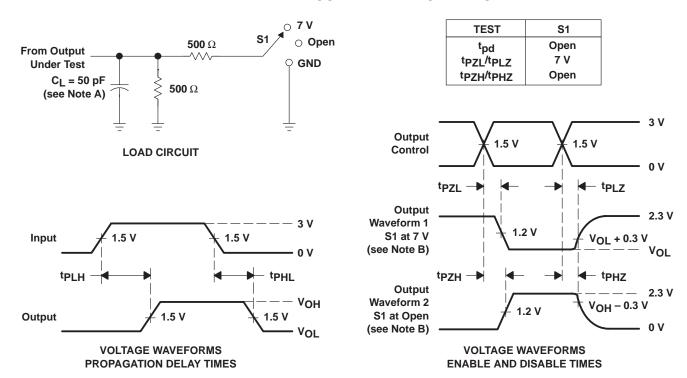
PARAMETER	DESCRIPTION	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
t _{mbb} ‡	Make-before-break time	0	2	0	2	ns

[‡] The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal $500-\Omega$ pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal $500-\Omega$ pulldown resistor.
- C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq 2.5~\text{ns}, t_f \leq 2.5~\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} . $Z = R_{INT} = 500~\Omega$
- F. tpzL and tpzH are the same as t_{en} . Z = R_{INT} = 500 Ω
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	Lead finish/ MSL rating/ Ball material Peak reflow		Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74CBT16292DGGR	NRND	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DGGR.A	NRND	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DGVR	NRND	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY292
SN74CBT16292DGVR.A	NRND	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY292
SN74CBT16292DL	NRND	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DL.A	NRND	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DLR	NRND	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DLR.A	NRND	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16292DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CBT16292DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CBT16292DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16292DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74CBT16292DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CBT16292DLR	SSOP	DL	56	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

ĺ	Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ĺ	SN74CBT16292DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
ĺ	SN74CBT16292DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194







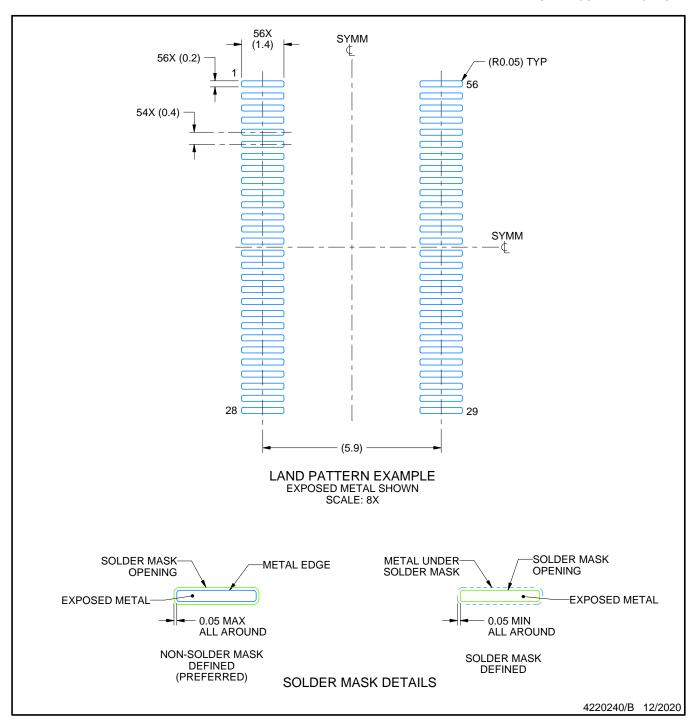
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-194.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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