SCDS139 - OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- Undershoot Protection for Off-Isolation on A and B Ports Up to -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on})
 Characteristics (r_{on} = 3 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C_{io(OFF)} = 5.5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 3 μA Max)
- V_{CC} Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

NC 48 1 1 OE 47 🛮 1A1 1B1 🛚 1B2 3 46 1 1A2 GND 4 45 | GND 44 🛛 1A3 1B3 🛮 5 1B4 🛮 6 43 1A4 V_{CC} **□** 7 42 V_{CC} 41 1 1A5 1B5 | 8 40 🛮 1A6 1B6 📙 9 GND [] 10 39 GND 38 🛮 1A7 1B7 🛮 11 37 1A8 1B8 🛮 12 2B1 ∏ 13 36 T 2A1 2B2 14 35 2A2 GND [] 15 34 GND 2B3 16 33 2A3 2B4 🛮 17 32 2A4 31 V_{CC} 18 V_{CC} $\cup{4}$ 2B5 🛮 19 30 2A5 29 2A6 2B6 20 GND [] 21 28 GND

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

NC - No internal connection

27 2A7

26 2A8

25 20E

2B7 22

2B8 [] 23

NC 24

description/ordering information

ORDERING INFORMATION

TA	PACK	AGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	0000 01	Tube SN74CBT16245CDL		ODT400450	
	SSOP – DL	Tape and reel	SN74CBT16245CDLR	CBT16245C	
	TOCOD DOC	Tube	SN74CBT16245CDGG	CBT16245C	
	TSSOP - DGG	Tape and reel	SN74CBT16245CDGGR	CB1 16245C	
	TVSOP - DGV	Tape and reel	SN74CBT16245CDGVR	CY245C	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information (continued)

The SN74CBT16245C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16245C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16245C is organized as two 8-bit bus switches with separate output-enable $(1\overline{OE}, 2\overline{OE})$ inputs. It can be used as two 8-bit bus switches or as one 16-bit bus switch. When \overline{OE} is low, the associated 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 8-bit bus switch is OFF and the high-impedance state exists between the A and B ports.

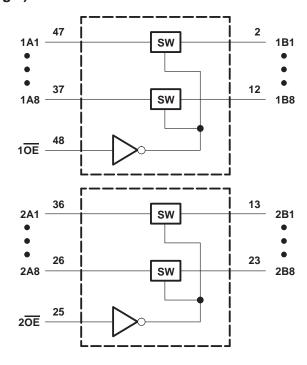
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE (each 8-bit bus switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect

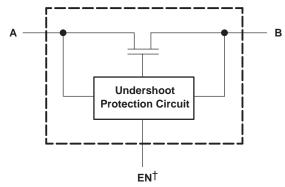
logic diagram (positive logic)





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simplified schematic, each FET switch (SW)



[†] EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	–0.5 V to 7 V
Control input voltage range, V _{IN} (see Notes 1 and 2)	0.5 V to 7 V
Switch I/O voltage range, V _{I/O} (see Notes 1, 2, and 3)	0.5 V to 7 V
Control input clamp current, I _{IK} (V _{IN} < 0)	–50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	–50 mA
ON-state switch current, I _{I/O} (see Note 4)	±128 mA
Continuous current through V _{CC} or GND terminals	±100 mA
Package thermal impedance, θ _{JA} (see Note 5): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T _{stq}	. −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
 - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 - 4. II and IO are used to denote specific conditions for II/O.
 - 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2	5.5	V
VIL	Low-level control input voltage	0	8.0	V
V _{I/O}	Data input/output voltage	0	5.5	V
TA	Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITIO	NS	MIN	TYP [†]	MAX	UNIT
VIK	Control inputs	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$				-1.8	V
VIKU	Data inputs	V _{CC} = 5 V,	$0 \text{ mA} > I_{I} \ge -50 \text{ mA},$ $V_{IN} = V_{CC} \text{ or GND},$	Switch OFF			-2	V
I _{IN}	Control inputs	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$ or GND				±1	μΑ
I _{OZ} ‡		V _{CC} = 5.5 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V _{IN} = V _{CC} or GND			±10	μА
l _{off}		$V_{CC} = 0$,	$V_{O} = 0 \text{ to } 5.5 \text{ V},$	V _I = 0				μΑ
ICC		V _{CC} = 5.5 V,	$I_{I/O} = 0,$ $V_{IN} = V_{CC} \text{ or GND},$	Switch ON or OFF			3	μΑ
∆lcc§	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
C _{in}	Control inputs	$V_{IN} = 3 V \text{ or } 0$				3.5		pF
C _{io(OFF)})	$V_{I/O} = 3 \text{ V or } 0,$	Switch OFF,	$V_{IN} = V_{CC}$ or GND		5.5		pF
C _{io(ON)}		$V_{I/O} = 3 \text{ V or } 0,$	Switch ON,	V _{IN} = V _{CC} or GND		14		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _O = -15 mA		8	12	
r_{on} ¶				I _O = 64 mA		3	6	Ω
o		V _{CC} = 4.5 V	V _I = 0	I _O = 30 mA		3	6	
			V _I = 2.4 V,	$I_{O} = -15 \text{ mA}$		5	10	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V	V _{CC} =	= 5 V 5 V	UNIT
	(INPOT)	(001701)	MIN MAX	MIN	MAX	
t _{pd} #	A or B	B or A	0.24		0.15	ns
t _{en}	ŌE	A or B	5.4	1.5	5	ns
t _{dis}	ŌĒ	A or B	5.6	1.5	5.6	ns

[#]The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



 V_{IN} and I_{IN} refer to control inputs. V_{I} , V_{O} , I_{I} , and I_{O} refer to data pins. † All typical values are at V_{CC} = 5 V (unless otherwise noted), T_{A} = 25°C.

For I/O ports, the parameter IOZ includes the input leakage current.

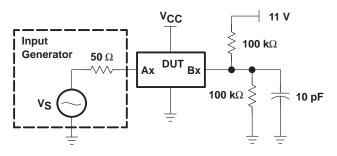
[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶]Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

undershoot characteristics (see Figures 1 and 2)

PARAMETER		TEST CONDITIONS				MAX	UNIT
Voutu	$V_{CC} = 5.5 \text{ V},$	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	V _{OH} -0.3		V

 $[\]dagger$ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.





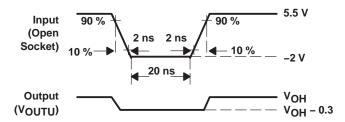
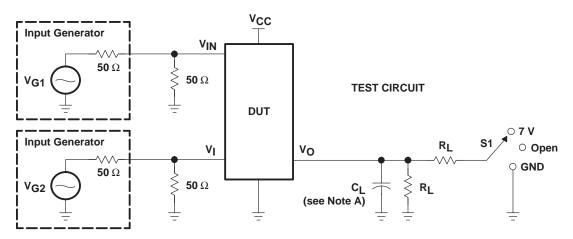
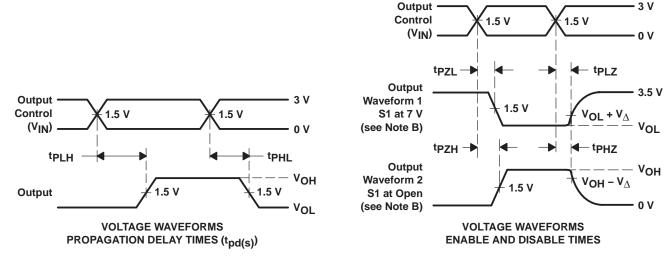


Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	${f v}_{\Delta}$
^t pd(s)	$\begin{array}{c} \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{4 V} \end{array}$	Open Open	500 Ω 500 Ω	V _{CC} or GND V _{CC} or GND	50 pF 50 pF	
tPLZ/tPZL	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
tPHZ/tPZH	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V _{CC}	50 pF 50 pF	0.3 V 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
74CBT16245CDGVRG4	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY245C
74CBT16245CDGVRG4.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY245C
SN74CBT16245CDGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16245C
SN74CBT16245CDGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16245C
SN74CBT16245CDGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY245C
SN74CBT16245CDGVR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY245C
SN74CBT16245CDL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16245C
SN74CBT16245CDL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16245C
SN74CBT16245CDLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16245C
SN74CBT16245CDLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16245C

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBT16245CDGVRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CBT16245CDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74CBT16245CDGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CBT16245CDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBT16245CDGVRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74CBT16245CDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74CBT16245CDGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74CBT16245CDLR	SSOP	DL	48	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT16245CDL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74CBT16245CDL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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