SCDS031I - MAY 1996 - REVISED OCTOBER 2000

- Members of Texas Instruments' Widebus™
 Family
- Standard '16244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

SN54CBT16244 . . . WD PACKAGE SN74CBT16244 . . . DGG, DGV, OR DL PACKAGE (TOP VIEW)

	_			
10E	1	U	48	2 <mark>0E</mark>
1B1 [2		47] 1A1
1B2	3		46] 1A2
GND [4		45	GND
1B3 [5		44	1A3
1B4 [6		43] 1A4
v _{cc} [7		42] v _{cc}
2B1	8		41	2A1
2B2	9		40	2A2
GND [10		39	GND
2B3 [11		38	2A3
2B4 [12		37	2A4
3B1 [13		36	3A1
3B2	14		35	3A2
GND [15		34	GND
3B3 [16		33	3A3
3B4 [17		32	3A4
v _{cc} [18		31] v _{cc}
4B1 [19		30] 4A1
4B2	20		29	4A2
GND [21		28	GND
4B3 [22		27] 4A3
4B4 [23		26] 4A4
40E	24		25	3 <u>OE</u>

ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	SSOP – DL	Tube	SN74CBT16244DL	CBT16244		
-40°C to 85°C	330F - DL	Tape and reel	SN74CBT16244DLR	CD110244		
-40 C to 65 C	TSSOP – DGG	Tape and reel	SN74CBT16244DGGR	CBT16244		
	TVSOP – DGV	Tape and reel	SN74CBT16244DGVR	CY244		
–55°C to 125°C	CFP – WD	Tube	SNJ54CBT16244WD	SNJ54CBT16244WD		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 4-bit bus switch)

INPUT OE	OUTPUTS A, B
L	A port = B port
Н	Disconnect

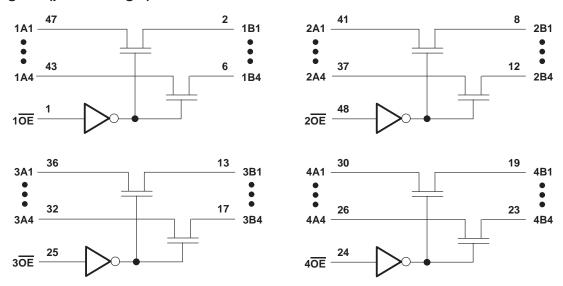


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

11,	
	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ _{JA} (see Note 2): DG0	G package 70°C/W
DG\	/ package 58°C/W
DL p	package 63°C/W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 3)

		SN54CB	Г16244	SN74CB	T16244	UNIT	
		MIN	MAX	MIN	MAX	ONIT	
Vcc	Supply voltage	4	5.5	4	5.5	V	
VIH	High-level control input voltage	2		2		V	
VIL	Low-level control input voltage		0.8		0.8	V	
TA	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA	METED	TEST COM	DITIONS	П	SN5	4CBT16	244	SN7	4CBT16	244	UNIT	
PAKAI	METER	TEST CON	DITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII	
VIK		I _I = -18 mA				-1.2			-1.2	V		
1.		VCC = 0	V _I = 5.5 V			10			10	μА		
ł _I		V _{CC} = 5.5 V	V _I = 5.5 V or GND				±1			±1	μΑ	
lcc		V _{CC} = 5.5 V, V _I = V _{CC} or GND	I _O = 0,				3.2			3	μΑ	
∆lcc‡	Control inputs	V _{CC} = 5.5 V, Other inputs at V _{CC} or GND	One input at 3.4 V,				2.5			2.5	mA	
Ci	Control inputs	V _I = 3 V or 0				2.5			2.5		pF	
C _{io(OFF}	=)	$V_O = 3 V \text{ or } 0,$	OE = VCC			4.5			4.5		pF	
		$V_{CC} = 4 V$,	$V_{I} = 2.4 \text{ V}, \qquad I_{I} = 15 \text{ n}$	Α			20			20		
r _{on} §			$V_{I} = 0,$ $I_{I} = 64 \text{ n}$	Α		5	10		5	7	Ω	
ons		V _{CC} = 4.5 V	$V_{I} = 0$, $I_{I} = 30 \text{ n}$	Α		5	10		5	7	52	
			V _I = 2.4 V, I _I = 15 n	Α		8	14		8	12		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	;	SN54CB	T16244		SN74CBT16244				
PARAMETER	FROM (INPUT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A				0.8*		0.35		0.25	ns
t _{en}	ŌĒ	A or B		10.3	1	9.2		5.5	1	5.1	ns
^t dis	ŌĒ	A or B		9.7	1	8.2		5.2	1	5.4	ns

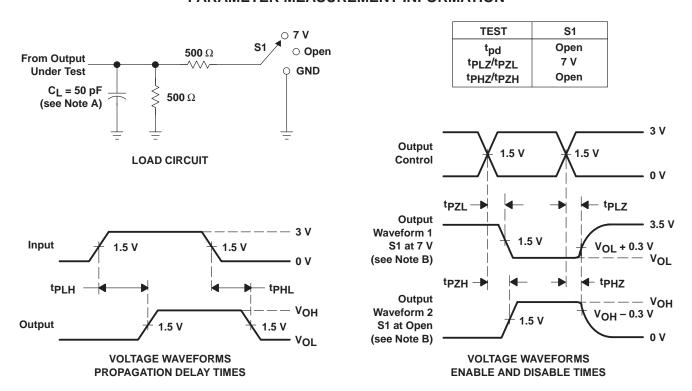
^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(.,	(=)			(0)	(4)	(5)		(0)
SN74CBT16244DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244
SN74CBT16244DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244
SN74CBT16244DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244
SN74CBT16244DL.A	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244
SN74CBT16244DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244
SN74CBT16244DLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74CBT16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74CBT16244DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0	
SN74CBT16244DLR	SSOP	DL	48	1000	356.0	356.0	53.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

	Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
	SN74CBT16244DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
Г	SN74CBT16244DL.A	DL	SSOP	48	25	473.7	14.24	5110	7.87



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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Last updated 10/2025