- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

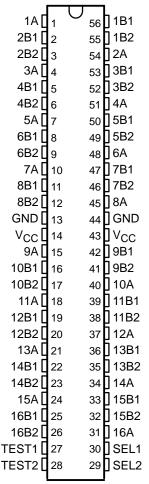
### description

The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

This device is designed so it does not have through current when switching directions.

# DGG, DGV, OR DL PACKAGE (TOP VIEW)



#### ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74CBT16233DL	CBT16233
-40°C to 85°C	330F - DL	Tape and reel	SN74CBT16233DLR	CB1 16233
-40 C to 65 C	TSSOP – DGG	Tape and reel	SN74CBT16233DGGR	CBT16233
	TVSOP – DGV	Tape and reel	SN74CBT16233DGVR	CY233

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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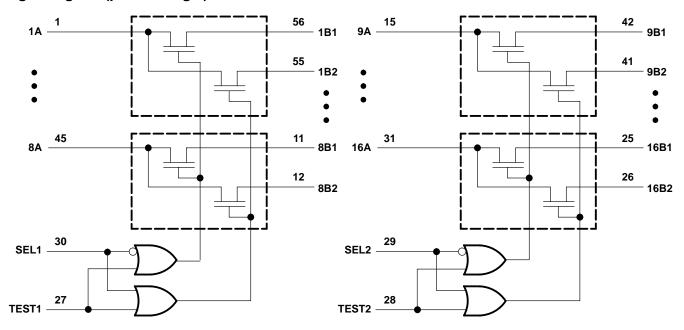
Widebus is a trademark of Texas Instruments.



# FUNCTION TABLE (each multiplexer/demultiplexer)

INP	UTS	FUNCTION
SEL	TEST	FUNCTION
L	L	A = B1
Н	L	A = B2
Х	Н	A = B1 and A = B2

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		$5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Continuous channel current		128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2):	): DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T <sub>stq</sub>		−65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



# recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.25	V
VIH	High-level control input voltage	2		V
V <sub>IL</sub>	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITI	MIN	TYP <sup>†</sup>	MAX	UNIT	
VIK		$V_{CC} = 4.75 \text{ V},$	I <sub>I</sub> = -18 mA				-1.2	V
1.		$V_{CC} = 0$ ,	V <sub>I</sub> = 5.25 V				10	μΑ
'		$V_{CC} = 5.25 \text{ V},$	V <sub>I</sub> = 5.25 V or GND				±1	μΑ
ICC VCC		$V_{CC} = 5.25 \text{ V},$	I <sub>O</sub> = 0,	$V_I = V_{CC}$ or GND			3	μΑ
∆lcc <sup>‡</sup>	Control inputs	$V_{CC} = 5.25 \text{ V},$	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			2.5	mA
Ci	Control inputs	V <sub>I</sub> = 3 V or 0				4.5		pF
C <sub>io(OFF)</sub>		$V_O = 3 \text{ V or } 0$				4		pF
			\/ı = 0	I <sub>I</sub> = 64 mA		5	7	
r <sub>on</sub> §		V <sub>CC</sub> = 4.75 V	V <sub>I</sub> = 0	I <sub>I</sub> = 30 mA		5	7	Ω
			$V_1 = 2.4 V,$	I <sub>I</sub> = 15 mA		7	12	

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

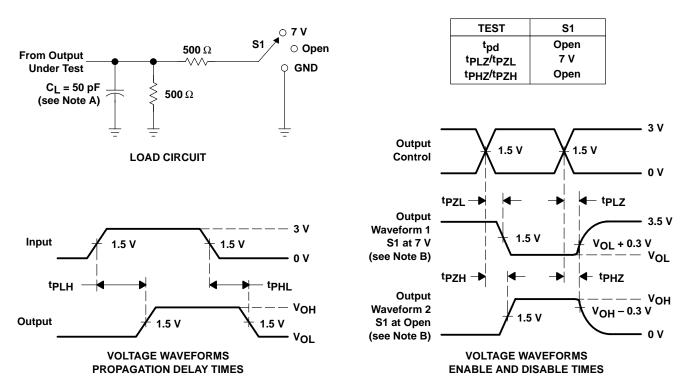
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> ¶	A or B	B or A		0.25	ns
<sup>t</sup> pd	SEL	А	1.6	5.3	ns
<sup>t</sup> en	TEST or SEL	В	1.3	5.2	ns
<sup>t</sup> dis	TEST or SEL	В	1	5.3	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

<sup>&</sup>lt;sup>‡</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

<sup>§</sup> Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74CBT16233DGGR	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DGGR.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DGGRG4	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DGGRG4.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DGVR	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY233
SN74CBT16233DGVR.B	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY233
SN74CBT16233DGVRG4	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY233
SN74CBT16233DGVRG4.B	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY233
SN74CBT16233DL	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DL.B	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DLR	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233
SN74CBT16233DLR.B	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16233

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# PACKAGE OPTION ADDENDUM

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# **PACKAGE MATERIALS INFORMATION**

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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16233DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CBT16233DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CBT16233DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CBT16233DGVRG4	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CBT16233DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



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# \*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74CBT16233DGGR	TSSOP	DGG	56	2000	356.0	356.0	41.0	
SN74CBT16233DGGRG4	TSSOP DGG		56	2000	356.0	356.0	45.0	
SN74CBT16233DGVR	TVSOP	TVSOP	DGV	56	2000	356.0	356.0 356.0	45.0
SN74CBT16233DGVRG4	TVSOP	DGV	56	2000	356.0	356.0	45.0	
SN74CBT16233DLR	SSOP	DL	56	1000	356.0	356.0	53.0	

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

# **TUBE**



## \*All dimensions are nominal

Ì	Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ĺ	SN74CBT16233DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
ĺ	SN74CBT16233DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

# DGV (R-PDSO-G\*\*)

## **24 PINS SHOWN**

## **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194







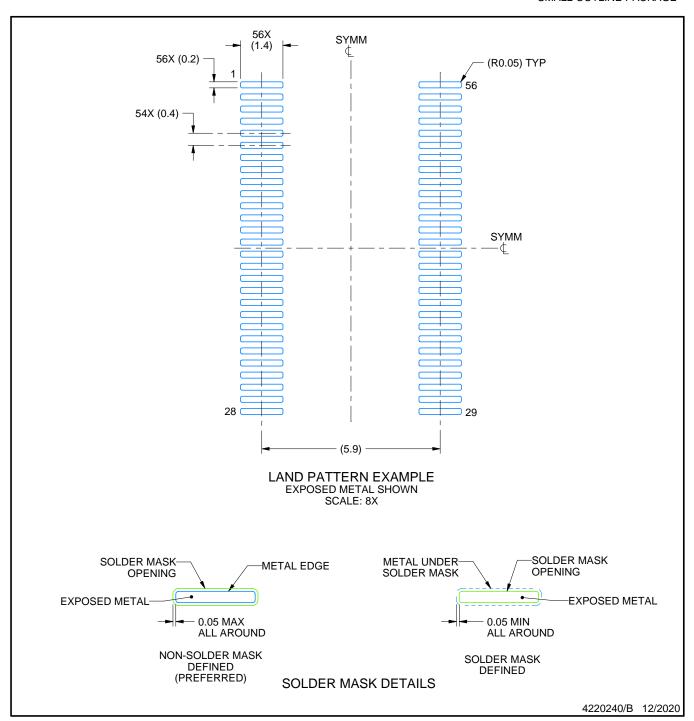
### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-194.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# DL (R-PDSO-G56)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-153.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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