

FEATURES

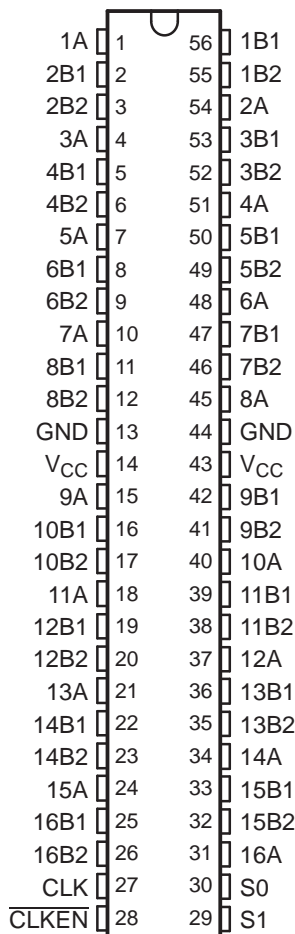
- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels

DESCRIPTION/ ORDERING INFORMATION

The SN74CBT16232 is a synchronous 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path.

Two select (S0 and S1) inputs control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.

DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16232DL	CBT16232
		Tape and reel	SN74CBT16232DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16232DGGR	CBT16232

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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SN74CBT16232

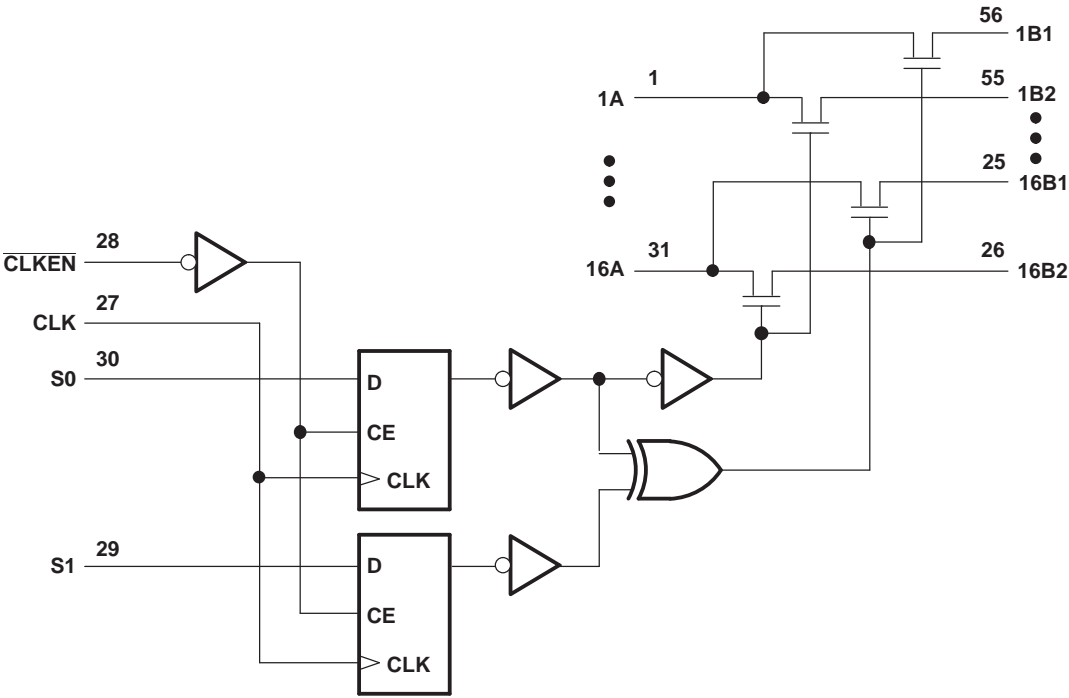
SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009N—MAY 1995—REVISED JUNE 2007

FUNCTION TABLE

INPUTS				FUNCTION
S1	S0	CLK	CLKEN	
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
	Continuous channel current		128	mA
I _{IK}	Input clamp current		-50	mA
		V _I < 0		
θ _{JA}	Package thermal impedance ⁽³⁾		64	°C/W
			56	
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
T _A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA				−1.2	V
I _I		V _{CC} = 5.5 V, V _I = 5.5 V or GND				±1	μA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND				3	μA
ΔI _{CC} ⁽²⁾	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				2.5	mA
C _I	Control inputs	V _I = 3 V or 0			4.5		pF
C _{io(OFF)}	A port	V _O = 3 V or 0, $\overline{\text{CLKEN}}$ = 0, S0 and S1 = GND			6.5		pF
	B port				4		
r _{on} ⁽³⁾	V _{CC} = 4 V, TYP at V _{CC} = 4 V		V _I = 2.4 V, I _I = 15 mA		14	20	Ω
			V _I = 0		I _I = 64 mA	5	
	V _I = 2.4 V, I _I = 15 mA				I _I = 30 mA	5	
						10	

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

(2) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC} = 4 V		V _{CC} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			150		150	MHz
t _w	Pulse duration	CLK high or low	3.3		3.3		ns
t _{su}	Setup time	S0, S1 before CLK↑	2.2		1.9		ns
		$\overline{\text{CLKEN}}$ before CLK↑	2.4		1.9		
t _h	Hold time	S0, S1 after CLK↑	0.5		1		ns
		$\overline{\text{CLKEN}}$ after CLK↑	1.9		1.8		

SN74CBT16232

SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009N—MAY 1995—REVISED JUNE 2007

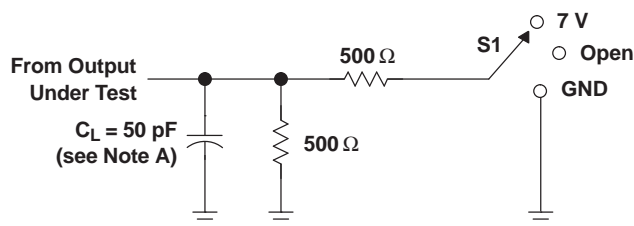
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

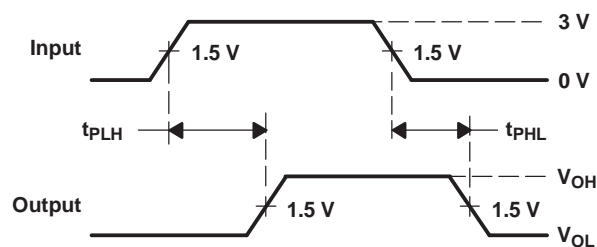
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
t _{pd} ⁽¹⁾	A or B	B or A		0.35		0.25	ns
t _{pd}	CLK	A or B		6.7	2	5.8	ns
t _{en}	CLK	A, B1, B2		7.2	1.8	6.2	ns
		B1 and B2		8.5	3.1	7.9	
t _{dis}	CLK	A or B		6.3	1.9	6.2	ns

- (1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

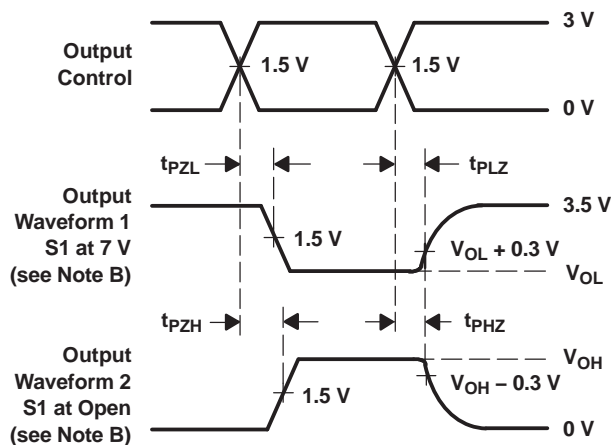


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT16232DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16232
SN74CBT16232DGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16232
SN74CBT16232DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16232
SN74CBT16232DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16232
SN74CBT16232DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16232
SN74CBT16232DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16232

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16232DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CBT16232DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16232DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CBT16232DLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE

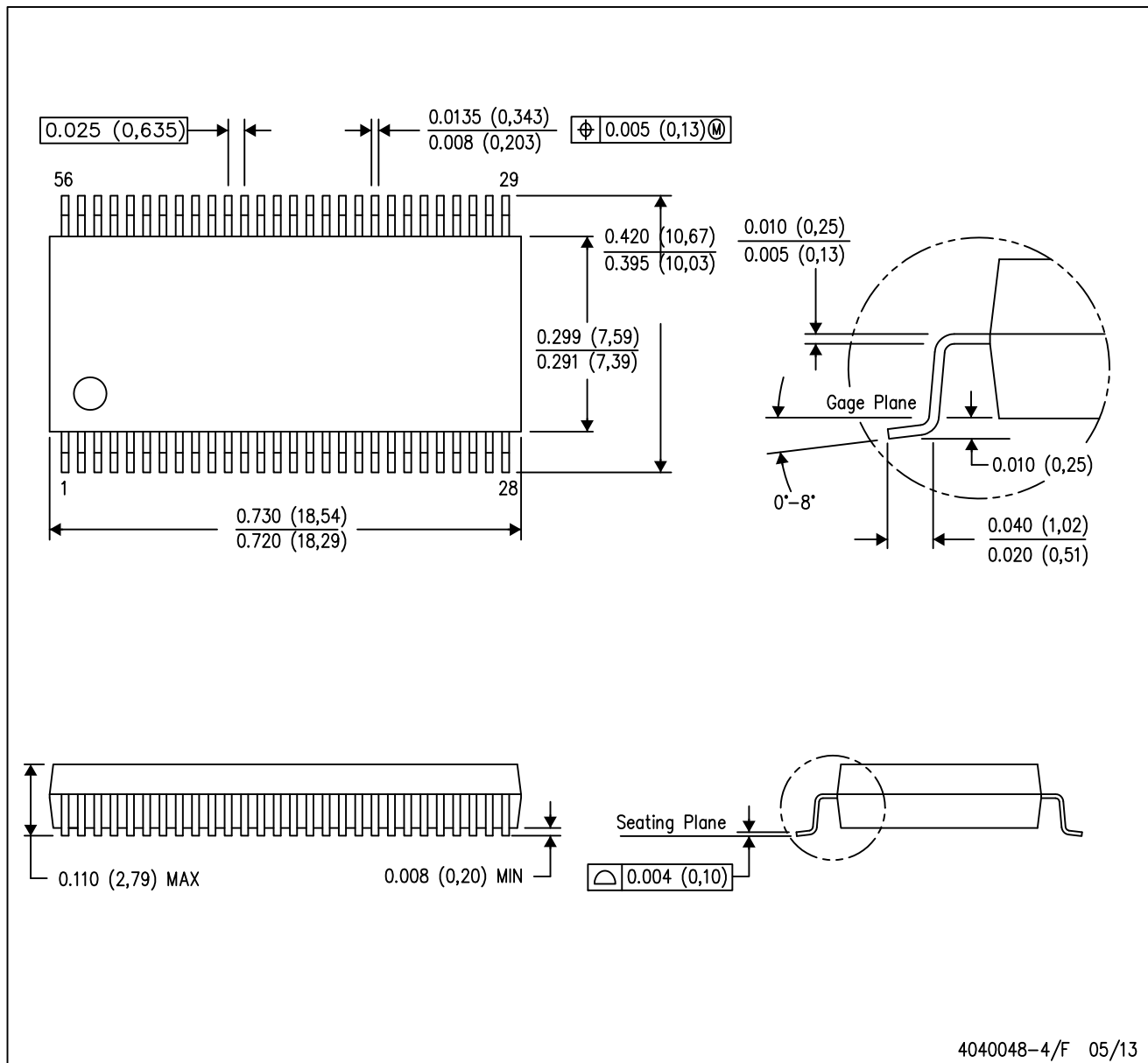


*All dimensions are nominal

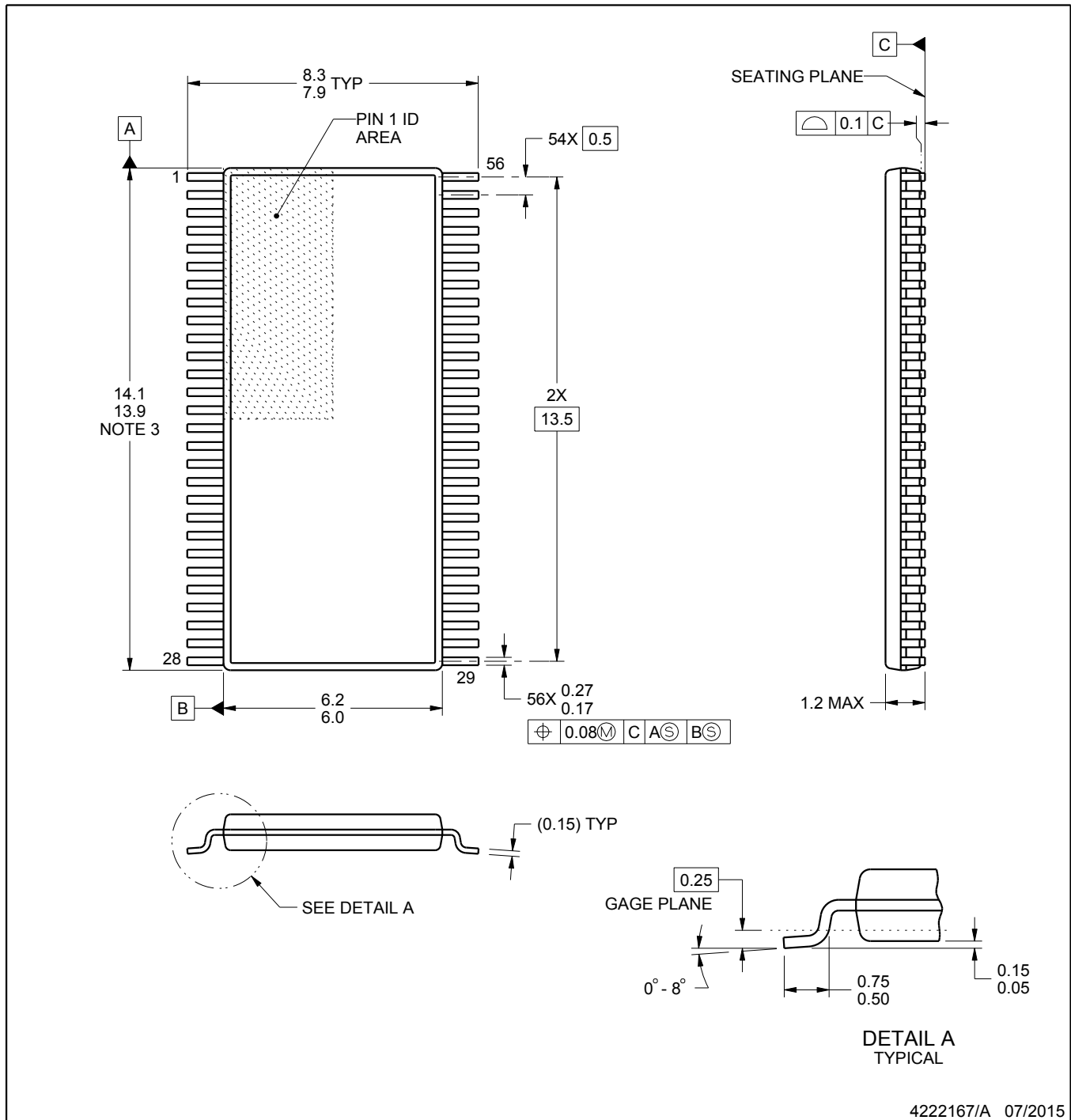
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT16232DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74CBT16232DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



4222167/A 07/2015

NOTES:

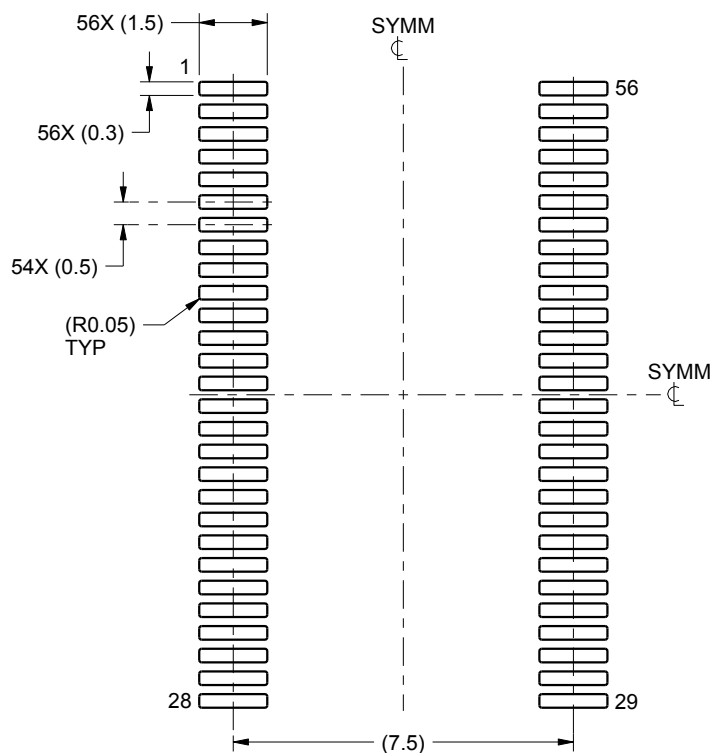
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

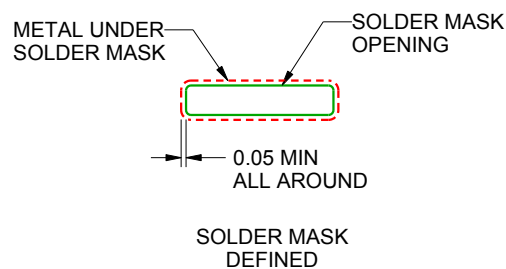
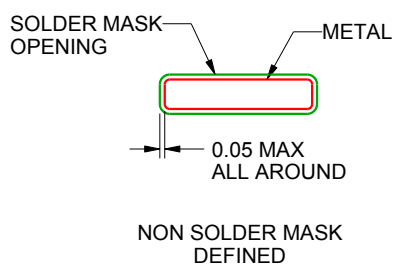
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

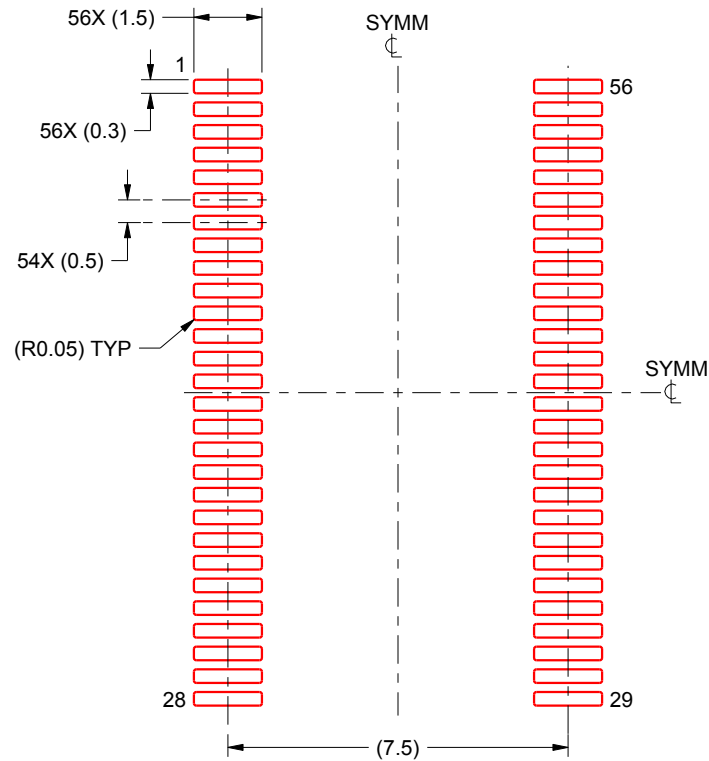
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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