SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007U - NOVEMBER 1992 - REVISED JUNE 2005

- Members of the Texas Instruments
 Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 200-V Machine Model (A115-A)

description/ordering information

The 'CBT16212A devices provide 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Each device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

SN54CBT16212A . . . WD PACKAGE SN74CBT16212A . . . DGG, DGV, OR DL PACKAGE (TOP VIEW)

			1
S0 [1	56] S1
1A1 [2	55] S2
1A2 [3	54] 1B1
2A1 [4	53] 1B2
2A2 [5	52] 2B1
3A1 [6	51] 2B2
3A2[7	50] 3B1
GND [8	49] GND
4A1 [9	48] 3B2
4A2 [10	47] 4B1
5A1 [11	46] 4B2
5A2 [12	45] 5B1
6A1 [13	44] 5B2
6A2[14	43] 6B1
7A1 [15	42] 6B2
7A2 [16	41] 7B1
v _{cc} [17	40] 7B2
8A1 [18	39] 8B1
GND[19	38] GND
8A2 [20	37] 8B2
9A1 [21	36] 9B1
9A2 [22	35] 9B2
10A1 [23	34] 10B1
10A2[24	33] 10B2
11A1 [25	32] 11B1
11A2 [26	31] 11B2
12A1 [27	30] 12B1
12A2 [28	29	12B2

ORDERING INFORMATION

TA	PACKAGE	†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	0000 01	Tube	SN74CBT16212ADL	ODT400404	
4000 / 0500	SSOP - DL	Tape and reel	SN74CBT16212ADLR	CBT16212A	
	TSSOP - DGG	Tape and reel	SN74CBT16212ADGGR	CBT16212A	
-40°C to 85°C	TVSOP - DGV	Tape and reel	SN74CBT16212ADGVR	CY212A	
	VFBGA – GQL	Town and made	SN74CBT16212AGQLR	0)/0404	
	VFBGA – ZQL (Pb-free)	BGA – ZQL (Pb-free)		CY212A	
–55°C to 125°C	CFP – WD	Tube	SNJ54CBT16212AWD	SNJ54CBT16212AWD	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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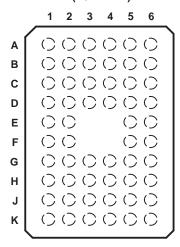
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GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

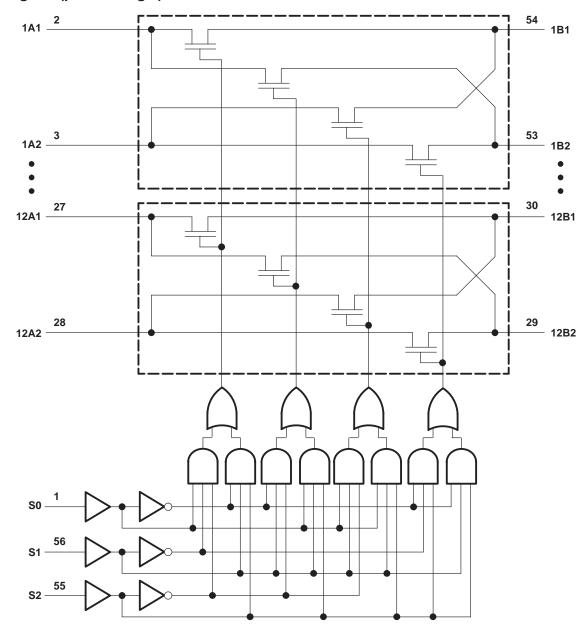
	1	2	3	4	5	6
Α	1A2	1A1	S0	S1	S2	1B1
В	3A1	2A2	2A1	1B2	2B1	2B2
С	4A1	GND	3A2	3B1	GND	3B2
D	5A2	4A2	5A1	4B2	4B1	5B1
Е	6A2	6A1			5B2	6B1
F	7A1	7A2			7B1	6B2
G	Vcc	GND	8A1	8B1	GND	7B2
Н	8A2	9A1	9A2	9B2	9B1	8B2
J	10A1	10A2	11A1	11B1	10B2	10B1
K	11A2	12A1	12A2	12B2	12B1	11B2

FUNCTION TABLE

	INPUTS		INPUTS/0	OUTPUTS	FUNCTION
S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	Н	B1 port	Z	A1 port = B1 port
L	Н	L	B2 port	Z	A1 port = B2 port
L	Н	Н	Z B1 port		A2 port = B1 port
Н	L	L	Z	B2 port	A2 port = B2 port
Н	L	Н	Z	Z	Disconnect
Н	Н	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
Н	Н	Н	B2 port	B1 port	A1 port = B2 port A2 port = B1 port



logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		-0.5	\mbox{V} to 7 \mbox{V}
Input voltage range, V _I (see Note 1)		-0.5	\mbox{V} to 7 \mbox{V}
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			-50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		64°C/W
	DGV package		48°C/W
	DL package		56°C/W
	GQL/ZQL package		42°C/W
Storage temperature range, T _{sta}		65°C 1	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		SN54CBT	16212A	SN74CBT		
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	4	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-			CONDITIONS		SN54	SN54CBT16212A			CBT162	12A	
PAI	RAMETER	IEST	CONDITIONS	•	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 0$,	V _I = 5.5 V			10			10		
1 ₁		$V_{CC} = 5.5 V,$	V _I = 5.5 V or			±1			±1	μΑ	
ICC		$V_{CC} = 5.5 V,$	I _O = 0, V _I =			3.2			3	μΑ	
ΔICC§	Control inputs	V _{CC} = 5.5 V, One inp Other inputs at V _{CC} of			2.5			2.5	mA		
Ci	Control inputs	V _I = 3 V or 0				2.5			2.5		pF
C _{io(off)}		$V_0 = 3 \text{ V or } 0,$	S0, S1, and	S2 = GND		7.5			7.5		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _I = 15 mA		14	20		14	20	
r _{on} ¶	r _{on} ¶ V _{CC} = 4.5 V		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	I _I = 64 mA		4	10		4	7	Ω
			$V_I = 0$ $I_I = 30 \text{ mA}$			4	10		4	7	
			$V_{I} = 2.4 V$,	I _I = 15 mA		6	14		6	12	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

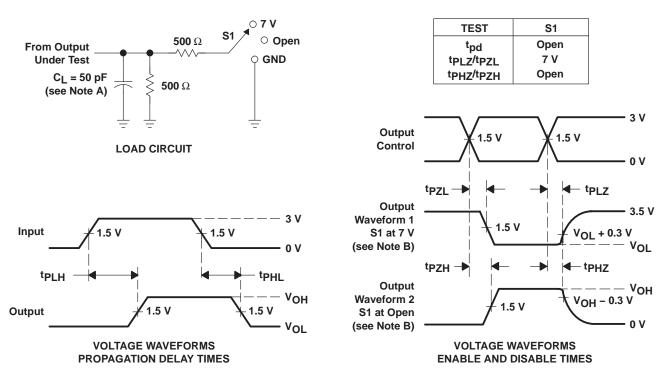
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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	S	N54CB	T16212A	ı	SN74CBT16212A				
PARAMETER	FROM (INPUT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A				0.8*		0.35		0.25	ns
^t pd	S	A or B		14	1.5	13		10	1.5	9.1	ns
t _{en}	S	A or B		15	1.5	13.7		10.4	1.5	9.7	ns
t _{dis}	S	A or B		14.2	1.5	13.5		9.2	1.5	8.8	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74CBT16212ADGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212A
SN74CBT16212ADGGR.A	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212A
SN74CBT16212ADL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212A
SN74CBT16212ADL.A	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212A
SN74CBT16212ADLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212A
SN74CBT16212ADLR.A	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212A

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16212ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CBT16212ADLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16212ADGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74CBT16212ADLR	SSOP	DL	56	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT16212ADL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74CBT16212ADL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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