SN74CB3T3253 Dual 1-of-4 FET Multiplexer/Demutiplexer 2.5V/3.3V Low-voltage Bus Switch With 5V Tolerant Level Shifter

1 Features

- Output voltage translation tracks V_{CC}
- Supports mixed-mode signal operation on all data I/O ports
  - 5V input down to 3.3V output level shift with 3.3V V_{CC}
  - 5V/3.3V input down to 2.5V output level shift with 2.5V V_{CC}
- 5V tolerant I/Os with device powered up or powered down
- Bidirectional data flow with near-zero propagation delay
- Low ON-state resistance (r_{on}) characteristics (r_{on} = 5Ω typ)
- Low input/output capacitance minimizes loading ($C_{io(OFF)}$ = 5pF typ)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (I_{CC} = 20µA max)
- V_{CC} operating range from 2.3V to 3.6V
- Data I/Os support 0V to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control inputs can be driven by TTL or 5V/3.3V CMOS outputs
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250mA per JESD 17
- ESD performance tested per JESD 22
  - 2000V human-body model (A114-B, Class II)
  - 1000V charged-device model (C101)

2 Applications

- Supports digital applications:
  - Level translation
  - USB interface
  - Memory interleaving
  - Bus isolation
- Designed for low-power portable equipment

3 Description

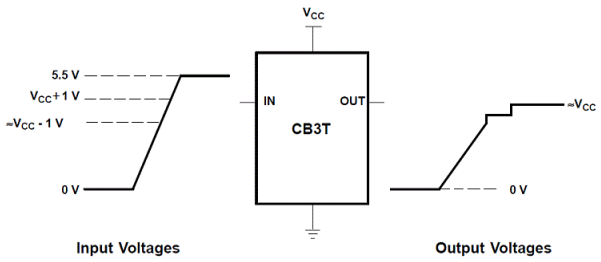
The SN74CB3T3253 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3253 supports systems using 5V TTL, 3.3V LVTTL, and 2.5V CMOS switching standards, as well as user-defined switching levels (see Typical DC Voltage-Translation Characteristics).

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature establishes that damaging current does not backflow through the device when it is powered down. The device has isolation during power off.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
SN74CB3T3253D	D (SOIC, 16)	9.9mm × 6mm
SN74CB3T3253DBQ	DBQ (SSOP, 16)	4.9mm × 6mm
SN74CB3T3253DGV	DGV (TVSO, 16)	3.60mm × 6.mm
SN74CB3T3253PW	PW (TSSOP, 16)	5mm × 6.4mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



If the input high voltage (V_{IH}) level is greater than or equal to V_{CC}+ 1V, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Typical DC Voltage-Translation Characteristics

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4 Pin Configuration and Functions

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)

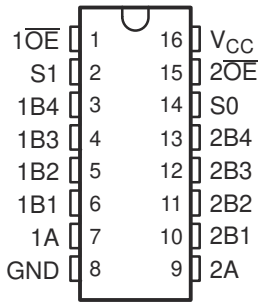


Figure 4-1. D, DBQ, DGV, or PW Package 16-Pin SOIC, SSOP, TVSOP, or TSSOP Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1 $\overline{OE}$	1	I	Output Enable 1 Active-Low
S1	2	I	Select Pin 1
1B4	3	I/O	Channel 1 I/O 4
1B3	4	I/O	Channel 1 I/O 3
1B2	5	I/O	Channel 1 I/O 2
1B1	6	I/O	Channel 1 I/O 1
1A	7	I/O	Channel 1 common
GND	8	—	Ground
2A	9	I/O	Channel 2 common
2B1	10	I/O	Channel 2 I/O 1
2B2	11	I/O	Channel 2 I/O 2
2B3	12	I/O	Channel 2 I/O 3
2B4	13	I/O	Channel 2 I/O 4
S0	14	I	Select Pin 0
2 $\overline{OE}$	15	I	Output Enable 2 Active-Low
V_{CC}	16	—	Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	7	V
V_{IN}	Control input voltage range(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	D package		73	°C/W
		DBQ package		90	
		DGV package		120	
		PW package		108	
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.

5.4 Thermal Information

THERMAL METRIC(1)		SN74CB3T3253				UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	90	120	129.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Over operating free-air temperature range

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
		V_{CC} V	**$V_{I/o}$ V or Ii or VIN**	**I_O mA or Vo or VIN**	**T_A**				
r_{ON}	ON-state switch resistance	2.3, TYP at 2.5V	V_I = 0 V	I_O = 24 mA	–40°C to +85°C		5	8	Ω
r_{ON}	ON-state switch resistance	2.3, TYP at 2.5V	V_I = 0 V	I_O = 16 mA	–40°C to +85°C		5	8	Ω
r_{ON}	ON-state switch resistance	3, TYP at 3.3V	V_I = 0 V	I_O = 64 mA	–40°C to +85°C		5	7	Ω
r_{ON}	ON-state switch resistance	3, TYP at 3.3V	V_I = 0 V	I_O = 32 mA	–40°C to +85°C		5	7	Ω
Ioff	Power down switch leakage current	0	V_I = 0 V	0 ≤ V_O ≤ 5.5 V	–40°C to +85°C	-10		10	µA
Ioz	Switch OFF leakage current	3.6	V_I = 0 V, Vin = Vcc or GND	0 ≤ V_O ≤ 5.5 V	–40°C to +85°C	-10		10	µA
II	ON-state switch leakage current	3.6	V_I = Vcc-0.7 to 5.5V	V_{IN} = V_{CC} or GND	–40°C to +85°C	-20		20	µA
II	ON-state switch leakage current	3.6	V_I = 0.7 to Vcc-0.7	V_{IN} = V_{CC} or GND	–40°C to +85°C			-40	µA
I_{II}	ON-state switch leakage current	3.6	V_I = 0 to 0.7V	V_{IN} = V_{CC} or GND	–40°C to +85°C	-5		5	µA
I_{IN}	Control input current	3.6	Vcc ≤ V_{IN} ≤ 5.5 or Vin = 0V		–40°C to +85°C	-10		10	µA
I_{CC}	Supply current	3.6	V_I = Vcc or GND, Ii/o = 0	V_{IN} = V_{CC} or GND	–40°C to +85°C			20	µA
I_{CC}	Supply current	3.6	V_I = 5.5V, Ii/o = 0	V_{IN} = V_{CC} or GND	–40°C to +85°C			20	µA
ΔI_{CC}	Quiescent Device Current w.r.t Control inputs	3 to 3.6V	V_{IN} = Vcc - 0.6V	Other inputs at 0/VCC	–40°C to +85°C			300	µA
C_I	Control input capacitance	3.3	V_{IN} = Vcc or GND		25°C		3		pF
$C_{io(off)}$	A port: Switch input/output capacitance	3.3	V_I = 5.5V, 3.3V, 0V	V_{IN} = 0/Vcc s.t switch is off	25°C		15		pF
$C_{io(on)}$	A port: Switch input/output capacitance	3.3	V_I = 5.5V or 3.3V	V_{IN} = 0/Vcc s.t switch is on	25°C		10		pF
$C_{io(on)}$	A port: Switch input/output capacitance	3.3	V_I = 0V	V_{IN} = 0/Vcc s.t switch is on	25°C		22		pF
$C_{io(off)}$	B port: Switch input/output capacitance	3.3	V_I = 5.5V, 3.3V, 0V	V_{IN} = 0/Vcc s.t switch is off	25°C		5		pF
$C_{io(on)}$	B port: Switch input/output capacitance	3.3	V_I = 5.5V or 3.3V	V_{IN} = 0/Vcc s.t switch is on	25°C		4		pF
$C_{io(on)}$	B port: Switch input/output capacitance	3.3	V_I = 0V	V_{IN} = 0/Vcc s.t switch is on	25°C		22		pF
V_{ik}	Clamp voltage	3	I_I = -18mA		–40°C to +85°C			-1.2	V

5.6 Switching Characteristics 85C

over operating free-air temperature range (unless otherwise noted)

Parameter with Test conditions		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 1GΩ, C_L = 30pF, V_{load} = 0V. Calculated Tpd with switch resistance*CL	A or B	B or A	2.5 V ± 0.2 V			0.15	ns
t_{pd}	R_L = 1GΩ, C_L = 50pF, V_{load} = 0V. Calculated Tpd with switch resistance*CL	A or B	B or A	3.3 V ± 0.3 V			0.25	ns

over operating free-air temperature range (unless otherwise noted)

Parameter with Test conditions		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{en}	ZL: R_L = 250Ω, C_L = 30pF, V_{load} = VCC, ZH: RL = 500Ω, CL = 30pF, Vload = GND, 50ohm termination at input	OE	A or B	2.5 V ± 0.2 V	1		10.4	ns
t_{en}	ZL: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC} ZH: RL = 500Ω, CL = 50pF, Vload = GND, 50ohm termination at input	OE	A or B	3.3 V ± 0.3 V	1		8.3	ns
t_{dis}	LZ: R_L = 250Ω, C_L = 30pF, V_{load} = V_{CC}, V▲ = 0.15V; HZ: RL = 500Ω, CL = 30pF, Vload = GND, V▲ = 0.15V; 50ohm termination at input	OE	A or B	2.5 V ± 0.2 V	1		7.4	ns
t_{dis}	LZ: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, V▲ = 0.3V; HZ: RL = 500Ω, CL = 50pF, Vload = GND, V▲ = 0.3V; 50ohm termination at input	OE	A or B	3.3 V ± 0.3 V	1		8	ns
$t_{pd(s)}$	R_L = 500Ω, C_L = 30pF, V_{load} = 0V. Vinput = 3.6V domain. 50ohm termination at input	S	A	2.5 V ± 0.2 V			14.4	ns
$t_{pd(s)}$	R_L = 500Ω, C_L = 50pF, V_{load} = 0V. Vinput = 5.5V domain. 50ohm termination at input	S	A	3.3 V ± 0.3 V			11	ns
$t_{en(s)}$	ZL: R_L = 250Ω, C_L = 30pF, V_{load} = VCC, ZH: RL = 500Ω, CL = 30pF, Vload = GND; 50ohm termination at input	S	B	2.5 V ± 0.2 V	1		13.9	ns
$t_{en(s)}$	ZL: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC} ZH: RL = 500Ω, CL = 50pF, Vload = GND; 50ohm termination at input	S	B	3.3 V ± 0.3 V	1		10.6	ns
$t_{dis(s)}$	LZ: R_L = 250Ω, C_L = 30pF, V_{load} = V_{CC}, V▲ = 0.15V; HZ: RL = 500Ω, CL = 30pF, Vload = GND, V▲ = 0.15V; 50ohm termination at input	S	B	2.5 V ± 0.2 V	1		9.1	ns
$t_{dis(s)}$	LZ: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, V▲ = 0.3V; HZ: RL = 500Ω, CL = 50pF, Vload = GND, V▲ = 0.3V; 50ohm termination at input	S	B	3.3 V ± 0.3 V	1		8.5	ns

5.7 Typical Characteristics

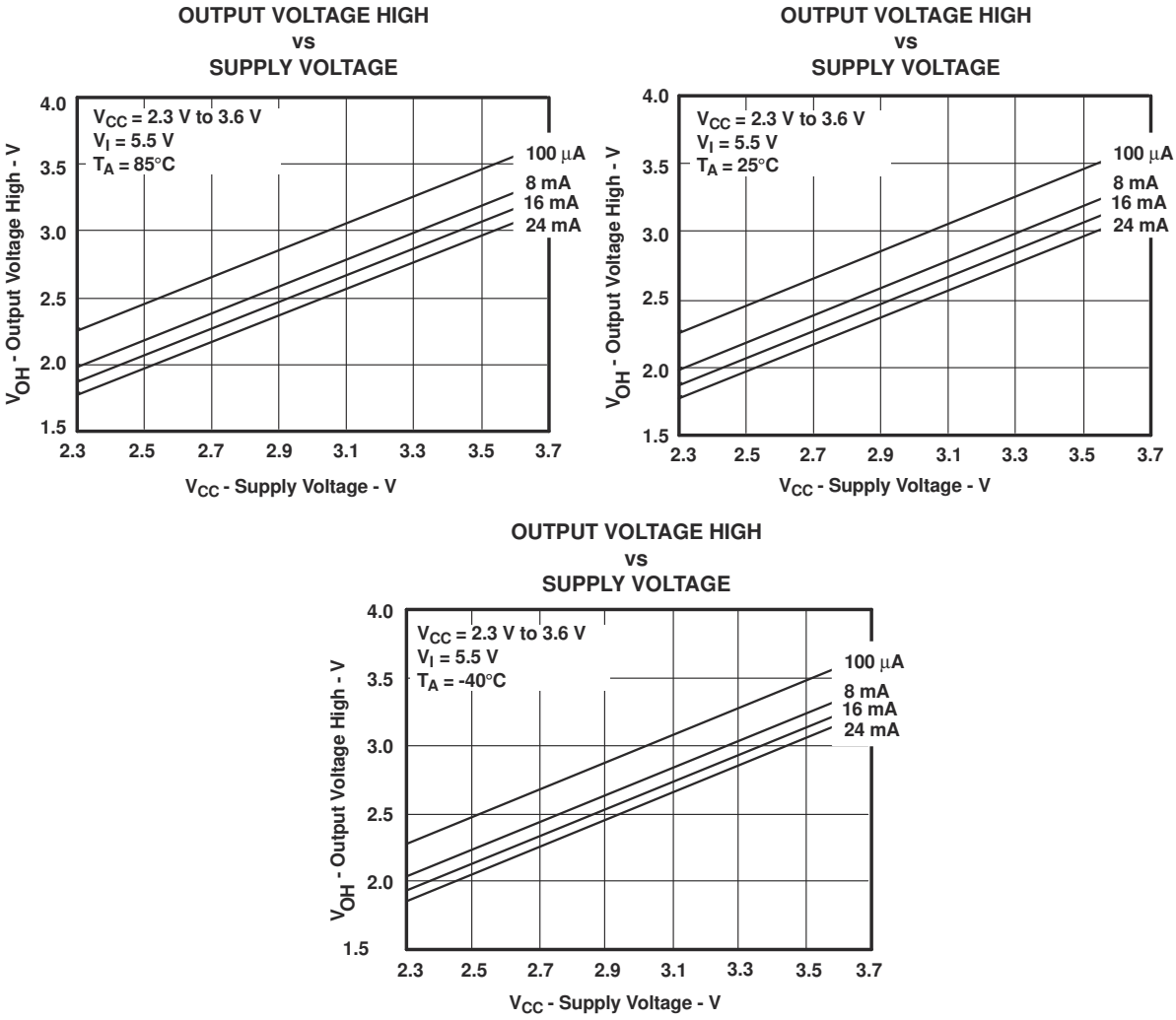
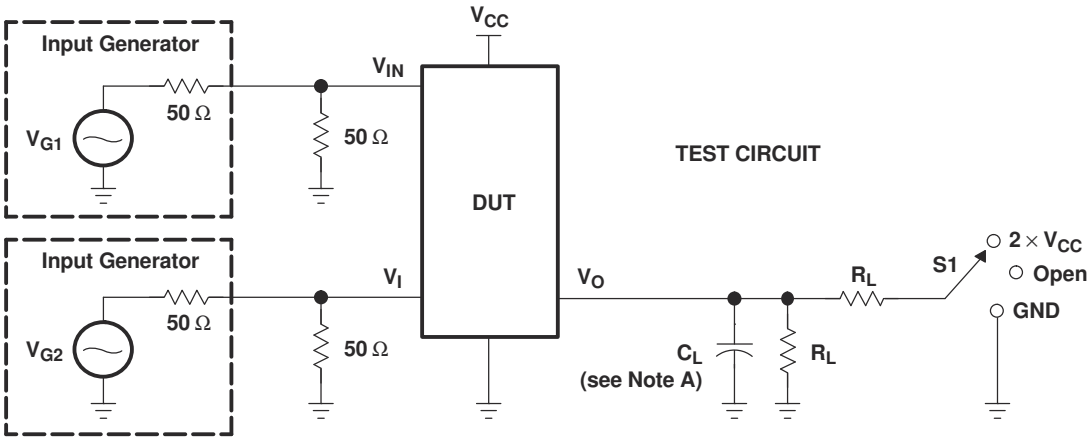
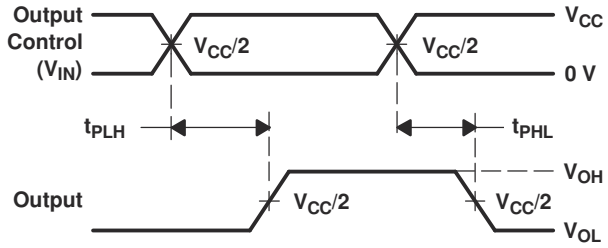


Figure 5-1. V_{OH} Values

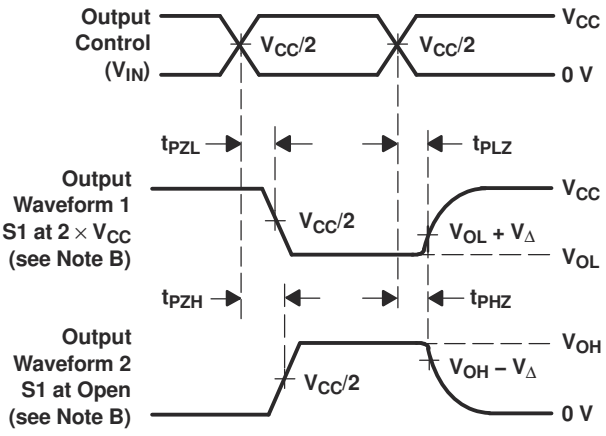
6 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	$2 \times V_{CC}$ $2 \times V_{CC}$	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74CB3T3253 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3253 supports systems using 5V TTL, 3.3V LVTTL, and 2.5V CMOS switching standards, as well as user-defined switching levels (see Typical DC Voltage-Translation Characteristics).

The SN74CB3T3253 is organized as two 1-of-4 multiplexer/demultiplexers with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature establishes that damaging current does not backflow through the device when the device is powered down. The device has isolation during power off.

To certify the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagrams

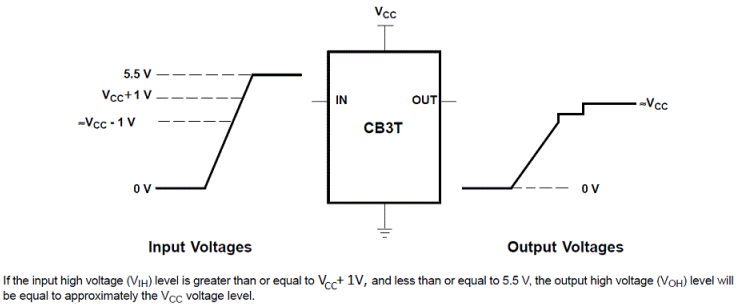


Figure 7-1. Typical DC Voltage-Translation Characteristics

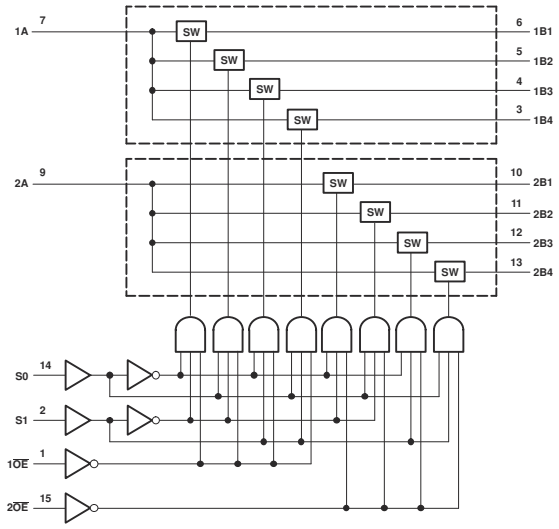
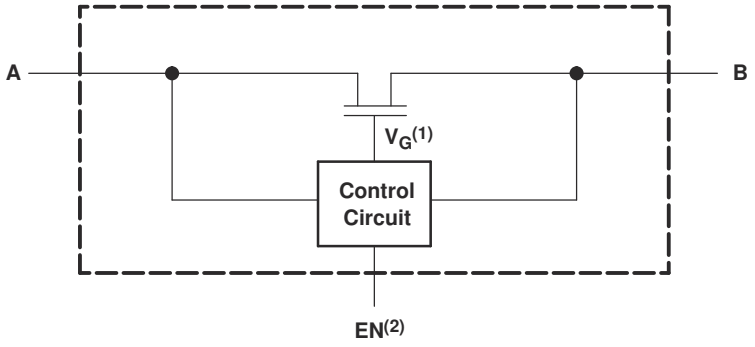


Figure 7-2. Logic Diagram (Positive Logic)



(1) Gate voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
(2) EN is the internal enable signal applied to the switch.

Figure 7-3. Simplified Schematic, Each FET Switch (SW)

7.3 Feature Description

The SN74CB3T3253 device is functionally equivalent to the QS3253 and has a 5Ω switch connection between two ports. The device also has rail-to-rail switching on data I/O ports as well as I_{off} supporting partial-power-down mode operation.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74CBTLV3253.

Table 7-1. Function Table (Each Multiplexer/Demultiplexer)

INPUTS			FUNCTION
$\overline{OE}$	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74CB3T3253 can be used to multiplex and demultiplex up to 2 channels simultaneously in a 4:1 configuration. The application shown here is a 2-bit bus multiplexed between two devices. The $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a generic example that is applicable in many situations.

8.2 Typical Application

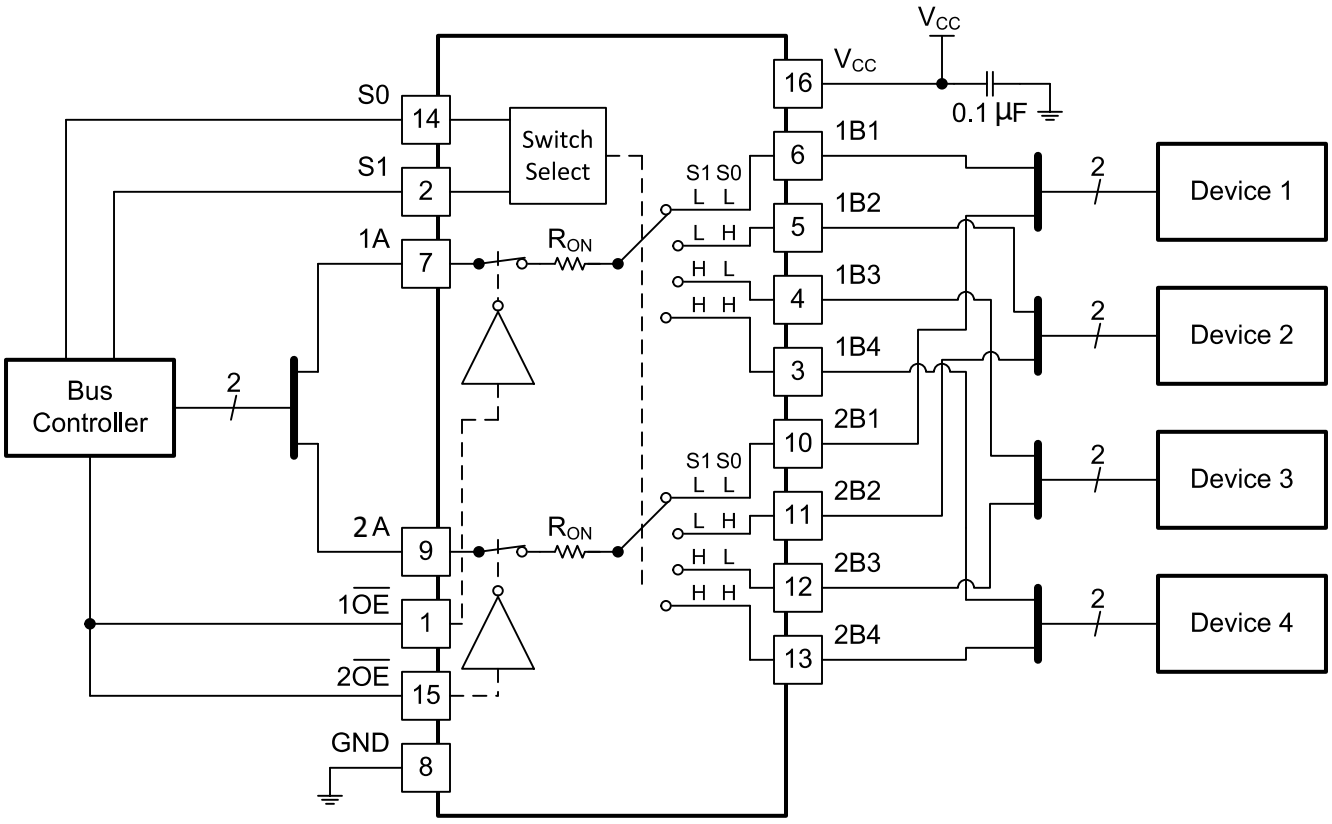


Figure 8-1. Typical Application of the SN74CB3T3253

8.2.1 Design Requirements

Place the 0.1µF capacitor as close as possible to the device.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in Section 5.3.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents must not exceed ±128mA per channel.
3. Frequency Selection Criterion:
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in Layout.

8.2.3 Application Curves

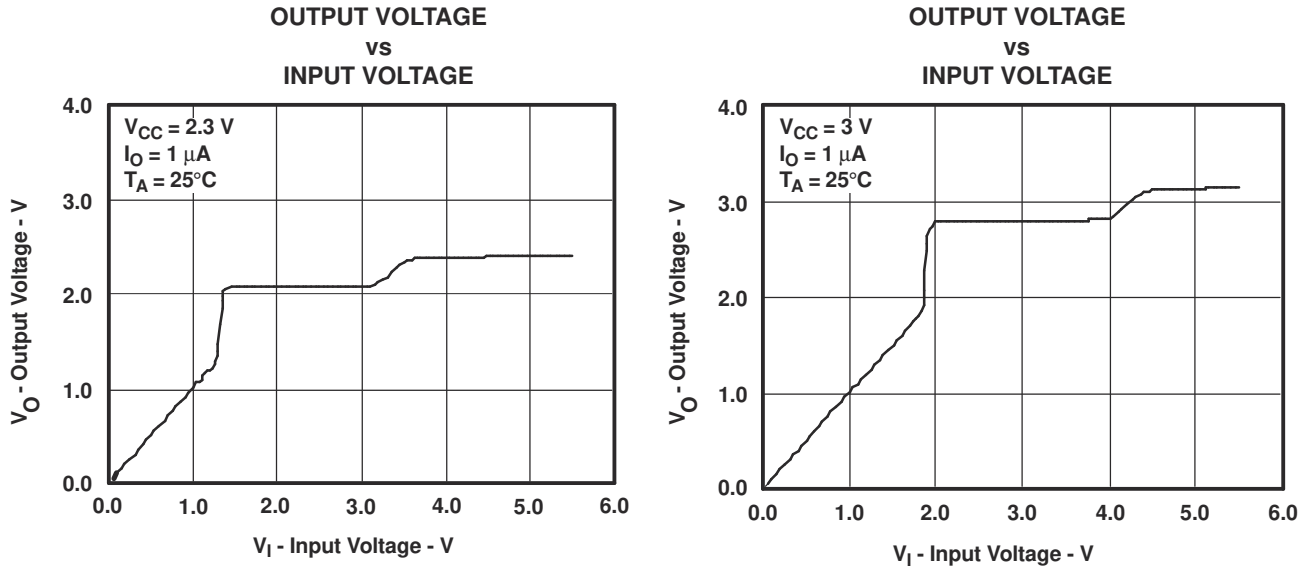


Figure 8-2. Data Output Voltage vs Data Input Voltage

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table.

To prevent power disturbance, confirm that Each V_{CC} terminal has a good bypass capacitor. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. For best results, install the bypass capacitor as close to the power terminal as possible.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Trace Example shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

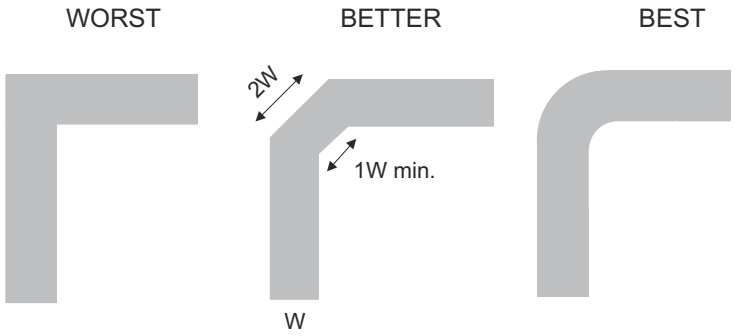


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2003) to Revision A (May 2025)	Page
• Added the *Applications*, *Package Information table*, *Pin Configuration and Functions*, *Specifications*, *ESD Ratings*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Application Information*, *Typical Application*, *Power Supply Recommendations*, *Layout*, and *Device and Documentation Support* sections	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated graphic and note in Typical DC Voltage-Translation Characteristics	1
• Updated specs in the *Electrical Characteristics* table	4
• Updated specs in the *Switching Characteristics* table	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3T3253D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3253
SN74CB3T3253D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3253
SN74CB3T3253DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	KS253
SN74CB3T3253DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	KS253
SN74CB3T3253DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3253
SN74CB3T3253DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3253
SN74CB3T3253PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	KS253
SN74CB3T3253PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253
SN74CB3T3253PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

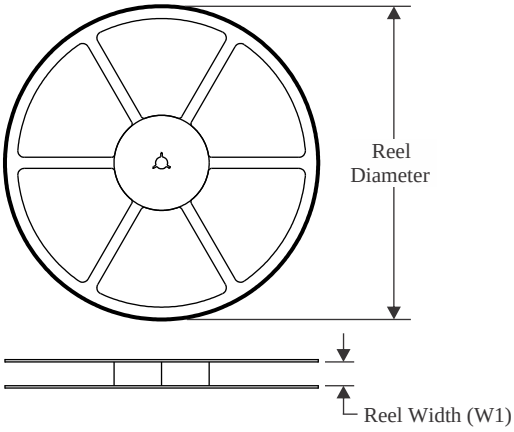
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

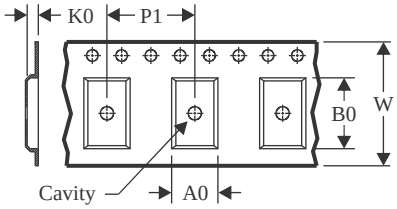
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

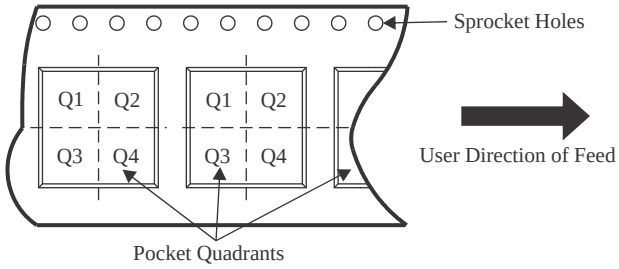


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

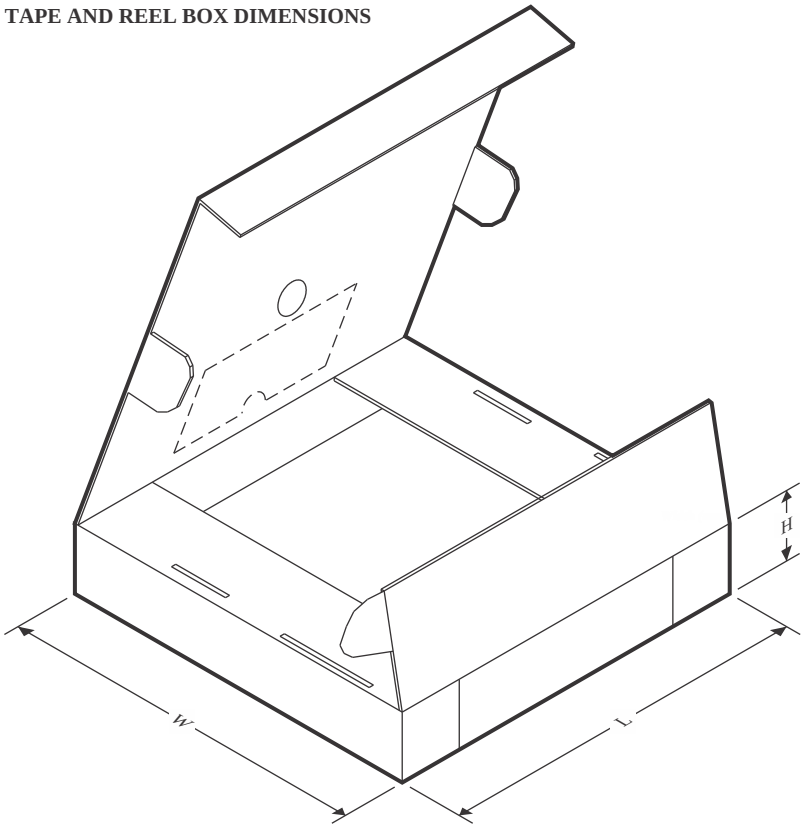
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3T3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3T3253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

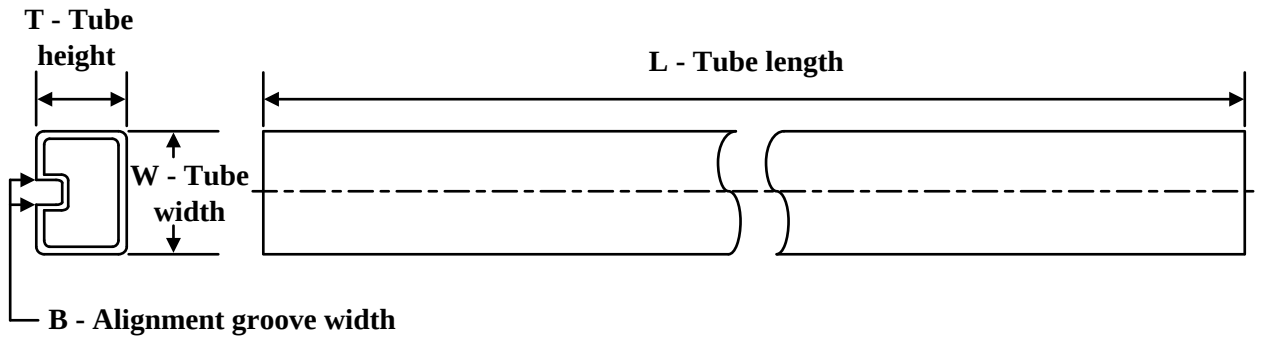
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3253DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CB3T3253DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CB3T3253DR	SOIC	D	16	2500	340.5	336.1	32.0

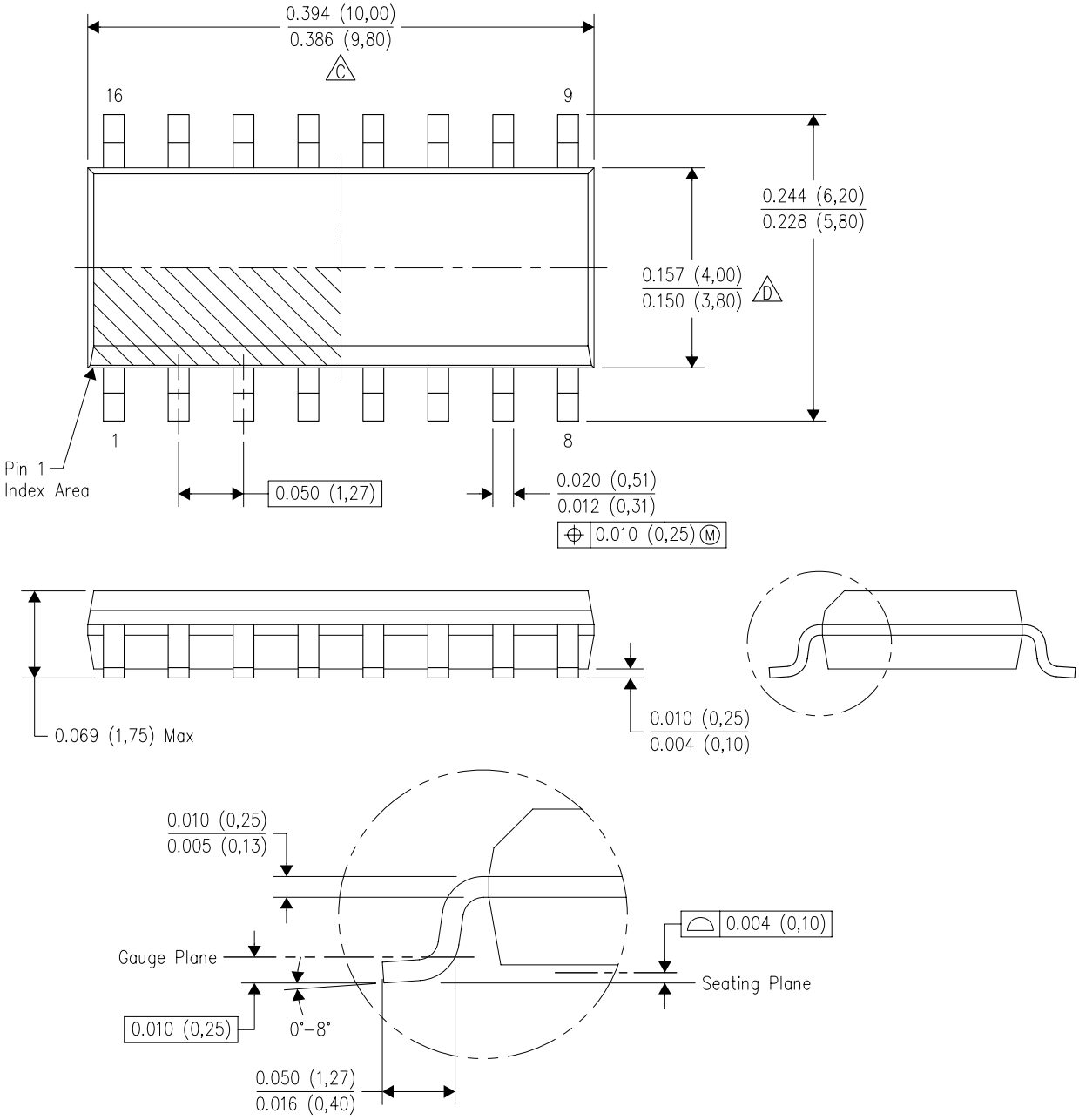
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3T3253D	D	SOIC	16	40	507	8	3940	4.32
SN74CB3T3253D.B	D	SOIC	16	40	507	8	3940	4.32

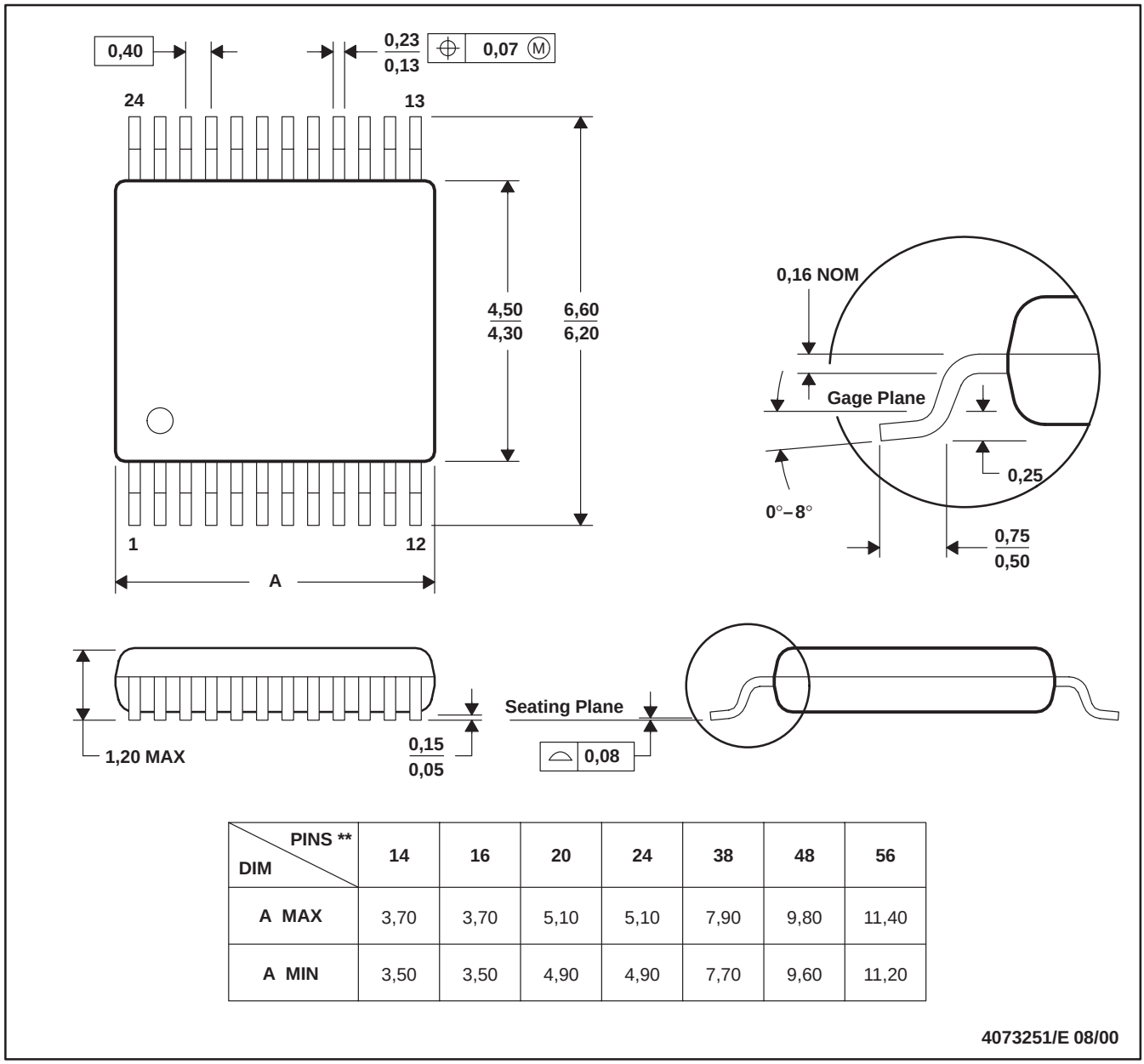
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

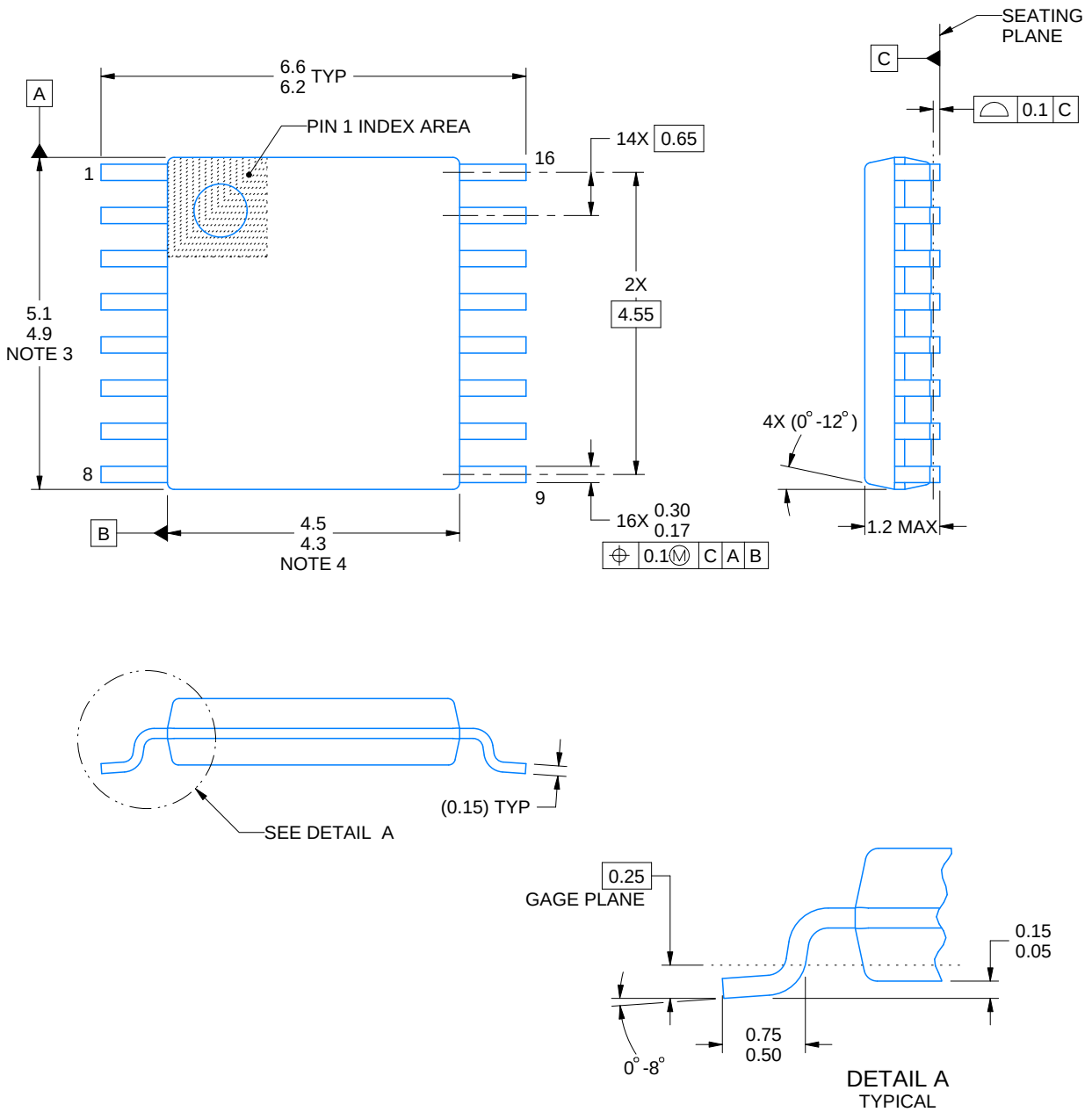
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

PW0016A

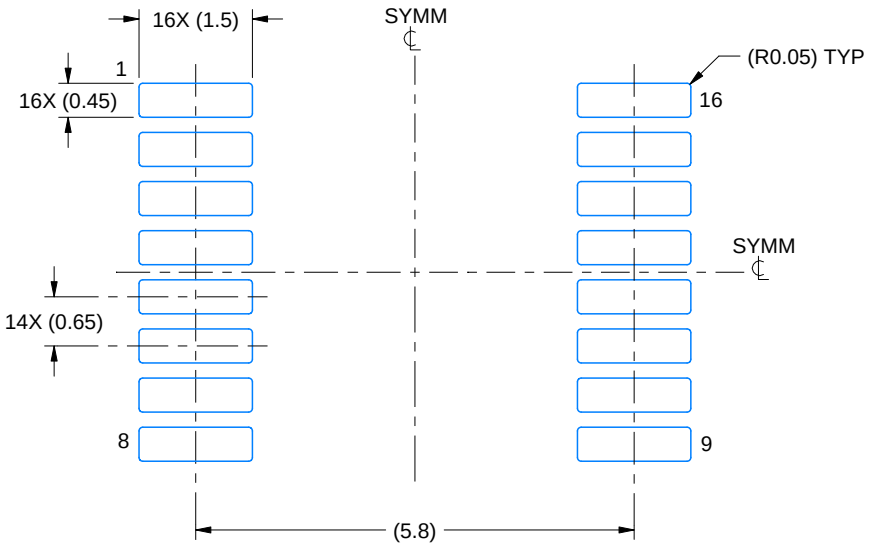
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



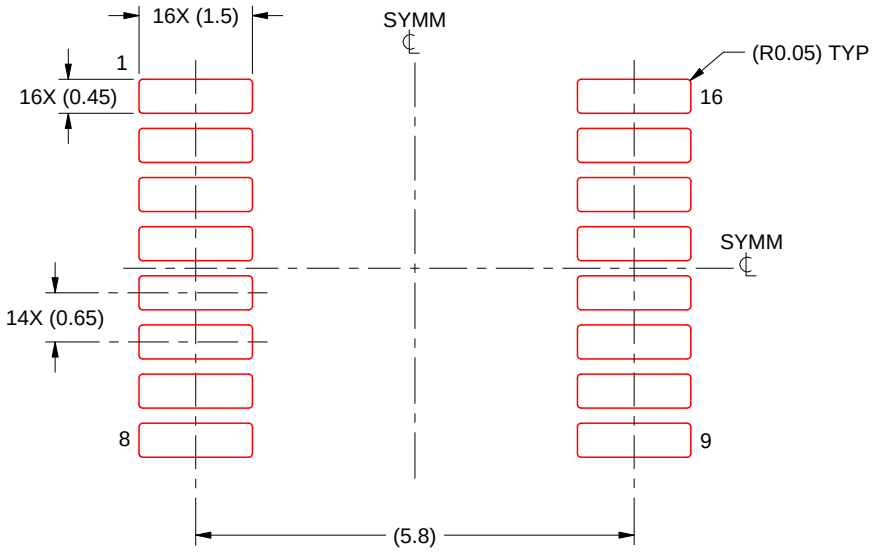
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

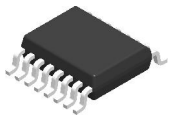


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

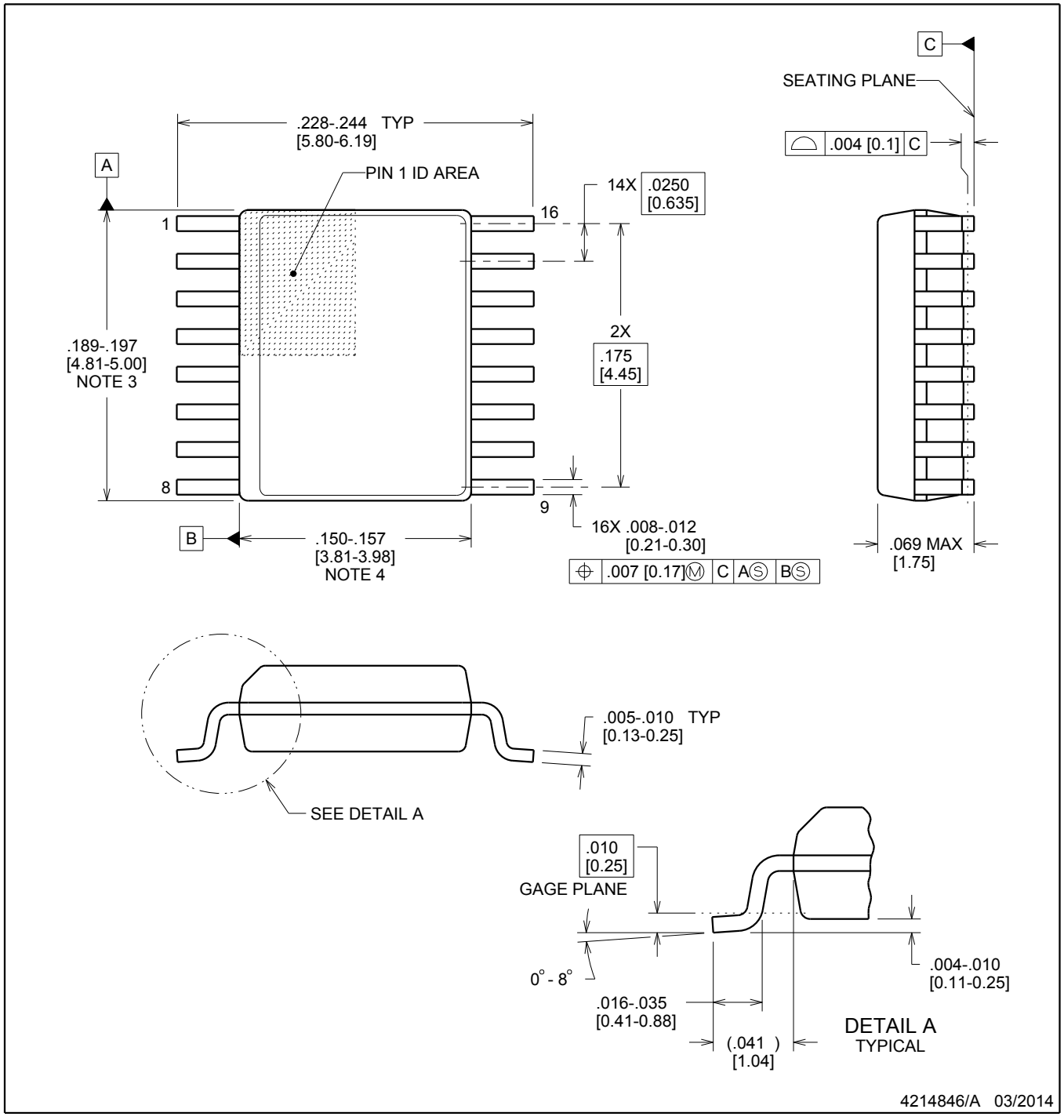


PACKAGE OUTLINE

DBQ0016A

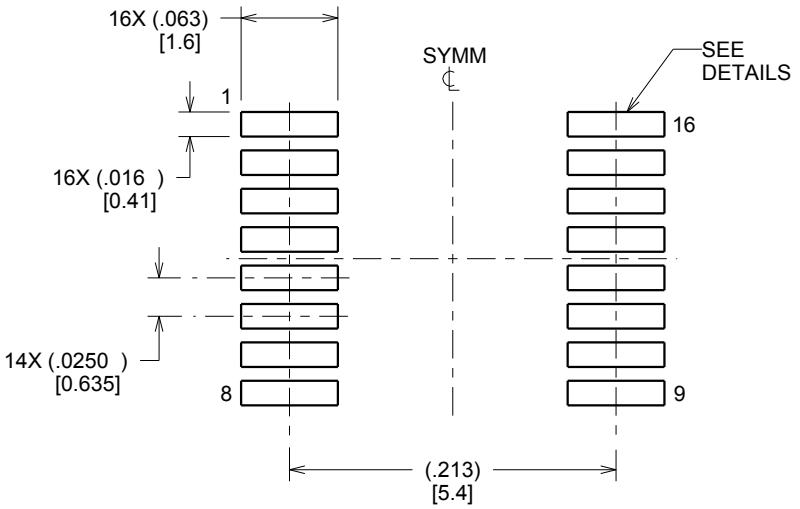
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

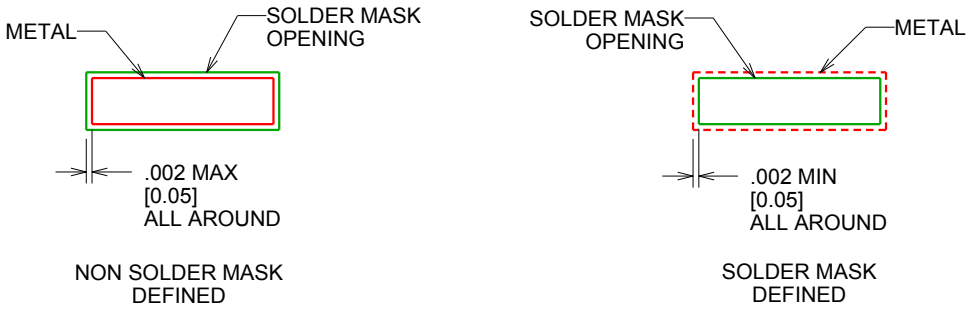


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

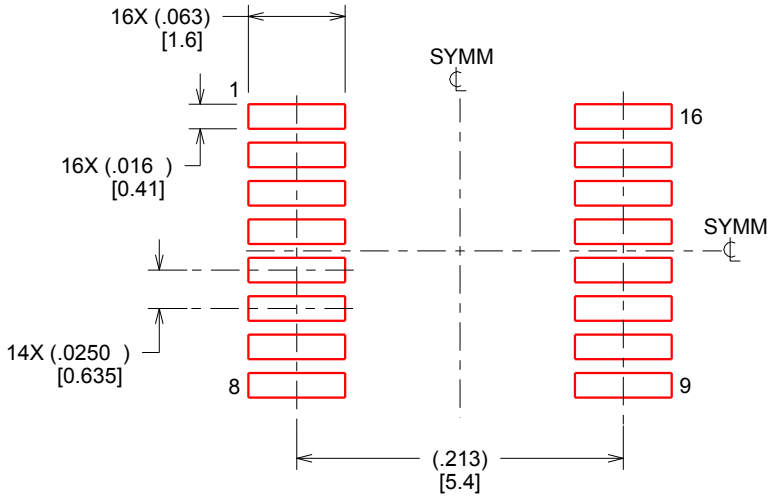
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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