- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (JT, NT)**

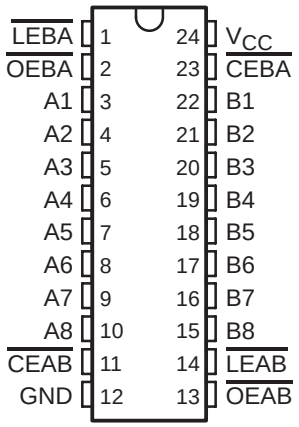
description

The ′BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

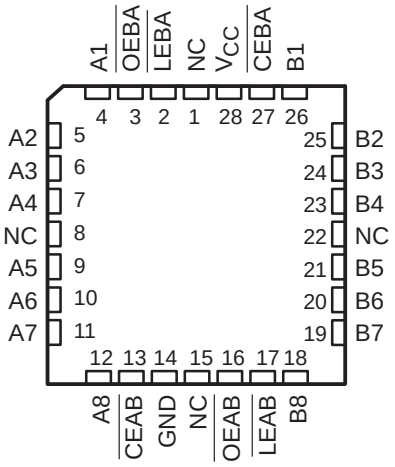
The A-to-B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT543 is characterized for operation from 0°C to 70°C.

SN54BCT543 . . . JT OR W PACKAGE
SN74BCT543 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT543 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.
‡ Output level before the indicated steady-state input conditions were established.

TEXAS INSTRUMENTS
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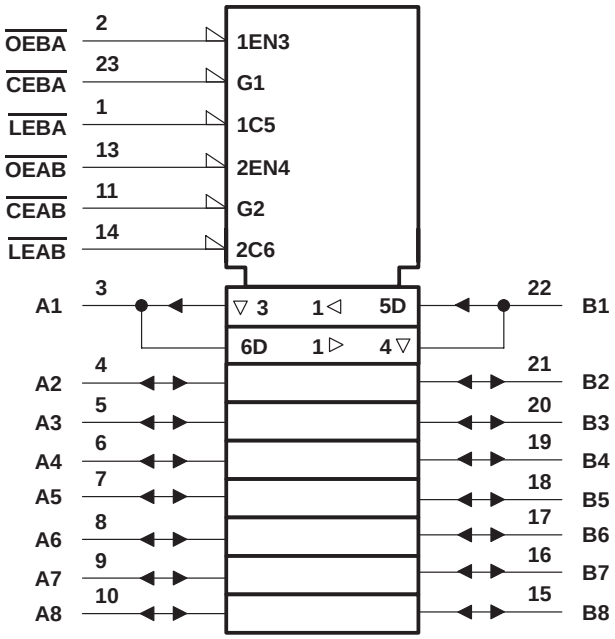
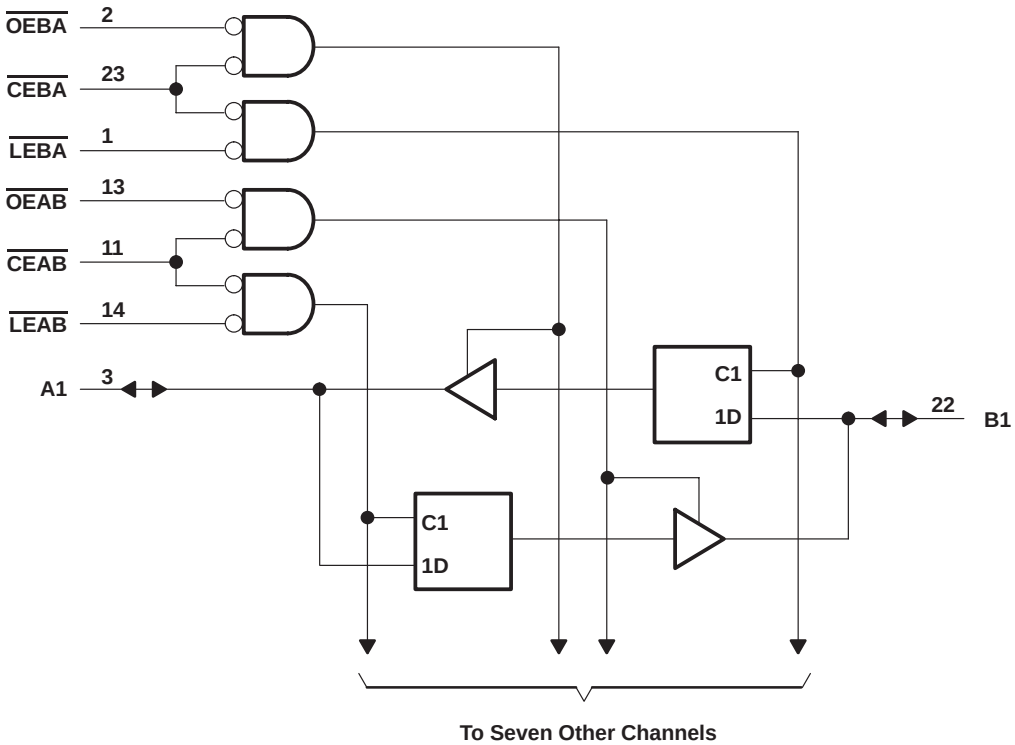
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . − 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1) . . . . . − 0.5 V to 7 V
I/O ports (see Note 1) . . . . . − 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . − 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . − 0.5 V to V_{CC}
Input clamp current, I_{IK} . . . . . −30 mA
Current into any output in the low state: SN54BCT543 . . . . . 96 mA
SN74BCT543 . . . . . 128 mA
Operating free-air temperature range: SN54BCT543 . . . . . − 55°C to 125°C
SN74BCT543 . . . . . 0°C to 70°C
Storage temperature range . . . . . − 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT543			SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT543			SN74BCT543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.4			0.4	mA
I_{IH}‡	A or B port	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	Control input					20			20	
I_{IL}‡	A or B port	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	Control input					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCL}	A or B port	V_{CC} = 5.5 V			45	71		45	71	mA
I_{CCH}	A or B port	V_{CC} = 5.5 V			5	8		5	8	mA
I_{CCZ}	A or B port	V_{CC} = 5.5 V			9	15		9	15	mA
C_i	Control input	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_{io}	A or B port	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		16			16		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54BCT543		SN74BCT543		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		7		8		7		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$↑	High or low	4.5		5.5		4.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$↑	High or low	1.5		1.5		1.5		ns

TEXAS INSTRUMENTS
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switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			′BCT543			SN54BCT543		SN74BCT543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	5.7	7.5	2	9.9	2	8.8	ns
t_{PHL}			2	6.3	8.2	2	9.7	2	9.6	
t_{PLH}	$\overline{LE}$	A or B	2	8.2	10.3	2	13.9	2	12.9	ns
t_{PHL}			2	8.5	10.6	2	13.2	2	12.7	
t_{PZH}	$\overline{OE}$	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
t_{PZL}			1	8.7	10.8	1	12.8	1	12.3	
t_{PHZ}	$\overline{OE}$	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
t_{PLZ}			1	4.7	6.4	1	8.1	1	7.2	
t_{PZH}	$\overline{CE}$	A or B	1	7.6	9.8	1	12.8	1	12	ns
t_{PZL}			1	9.5	11.6	1	13.8	1	13.5	
t_{PHZ}	$\overline{CE}$	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
t_{PLZ}			1	4.8	6.7	1	8.4	1	7.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9087001M3A	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9087001M3A SNJ54BCT 543FK
SN74BCT543DW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT543
SN74BCT543DW.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT543
SNJ54BCT543FK	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9087001M3A SNJ54BCT 543FK
SNJ54BCT543FK.A	Active	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9087001M3A SNJ54BCT 543FK
SNJ54BCT543JT	Active	Production	CDIP (JT) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9087001MLA SNJ54BCT543JT
SNJ54BCT543JT.A	Active	Production	CDIP (JT) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9087001MLA SNJ54BCT543JT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

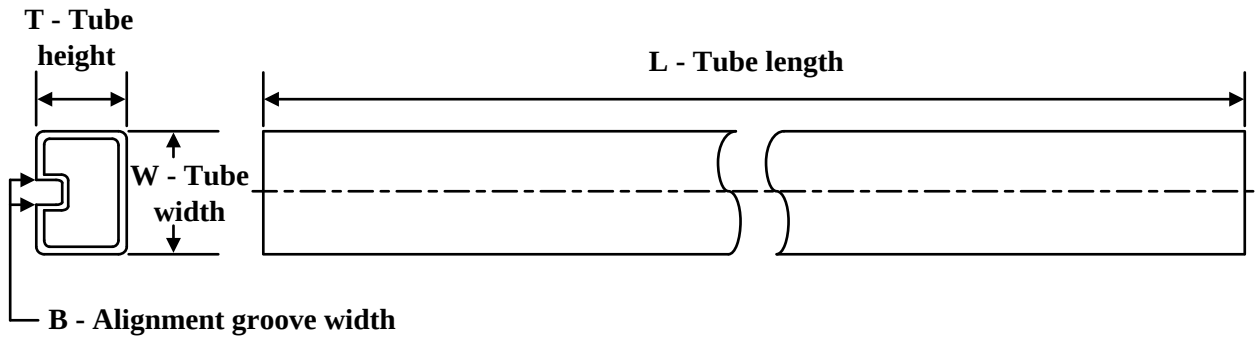
OTHER QUALIFIED VERSIONS OF SN54BCT543, SN74BCT543 :

- Catalog : SN74BCT543
- Military : SN54BCT543

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



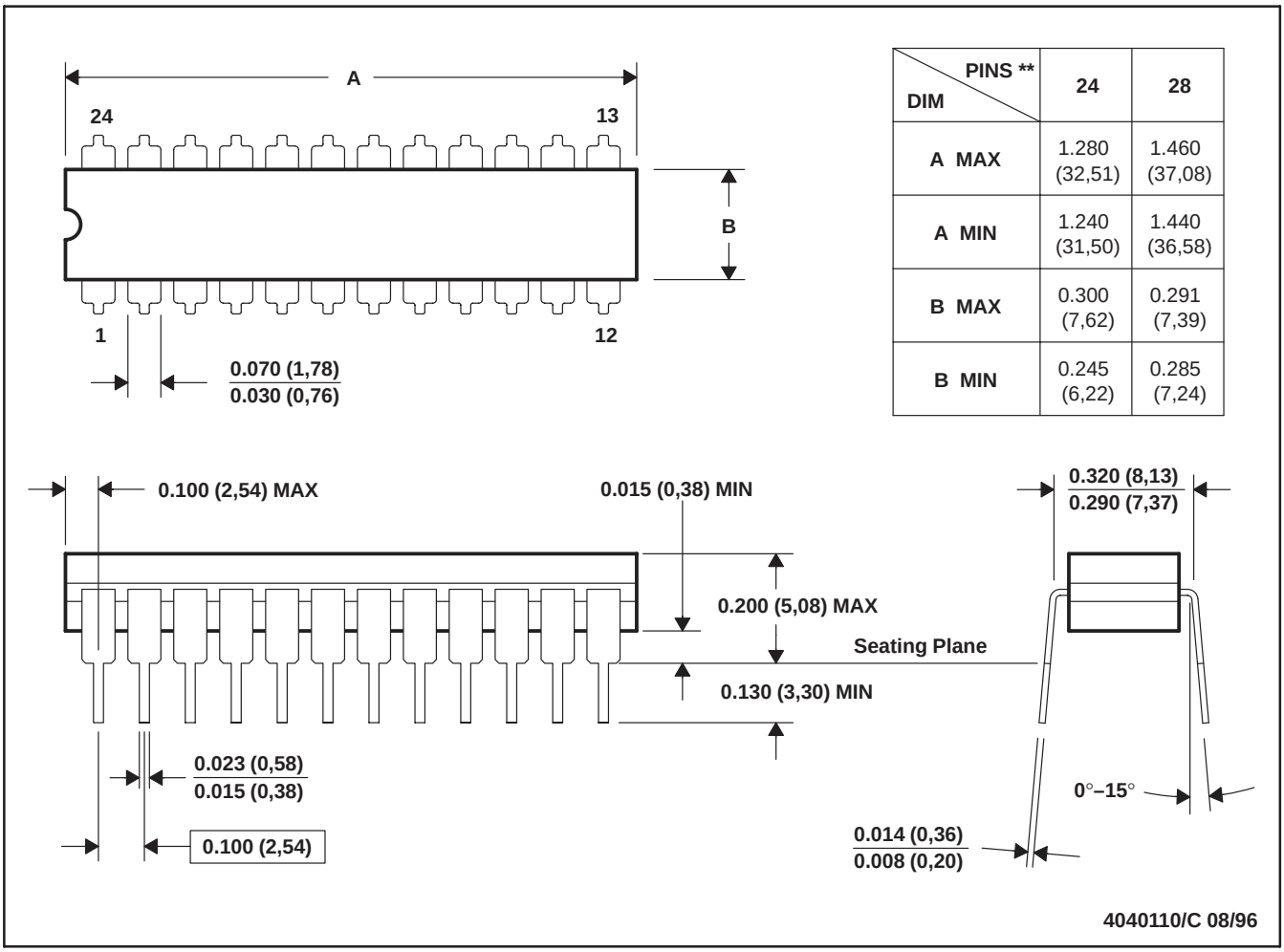
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74BCT543DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74BCT543DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN

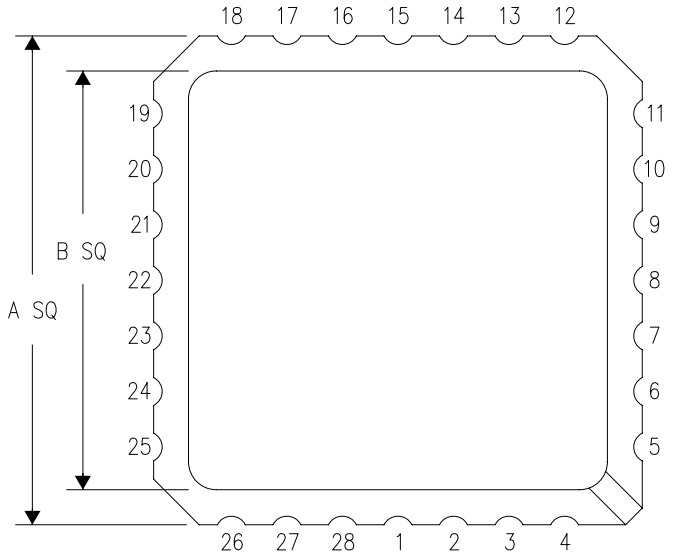


DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

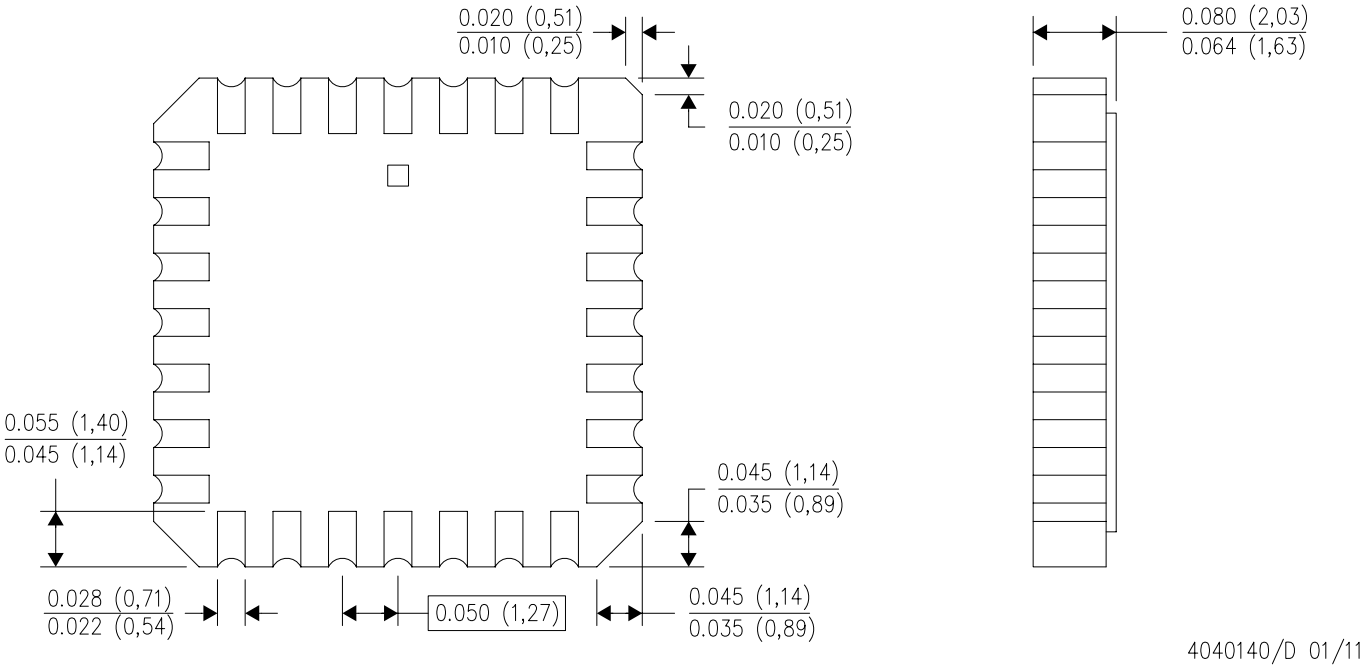
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



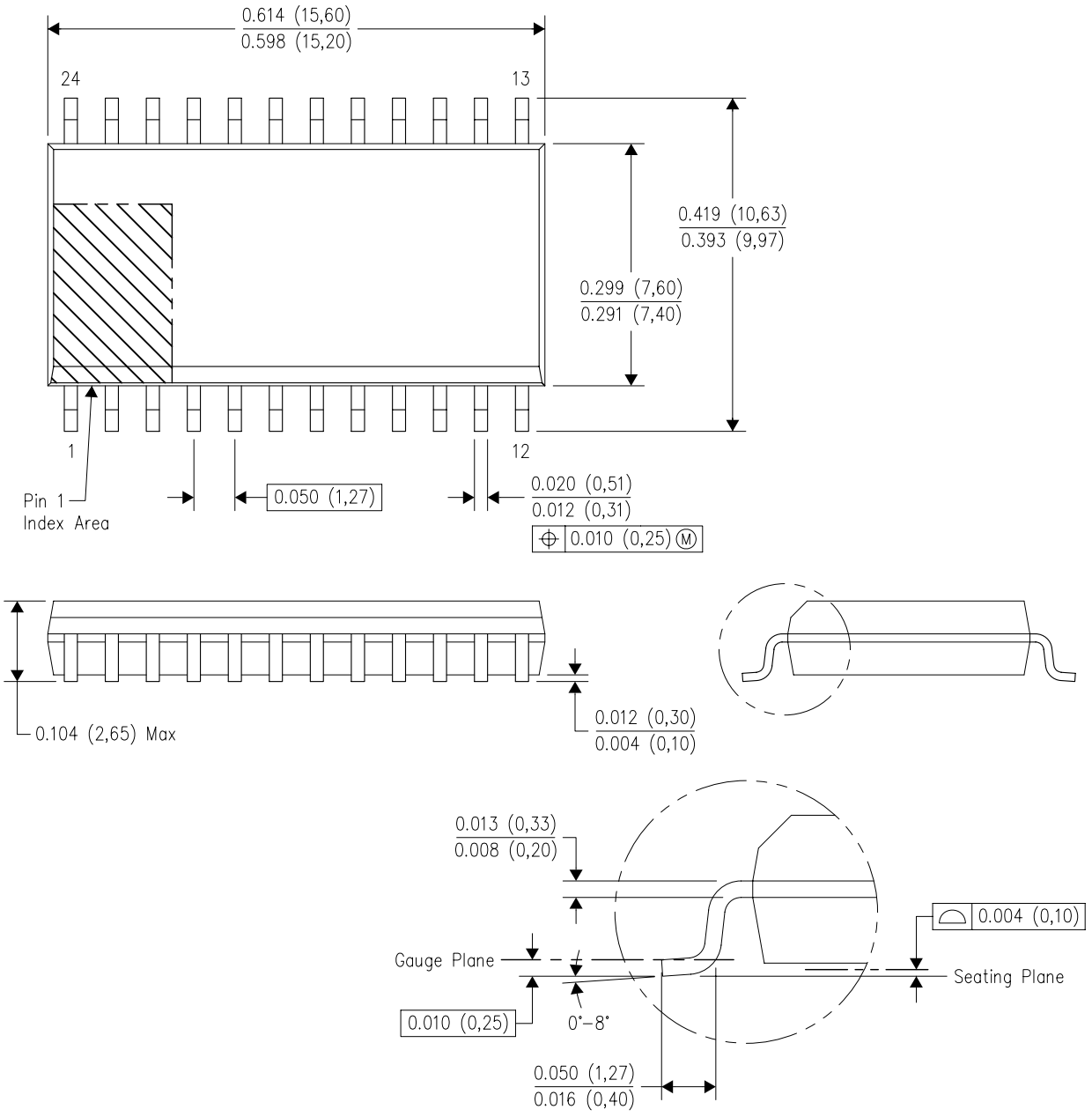
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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