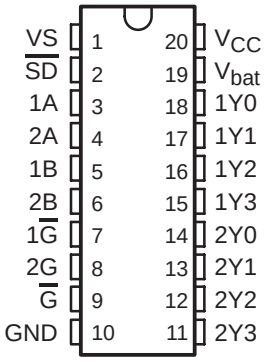
- **BiCMOS Design Substantially Reduces Standby Current**
- **Two Independent 2-Line to 4-Line Decoders or One 3-Line to 8-Line Decoder**
- **Separate Enable Inputs for Easy Cascading**
- **Two Supply Voltage Terminals (V_{CC} and V_{bat})**
- **Built-In Supply-Voltage Monitor for V_{CC}**
- **Automatic Cut Off of Outputs During V_{CC} Fail**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



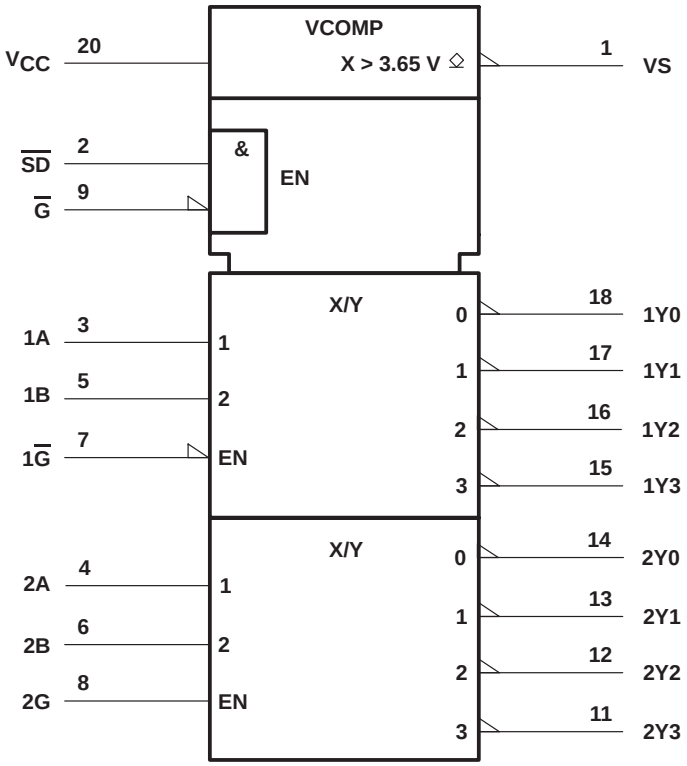
description

The SN74BCT2414 is a decoder specially designed to be used in memory systems with battery backup during power failure. The two independent 2-line to 4-line decoders with separate and common control inputs may be externally cascaded to implement a 3-line to 8-line decoder.

The circuit has two supply voltage inputs: the voltage monitor (bandgap) is powered via the V_{CC} terminal; the internal logic of the circuit is powered via the V_{bat} terminal. In case V_{CC} drops below 3.65 V (nominal), the voltage monitor forces the voltage-control (VS) and decoder outputs (Y) to the high level. VS may be used to disconnect the supply voltage of the memories (V_{bat}) from the system supply. This output is switched off when the on-chip supply voltage monitor detects a power failure.

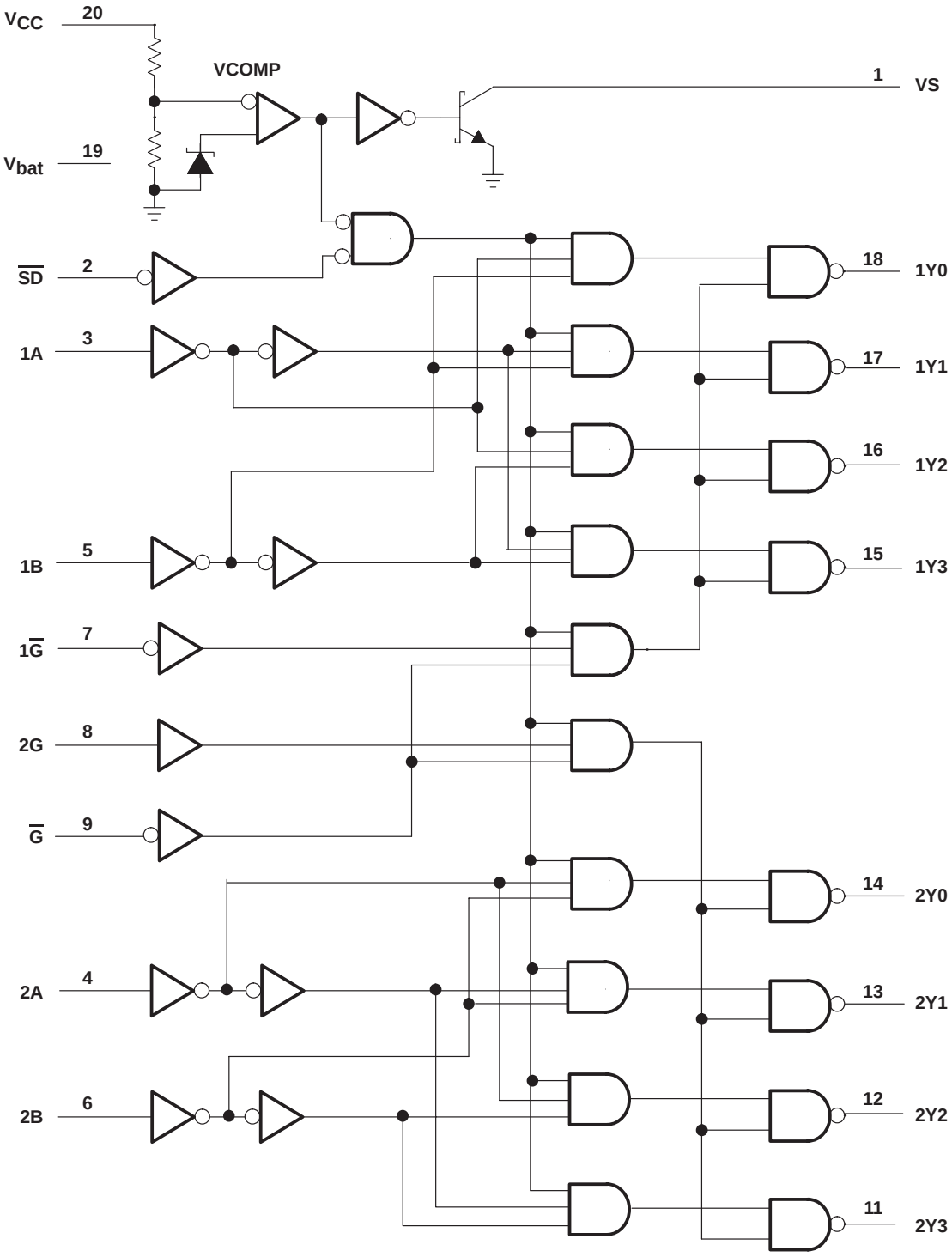
The SN74BCT2414 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLES

INPUTS					OUTPUTS			
CONTROL			SELECT					
$\overline{G}$	$1\overline{G}$	$\overline{SD}$	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	L	H	L	L	L	H	H	H
L	L	H	L	H	H	L	H	H
L	L	H	H	L	H	H	L	H
L	L	H	H	H	H	H	H	L

INPUTS					OUTPUTS			
CONTROL			SELECT					
$\overline{G}$	2G	$\overline{SD}$	2B	2A	2Y0	2Y1	2Y2	2Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	H	H	L	L	L	H	H	H
L	H	H	L	H	H	L	H	H
L	H	H	H	L	H	H	L	H
L	H	H	H	H	H	H	H	L

NOTE: For a 3-line to 8-line decoder, the following pins must be shorted: $1\overline{G}$ to 2G, 1A to 2A and 1B to 2B.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{bat} . . . . . −0.5 V to 7 V
Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage V_{CC} with respect to V_{bat} . . . . . −1.5 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC} + 0.5 V
Off-state output voltage range at VS . . . . . −0.5 V to 7 V
Voltage range applied to any Y output in the power-off state . . . . . −0.5 V to 7 V
Voltage applied to any Y output in the power-off state with respect to V_{bat} . . . . . 0.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{bat}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−400	µA
I_{OL}	Low-level output current	Y outputs			8	mA
		VS outputs			20	
t_t	Input transition time		0		10	ns/V
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{bat} = V_{CC} = 4.5 V	I_{OH} = − 20 µA	4.4			V
			I_{OH} = − 400 µA	3.5			
		V_{bat} = 2 V, V_{CC} = 0,	I_{OH} = − 50 µA	1.8			
V_{OL}	All except VS	V_{bat} = V_{CC} = 4.5 V	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.5	
	VS	V_{bat} = V_{CC} = 4.5 V,	I_{OL} = 20 mA			1	
V_T‡					3.65		V
I_I		V_{bat} = V_{CC} = 5.5 V,	V_I = 5.5 V			100	µA
I_{IH}		V_{bat} = V_{CC} = 5.5 V,	V_I = 2.7 V			±20	µA
I_{IL}		V_{bat} = V_{CC} = 5.5 V,	V_I = 0.5 V			±20	µA
I_{OH}	VS	V_{bat} = 4.5 V,	V_{CC} = 0			1	µA
I_O§		V_{bat} = V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−200	mA
I_{CC}		V_{bat} = V_{CC} = 5.5 V	Outputs high			3	mA
			Outputs low			3	
I_{bat}		V_{bat} = 2.5 V,	V_{CC} = 0		1	10	µA
		V_{bat} = V_{CC} = 5.5 V	Outputs high			20	
			Outputs low			3	mA
C_i		V_{bat} = V_{CC} = 5 V,	V_I = 0 or 3 V		4		pF
C_o	Any Y	V_{bat} = V_{CC} = 0			6.5		pF
	VS				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This value represents the V_{CC} monitor threshold voltage. Typical range is from 3.5 V to 3.8 V.
§ This output condition has been chosen to produce a current that closely approximates one half of the short-circuit output current, I_{OS}. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	5	10	1	12	ns
t_{PHL}			2	5.8	10	2	12	
t_{PLH}	Any $\overline{G}$	Any Y	1	4.5	9	1	10	ns
t_{PHL}			2	5.5	9	2	11	
t_{PLH}	$\overline{SD}$	Any Y	2	6.5	11	2	12	ns
t_{PHL}			2	6.5	11	2	12	

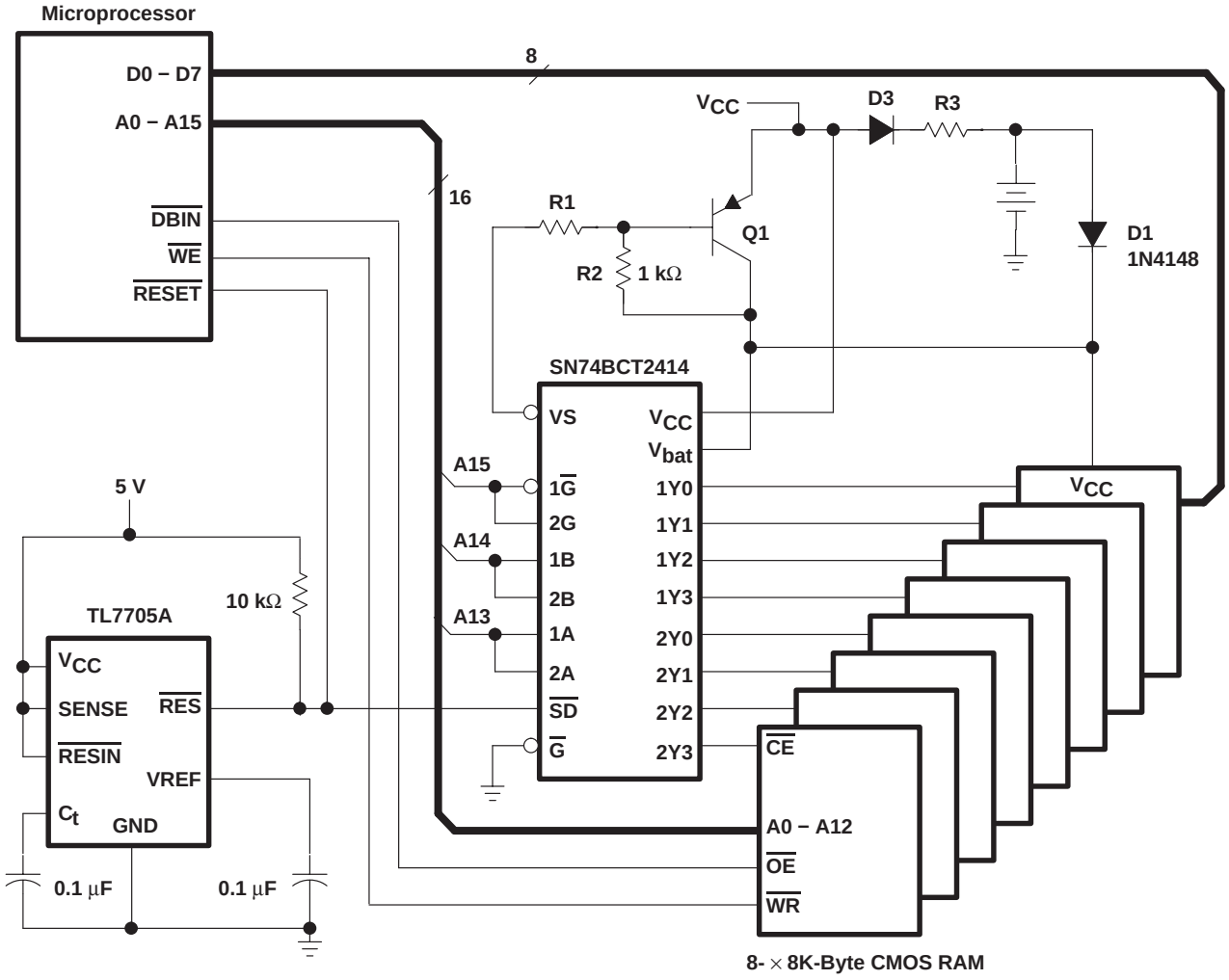
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	V_{CC}	Any Y	10	25	50	10	250	ns
t_{PHL}			15	45	100	15	250	
t_{PLH}	V_{CC}	VS	10	28	50	10	250	ns
t_{PHL}			20	50	100	20	250	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

A typical application circuit for a battery-buffered memory in a microcomputer system is shown in Figure 1 which uses the SN74BCT2414. When power fails, the supply-voltage supervisor (TL7705) resets the microcomputer and disables the memory by switching the shutdown input $\overline{SD}$ of the memory decoder to a logic zero. All memory decoder outputs are forced to a logic one. Abnormal write commands from the microprocessor, which may be issued during further voltage breakdown, no longer affect the contents of the memory. When the system supply voltage becomes lower than approximately 3.65 V, the voltage monitor inside the SN74BCT2414 memory decoder disconnects the input buffers of this circuit from the decoding logic internally and keeps all outputs at a logic one. The VS output is also switched off, disconnecting the system supply voltage from the memory circuits. During this low-voltage condition, the memory decoder and the memory circuits are supplied by the battery.



For further information on this device, please contact factory.

Figure 1. Memory System With Battery Backup

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74BCT2414DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2414
SN74BCT2414DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2414
SN74BCT2414N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT2414N
SN74BCT2414N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT2414N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

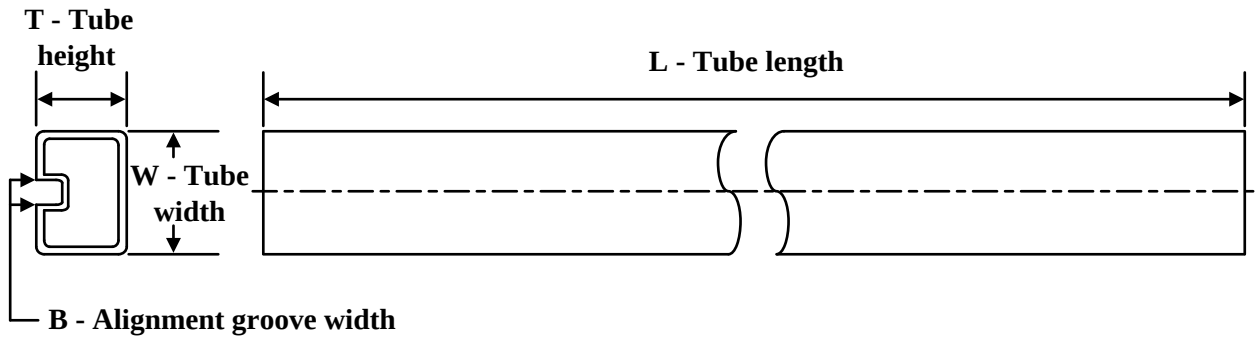
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



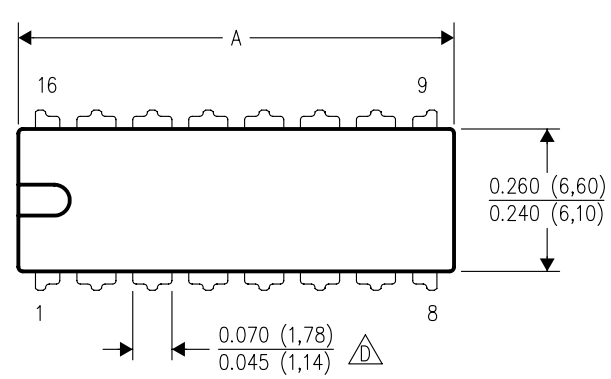
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74BCT2414DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT2414DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT2414N	N	PDIP	20	20	506	13.97	11230	4.32
SN74BCT2414N.A	N	PDIP	20	20	506	13.97	11230	4.32

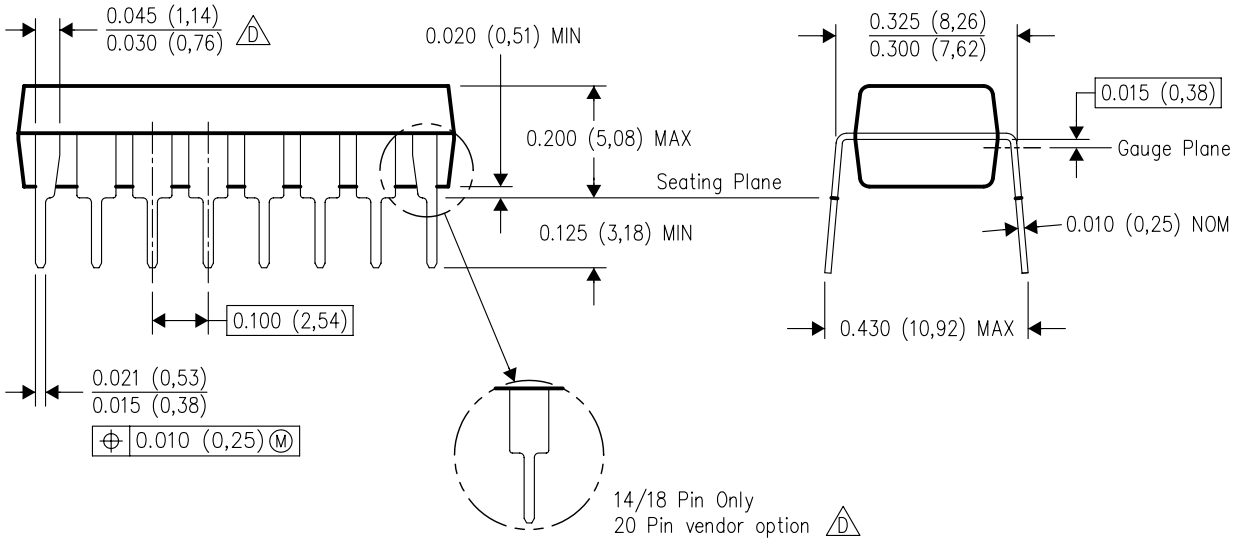
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

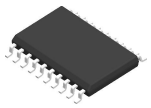


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

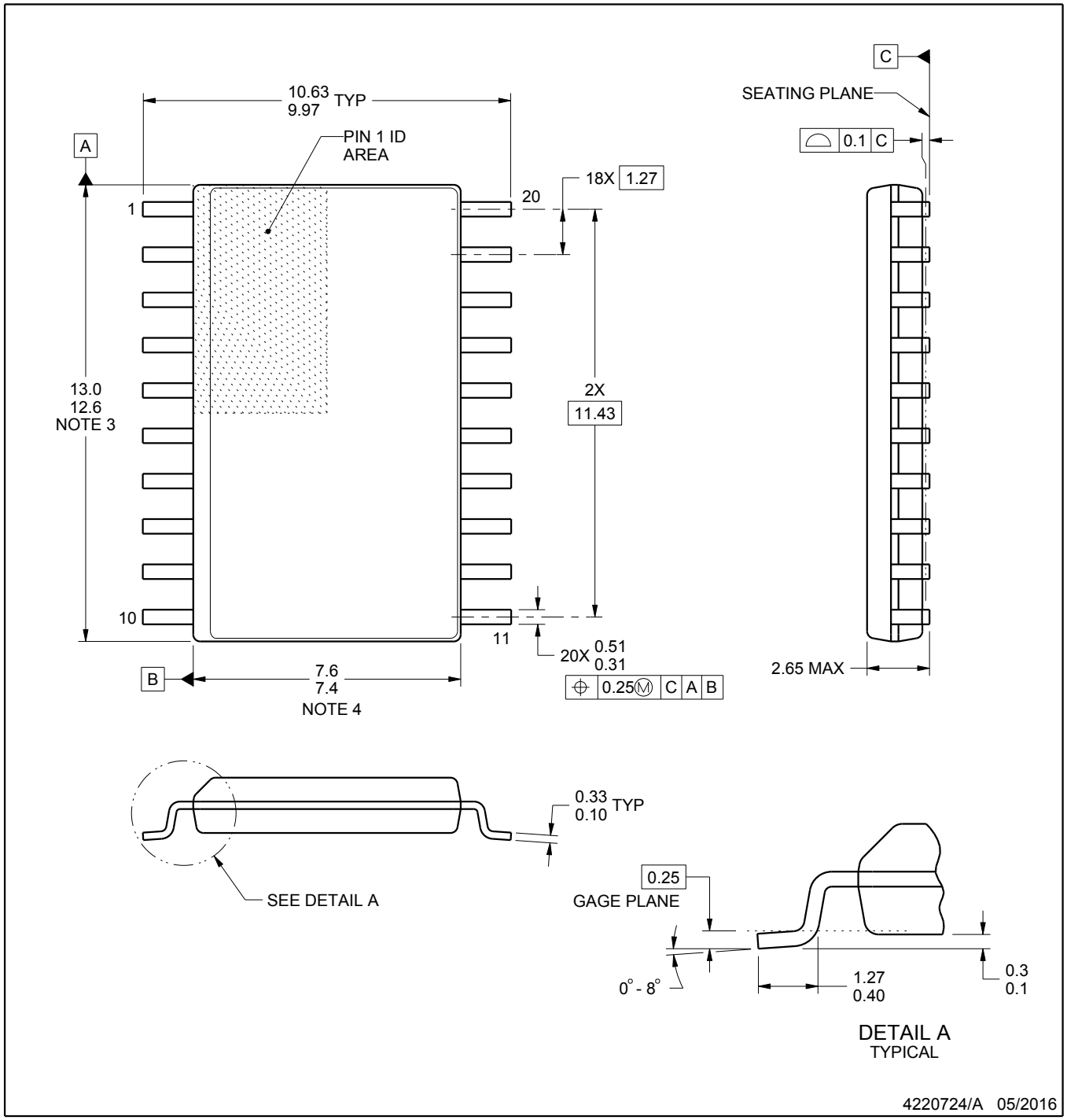


PACKAGE OUTLINE

DW0020A

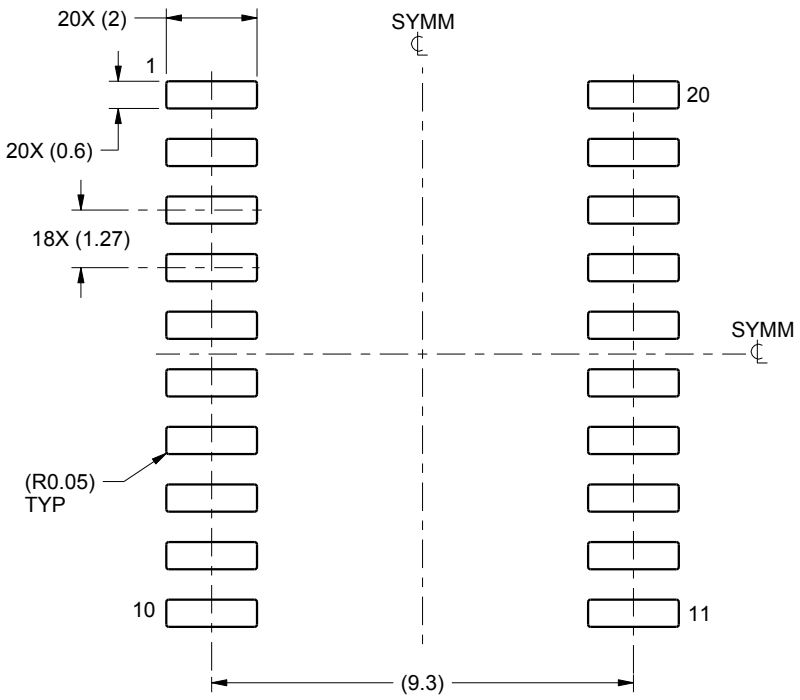
SOIC - 2.65 mm max height

SOIC

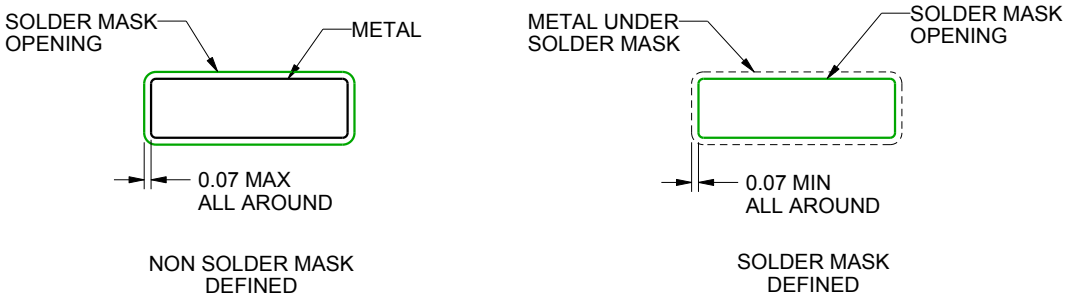


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

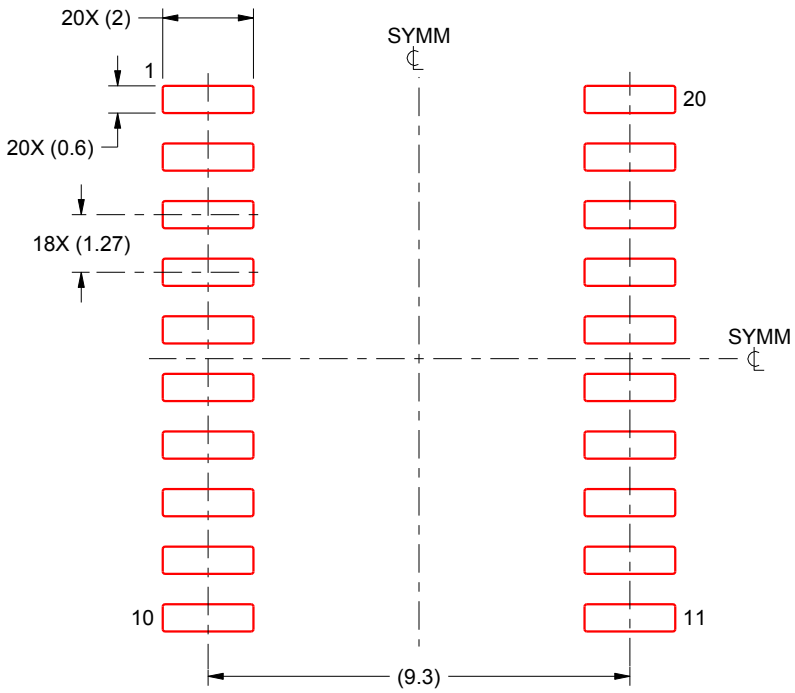


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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