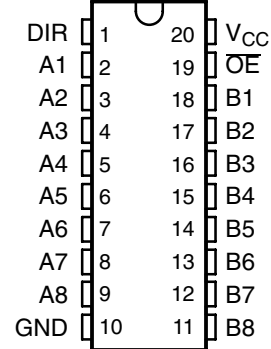


# SN74BCT2245 OCTAL TRANSCEIVER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

SCBS102C – FEBRUARY 1992 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- B Port Has Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DW, N, OR NS PACKAGE  
(TOP VIEW)



## description/ordering information

The SN74BCT2245 octal transceiver and line/MOS driver is designed for asynchronous communication between data buses.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can disable the devices so that both buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The B-port outputs, which are designed to source or sink up to 12 mA, include 33- $\Omega$  series resistors to reduce overshoot and undershoot.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT2245N	SN74BCT2245N
	SOIC – DW	Tube	SN74BCT2245DW	BCT2245
		Tape and reel	SN74BCT2245DWR	
	SOP – NS	Tape and reel	SN74BCT2245NSR	BCT2245
	SSOP – DB	Tape and reel	SN74BCT2245DBR	BA245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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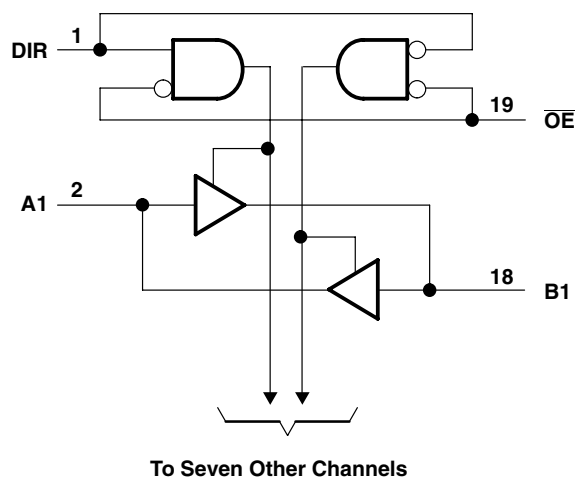
# SN74BCT2245

## OCTAL TRANSCEIVER AND LINE/MOS DRIVER

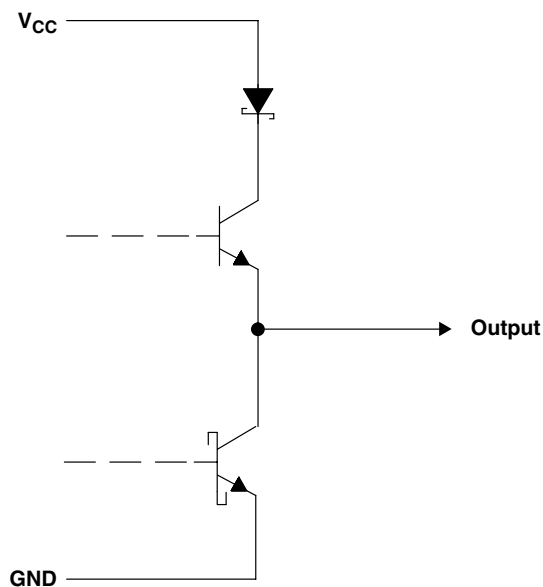
### WITH 3-STATE OUTPUTS

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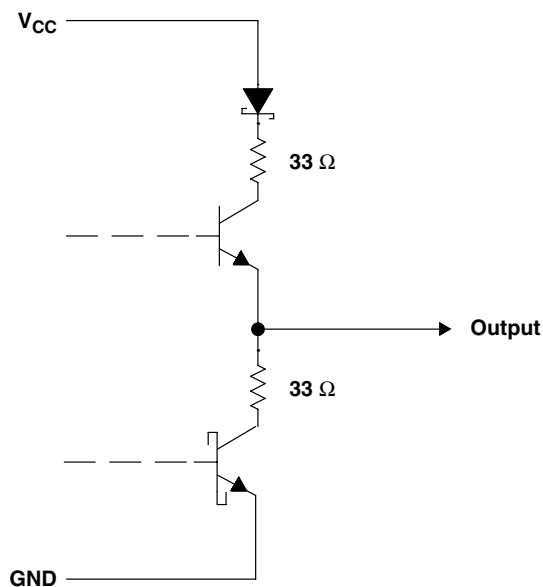
#### logic diagram (positive logic)



#### schematic of A-port outputs



#### schematic of B-port outputs



All resistor values shown are nominal.

# SN74BCT2245

## OCTAL TRANSCEIVER AND LINE/MOS DRIVER

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$	–30 mA
Current into any output in the low state, $I_O$	60 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			–18	mA
$I_{OH}$	High-level output current	A port		–3	mA
		B port		–12	
$I_{OL}$	Low-level output current	A port		24	mA
		B port		12	
$T_A$	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74BCT2245

## OCTAL TRANSCEIVER AND LINE/MOS DRIVER

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2			V
V <sub>OH</sub>	A port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −1 mA	2.5	3.4	V	
			I <sub>OH</sub> = −3 mA	2.4	3.3		
	B port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −1 mA	2.4	3.3		
			I <sub>OH</sub> = −12 mA	2	3.2		
V <sub>OL</sub>	A port	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 24 mA	0.35 0.5			V	
	B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 1 mA	0.5			
			I <sub>OL</sub> = 12 mA	0.8			
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V		0.1			mA
I <sub>IH</sub> ‡	A or B port	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	70			μA	
	Control input		20				
I <sub>IL</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V		−0.65			mA
I <sub>OS</sub> §	A port	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0	−60 −150			mA	
	B port		−100 −225				
I <sub>CCL</sub>	A to B	V <sub>CC</sub> = 5.5 V, Outputs open	63 100			mA	
	B to A		40 64				
I <sub>CCH</sub>	A to B	V <sub>CC</sub> = 5.5 V, Outputs open	37 59			mA	
	B to A		29 46				
I <sub>CCZ</sub>	A to B	V <sub>CC</sub> = 5.5 V, Outputs open	9 15			mA	
	B to A		8 14				
C <sub>i</sub>	Control input	V <sub>CC</sub> = 5 V, V <sub>I</sub> = 2.5 V or 0.5 V		7			pF
C <sub>io</sub>	A to B	V <sub>CC</sub> = 5 V, V <sub>O</sub> = 2.5 V or 0.5 V	9			pF	
	B to A		12				

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

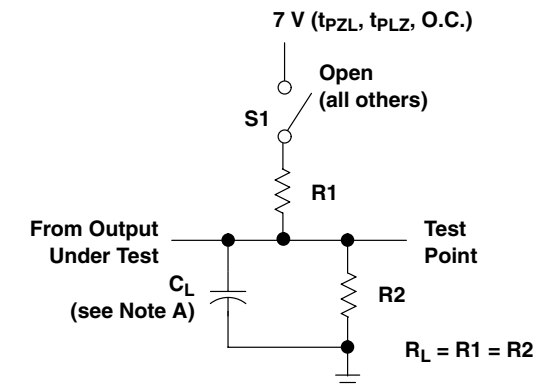
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	B	1	3.3	4.9	1	5.8	ns
	B	A	1.7	4.2	6.1	1.7	7	
$t_{PHL}$	A	B	2.5	5.1	6.9	2.5	7.8	ns
	B	A	2.2	4.7	7.1	2.2	7.7	
$t_{PZH}$	$\overline{OE}$	B	3.2	6.2	8.6	3.2	9.9	ns
		A	3.8	7.2	9.5	3.8	11.1	
$t_{PZL}$	$\overline{OE}$	B	5.6	8.3	10.9	5.6	12.2	ns
		A	4.2	7.6	10.1	4.2	11.4	
$t_{PHZ}$	$\overline{OE}$	B	2.6	5.2	7.1	2.6	8.2	ns
		A	3.1	5.7	8	3.1	9.4	
$t_{PLZ}$	$\overline{OE}$	B	3.5	6	7.9	3.5	9.2	ns
		A	2.3	4.7	6.5	2.3	7.6	



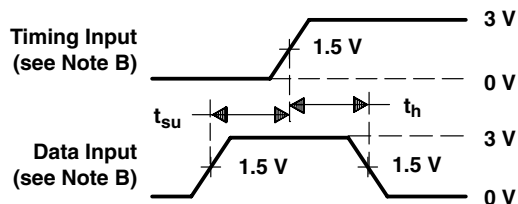
# SN74BCT2245 OCTAL TRANSCEIVER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

SCBS102C – FEBRUARY 1992 – REVISED MARCH 2003

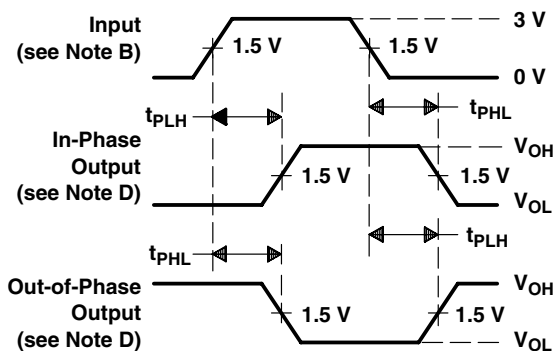
## PARAMETER MEASUREMENT INFORMATION



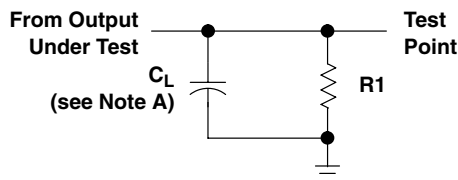
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



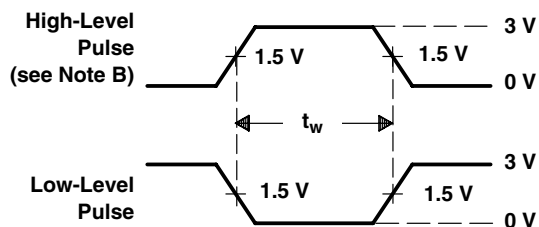
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



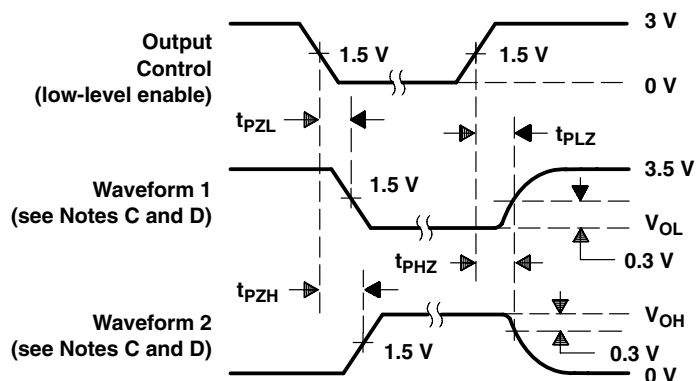
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - The outputs are measured one at a time with one transition per measurement.
  - When measuring propagation delay times of 3-state outputs, switch S1 is open.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74BCT2245DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2245
SN74BCT2245DW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2245
<a href="#">SN74BCT2245NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2245
SN74BCT2245NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2245

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT2245NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT2245NSR	SOP	NS	20	2000	356.0	356.0	45.0



## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74BCT2245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT2245DW.A	DW	SOIC	20	25	507	12.83	5080	6.6

# MECHANICAL DATA

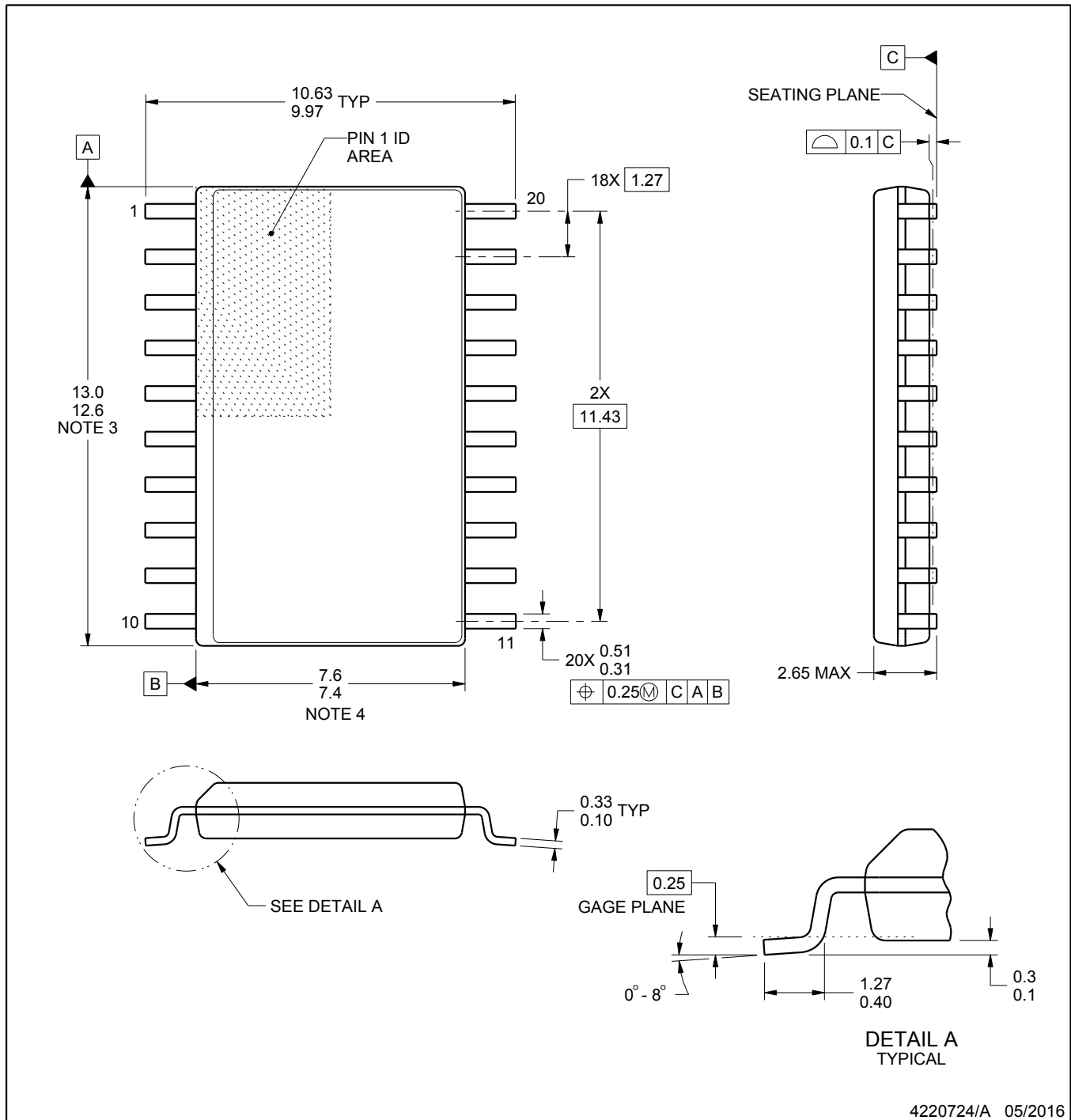
NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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