

## FEATURES

- Transceiver for Memory Card Interface [MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Compliant Products, SmartMedia Card, and xD-Picture Card™]
- Configurable I/O Switching Levels With Dual-Supply Pins Operating Over Full 1.4-V to 3.6-V Power-Supply Range
- For Low-Power Operation, A Ports Are Placed in High-Impedance State When Card-Side Supply Voltage Is Switched Off
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection for Card-Side Pins (B Port)
  - ±15 kV (±12 kV on Pin 14B) – IEC 61000-4-2 ESD, Air-Gap Discharge
  - ±8 kV – IEC 61000-4-2 ESD, Contact Discharge
- ESD Protection for A-Port Pins (Tested Per JESD 22) Exceeds
  - 2000-V Human-Body Model (A114-B)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

The SN74AVCA406 is a transceiver for interfacing microprocessors with MultiMediaCards (MMCs), secure digital (SD) cards, Memory Stick™ compliant products, SmartMedia cards, or xD-Picture Cards™. It integrates high ESD protection, which eliminates the need for external ESD diodes. Two supply-voltage pins allow the A-port and B-port input switching thresholds to be configured separately. The A port is designed to track  $V_{CCA}$ , while the B port is designed to track  $V_{CCB0}$  and  $V_{CCB1}$ .  $V_{CCA}$ ,  $V_{CCB0}$  and  $V_{CCB1}$  can accept any supply voltage from 1.4 V to 3.6 V.

Memory card standards recommend high ESD protection for devices that connect directly to the external memory card. To meet this need, the SN74AVCA406 incorporates ±15-kV air-gap discharge and ±8-kV contact discharge protection on the card side. If  $V_{CCB0}$  and  $V_{CCB1}$  are switched off (no card inserted), the A-port outputs are placed in the high-impedance state to conserve power.

The SN74AVCA406 enables system designers to easily interface low-voltage microprocessors to different memory cards operating at higher voltages. The mode (MODE0 and MODE1) pins are used to configure the device to interface with different types of cards.

The SN74AVCA406 is offered in the 48-ball MicroStar Jr.™ ball grid array (BGA) package. This package has dimensions of 4 × 4 mm, with a 0.5-mm ball pitch for effective board-space savings. Memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, set-top boxes, etc. Low static power consumption and small package size make the SN74AVCA406 an ideal choice for these applications.

## ORDERING INFORMATION

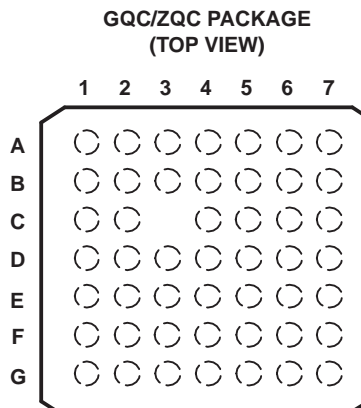
T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGGR	Tape and reel	SN74AVCA406DGGR	AVCA406
	VFBGA – GQC	Tape and reel	SN74AVCA406GQCR	WM406
	VFBGA – ZQC (Pb-free)	Tape and reel	SN74AVCA406ZQCR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



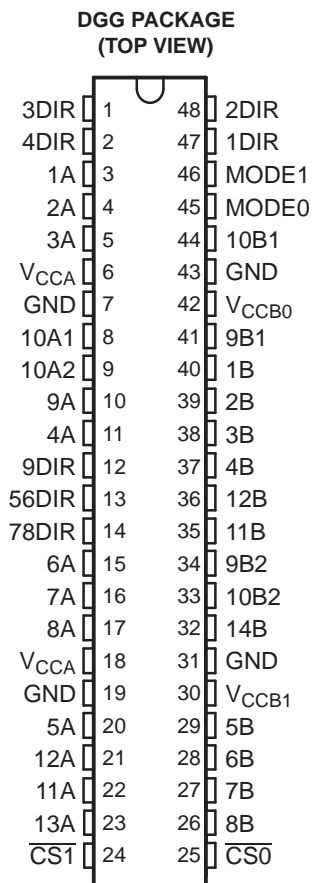
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**TERMINAL ASSIGNMENTS<sup>(1)</sup>**

	1	2	3	4	5	6	7
<b>A</b>	$V_{CCA}$	2A	4DIR	2DIR	MODE1	10B1	$V_{CCB0}$
<b>B</b>	10A1	3A	1A	1DIR	MODE0	9B1	1B
<b>C</b>	9A	10A2		3DIR	GND	2B	3B
<b>D</b>	9DIR	4A	56DIR	GND	4B	11B	12B
<b>E</b>	78DIR	6A	GND	$\overline{CS0}$	GND	10B2	9B2
<b>F</b>	7A	8A	12A	13A	7B	5B	14B
<b>G</b>	$V_{CCA}$	5A	11A	$\overline{CS1}$	8B	6B	$V_{CCB1}$

- (1)  $V_{CCA}$  powers all A-port I/Os and control inputs.  
 $V_{CCB0}$  powers 1B, 2B, 3B, 4B, 9B1, and 10B1.  
 $V_{CCB1}$  powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.



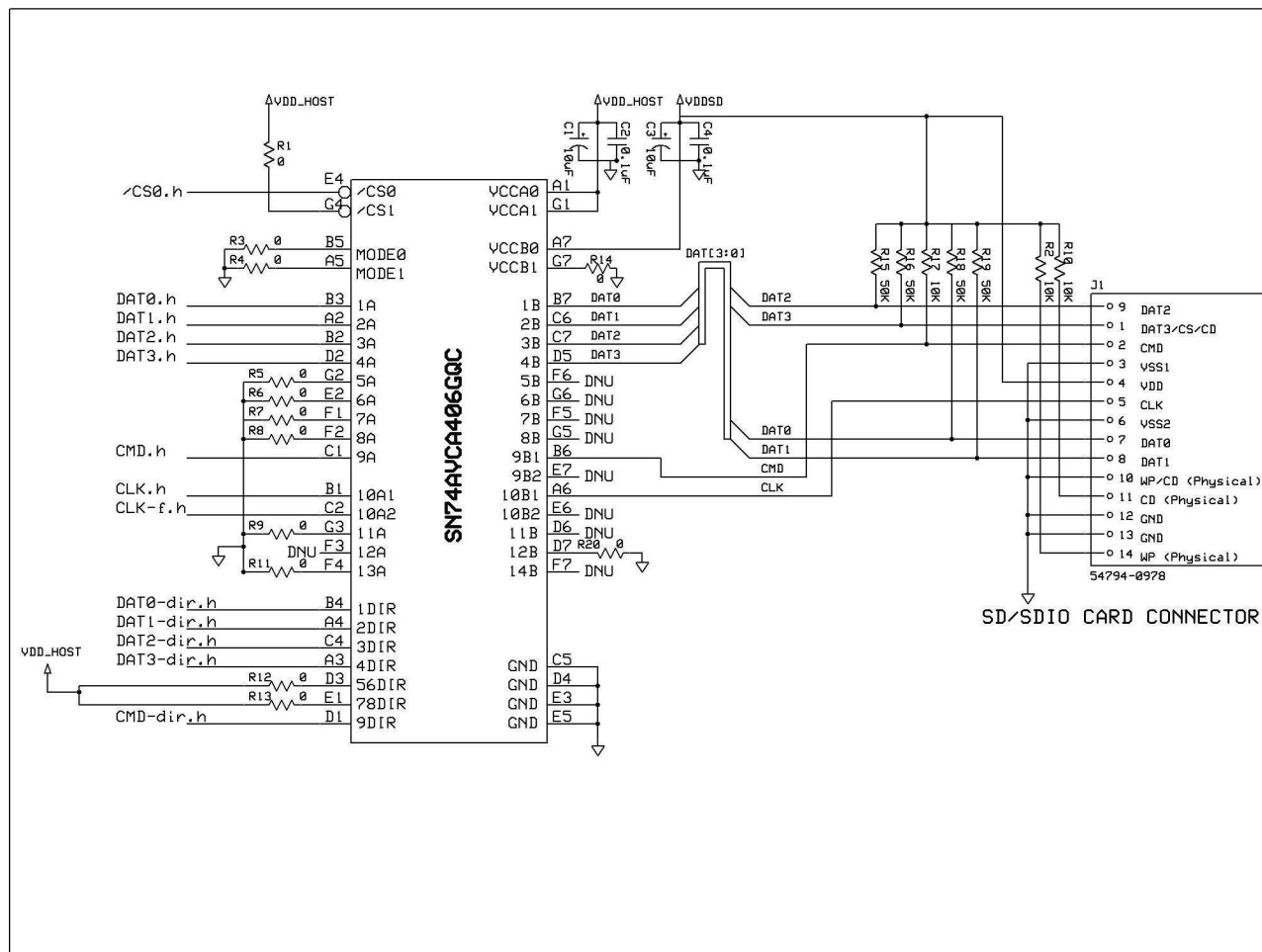
## Device Operation

The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track  $V_{CCB0}$  and  $V_{CCB1}$ .  $V_{CCB0}$  and  $V_{CCB1}$  can accept any supply voltage from 1.4 V to 3.6 V; however,  $V_{CCB0}$ ,  $V_{CCB1}$ , or both must be greater than or equal to  $V_{CCA}$  during normal operation. If  $V_{CCB0}$  and  $V_{CCB1}$  are both at GND, the A port is in the high-impedance state. The control pins are supplied by  $V_{CCA}$ . The microprocessor is connected to the A port, and the memory card(s) are connected to the B port. The device can be configured using MODE0, MODE1,  $\overline{CS0}$ , and  $\overline{CS1}$  pins to interface with 1-bit, 4-bit, or 8-bit memory cards. Outputs 12A and 14B are push-pull and open drain (OD), respectively, except for NAND flash (XD) mode, where they are open drain and push-pull, respectively.

**Table 1. Interface With Different Memory Cards**

MODE0	MODE1	MEMORY-CARD INTERFACE
0	X	SD/SDIO/MMC/Memory Stick/Memory Stick PRO
1	0	8-bit MMC/4-bit + GPIO translation
1	1	SmartMedia/xD-Picture Card

### Configuration 1a – Interfacing With SD or SDIO Card (SD Mode or SD 4-Bit Mode)

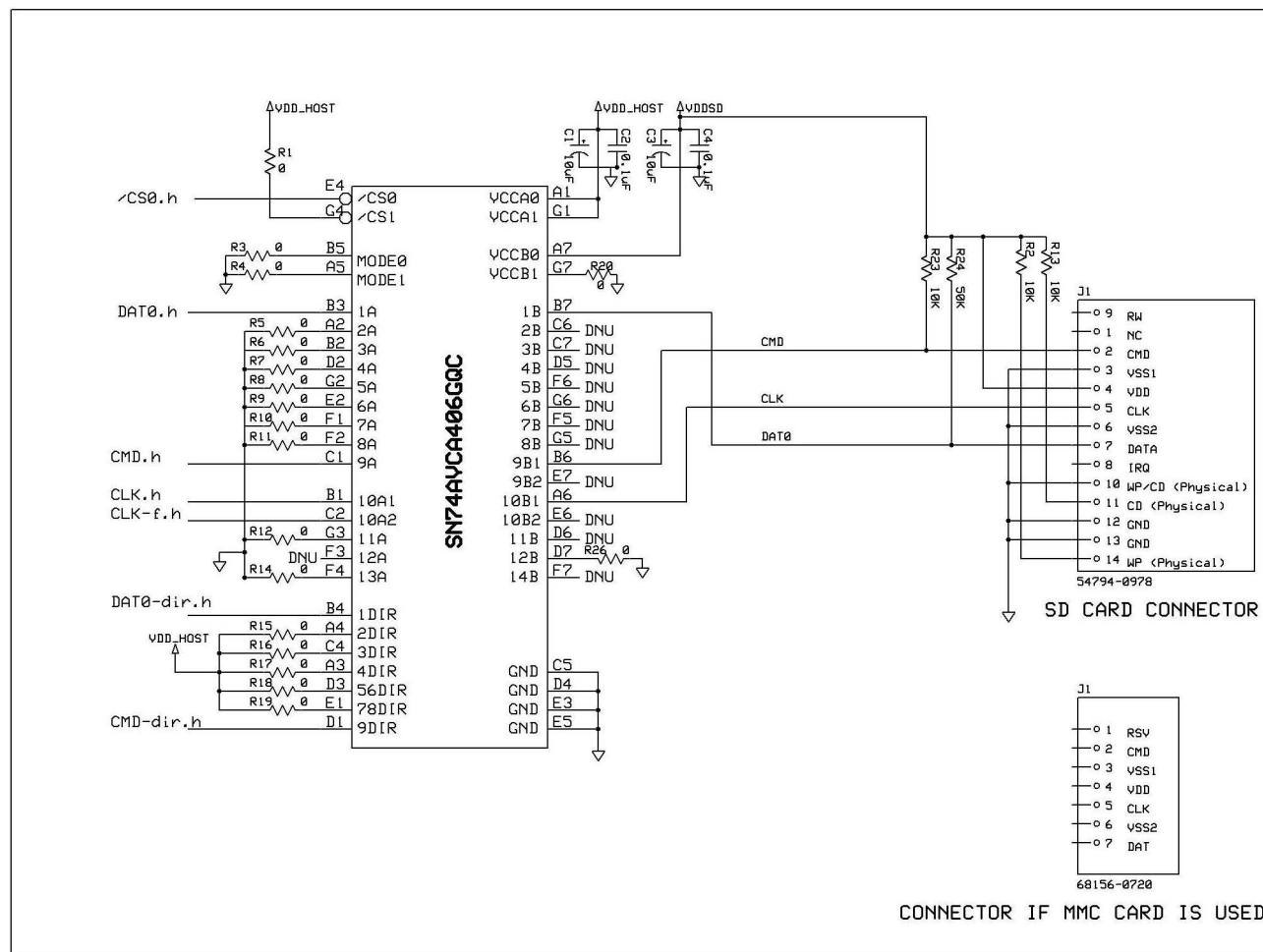


### Table 2. SD or SDIO Card

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	CLK.h	Clock signal from host	Input
C1	9A	CMD.h	Command signal connected to host	I/O
D1	9DIR	CMD-dir.h	Direction control for 9A/9B connected to host	Input
E1	78DIR	(tie-high)	Direction control for 7A/7B and 8A/8B. Not used in this mode. Tie to V <sub>CCA</sub> .	Input
F1	7A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	DAT1.h	Data bit 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	DAT2.h	Data bit 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	CLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	DAT3.h	Data bit 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
F2	8A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G2	5A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O

**Table 2. SD or SDIO Card (continued)**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A3	4DIR	DAT3-dir.h	Direction control for 4A/4B	Input
B3	1A	DAT0.h	Data bit 1 connected to host. Referenced to $V_{CCA}$ .	I/O
C3			Depopulated ball	
D3	56DIR	(tie-high)	Direction control for 5A/5B and 6A/6B. Not used in this mode. Tie to $V_{CCA}$ .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
A4	2DIR	DAT1-dir.h	Direction control for 2A/2B connected to host	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	DAT2-dir.h	Direction control for 3A/3B connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CS0}$ .h	Card select from host. Active low. When $\overline{CS0}$ = high, 1A, 2A, 3A, 4A, 1B, 2B, 3B, 4B, 9A, 9B1, and 10A2 are placed in Hi Z, and 10B1 is low.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	(tie-high)	Card select. Not used in this mode. Tie to $V_{CCA}$ for proper operation.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see <a href="#">Table 1</a> ). Tie to GND in this mode.	Input
B5	MODE0	(tie-low)		Input
C5	GND	GND	Ground	
D5	4B	DAT3	Data bit 4 connected to card. Referenced to $V_{CCB0}$ .	I/O
E5	GND	GND	Ground	
F5	7B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G5	8B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A6	10B1	CLK	Clock signal connected to card	Output
B6	9B1	CMD	Command signal connected to card	Output
C6	2B	DAT1	Data bit 2 connected to card. Referenced to $V_{CCB0}$ .	I/O
D6	11B	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
E6	10B2	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
F6	5B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G6	6B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A7	$V_{CCB0}$	$V_{CCB0}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DAT0	Data bit 1 connected to card. Referenced to $V_{CCB0}$ .	I/O
C7	3B	DAT3	Data bit 3 connected to card. Referenced to $V_{CCB0}$ .	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	(tie-low)	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B. Not used in this mode. Tie to GND.	Power

**Configuration 1b - Interfacing With SD Card or MMC  
(SD 1-Bit Mode or MMC Mode)**

**Table 3. SD Card or MMC**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	CLK.h	Clock signal from host	Input
C1	9A	CMD.h	Command signal connected to host	I/O
D1	9DIR	CMD-dir.h	Direction control for 9A/9B	Input
E1	78DIR	(tie-high)	Direction control for 7A/7B and 8A/8B. Not used in this mode. Tie to V <sub>CCA</sub> .	Input
F1	7A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
B2	3A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
C2	10A2	CLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
E2	6A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
F2	8A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G2	5A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O

**Table 3. SD Card or MMC (continued)**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A3	4DIR	(tie-high)	Direction control for 4A/4B. Not used in this mode. Tie to $V_{CCA}$ .	Input
B3	1A	DAT0.h	Data bit 1 connected to host. Referenced to $V_{CCA}$ .	I/O
C3			Depopulated ball	
D3	56DIR	(tie-high)	Direction control for 5A/5B and 6A/6B. Not used in this mode. Tie to $V_{CCA}$ .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
A4	2DIR	(tie-high)	Direction control for 2A/2B connected to host. Not used in this mode. Tie to $V_{CCA}$ .	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	(tie-high)	Direction control for 3A/3B connected to host. Not used in this mode. Tie to $V_{CCA}$ .	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CS0}$ .h	Card select from host. Active low. When $\overline{CS0}$ = high, 1A, 2A, 3A, 4A, 1B, 2B, 3B, 4B, and 9B1 are placed in Hi Z.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	(tie-high)	Card select. Not used in this mode. Tie to $V_{CCA}$ for proper operation.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see <a href="#">Table 1</a> ). Tie to GND in this mode.	Input
B5	MODE0	(tie-low)		Input
C5	GND	GND	Ground	
D5	4B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
E5	GND	GND	Ground	
F5	7B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G5	8B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A6	10B1	CLK	Clock signal connected to card	Output
B6	9B1	CMD	Command signal connected to card	Output
C6	2B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
D6	11B	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
E6	10B2	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
F6	5B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G6	6B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A7	$V_{CCB0}$	$V_{CCB0}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DAT0	Data bit 1 connected to card. Referenced to $V_{CCB0}$ .	I/O
C7	3B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	(tie-low)	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B. Not used in this mode. Tie to GND.	Power



### Configuration 1c - Interfacing With SD/SDIO Card or MMC (SPI Mode)

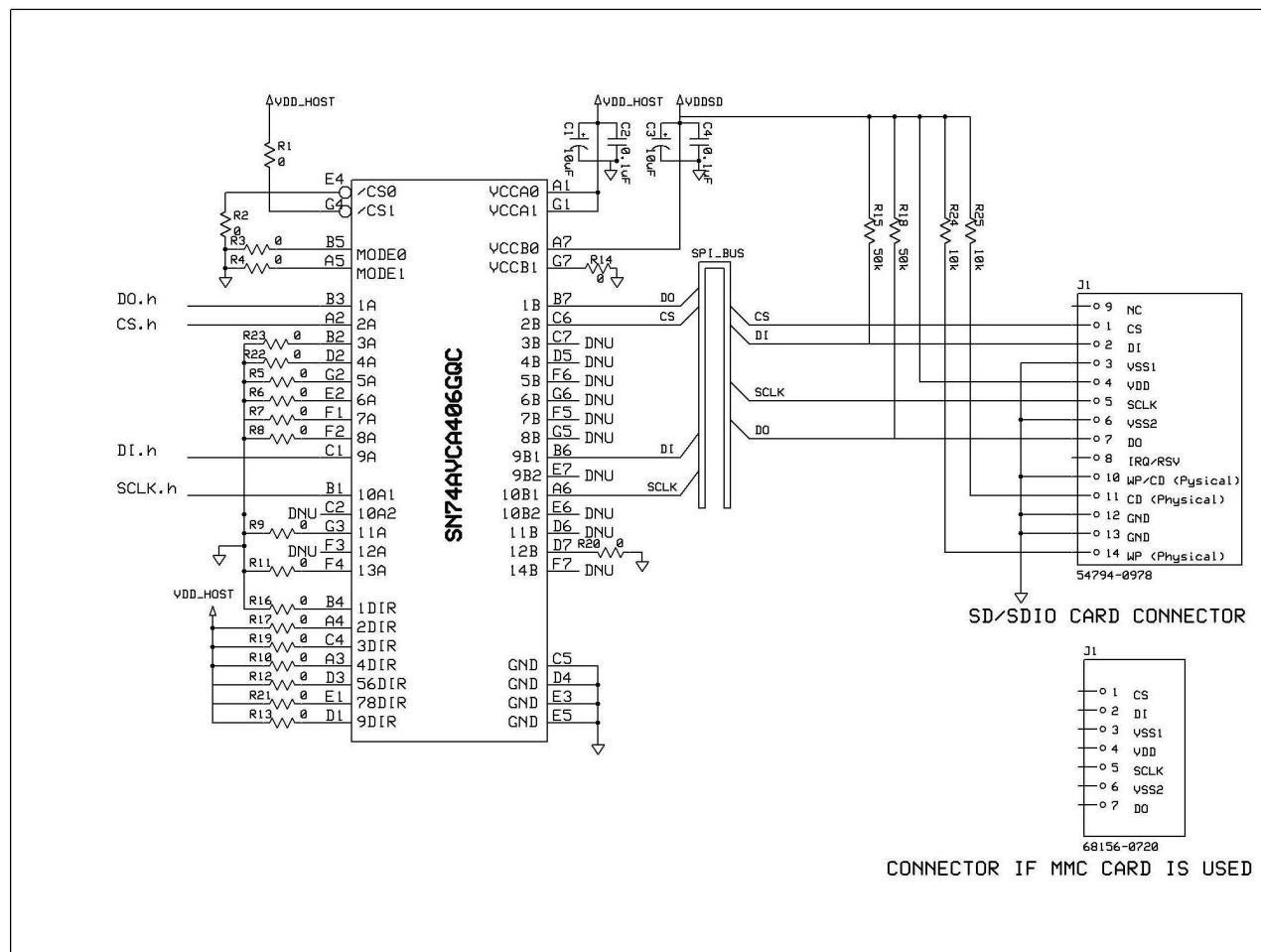


Table 4. SD/SDIO Card or MMC

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	SCLK.h	Serial clock signal from host	Input
C1	9A	DI.h	Serial data in (master out slave in) connected to host. Connect 9DIR to V <sub>CCA</sub> to make 9A an input.	I/O
D1	9DIR	(tie-high)	Direction control for 9A/9B. Tie high to make 9A an input and 9B an output.	Input
E1	78DIR	(tie-high)	Direction control for 7A/7B and 8A/8B. Not used in this mode. Tie to V <sub>CCA</sub> .	Input
F1	7A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	CS.h	Card select connected to host. Connect 2DIR to V <sub>CCA</sub> to make 2A an input.	I/O
B2	3A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
C2	10A2	DNU	Clock feedback to host. Not used in this mode. Leave unconnected.	Output
D2	4A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
E2	6A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
F2	8A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G2	5A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O



**Table 4. SD/SDIO Card or MMC (continued)**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A3	4DIR	(tie-high)	Direction control for 4A/4B. Not used in this mode. Tie to $V_{CCA}$ .	Input
B3	1A	DO.h	Serial data out (master in slave out) connected to host. Connect 1DIR to GND to make 1A an output.	I/O
C3	Depopulated ball			
D3	56DIR	(tie-high)	Direction control for 5A/5B and 6A/6B. Not used in this mode. Tie to $V_{CCA}$ .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
A4	2DIR	(tie-high)	Direction control for 2A/2B. Tie to $V_{CCA}$ to make 2A an input and 2B an output.	Input
B4	1DIR	(tie-low)	Direction control for 1A/1B. Tie to GND to make 1B an input and 1A an output.	Input
C4	3DIR	(tie-high)	Direction control for 3A/3B. Not used in this mode. Tie to $V_{CCA}$ .	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	(tie-low)	Card select signal. Not used in this mode. For proper operation, tie to GND.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	(tie-HIGH)	Card select. Not used in this mode. For proper operation, tie to $V_{CCA}$ .	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see Table 1). Tie to GND in this mode.	Input
B5	MODE0	(tie-low)		Input
C5	GND	GND	Ground	
D5	4B	DNU	Card select connected to card. Connect 2DIR to $V_{CCA}$ to make 2B an output.	I/O
E5	GND	GND	Ground	
F5	7B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G5	8B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A6	10B1	SCLK	Serial clock signal connected to card	Output
B6	9B1	DI	Serial data in (master out slave in) connected to card	Output
C6	2B	CS	I/O pin not used in this mode. Leave unconnected.	I/O
D6	11B	DNU	Output pin not used in this mode. Leave unconnected.	Output
E6	10B2	DNU	Output pin not used in this mode. Leave unconnected.	Output
F6	5B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G6	6B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A7	$V_{CCB0}$	$V_{CCB0}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DO	Serial data out (master in slave out) connected to host. Connect 1DIR to GND to make 1B an input.	I/O
C7	3B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	(tie-low)	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B. Not used in this mode. Tie to GND.	Power

# SN74AVCA406

## MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card

### ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANSCEIVER

SCES615H–OCTOBER 2004–REVISED JANUARY 2007

#### Configuration 1d - Interfacing With SDIO Card in Slot 0 and SD Card (4-bit Mode) in Slot 1

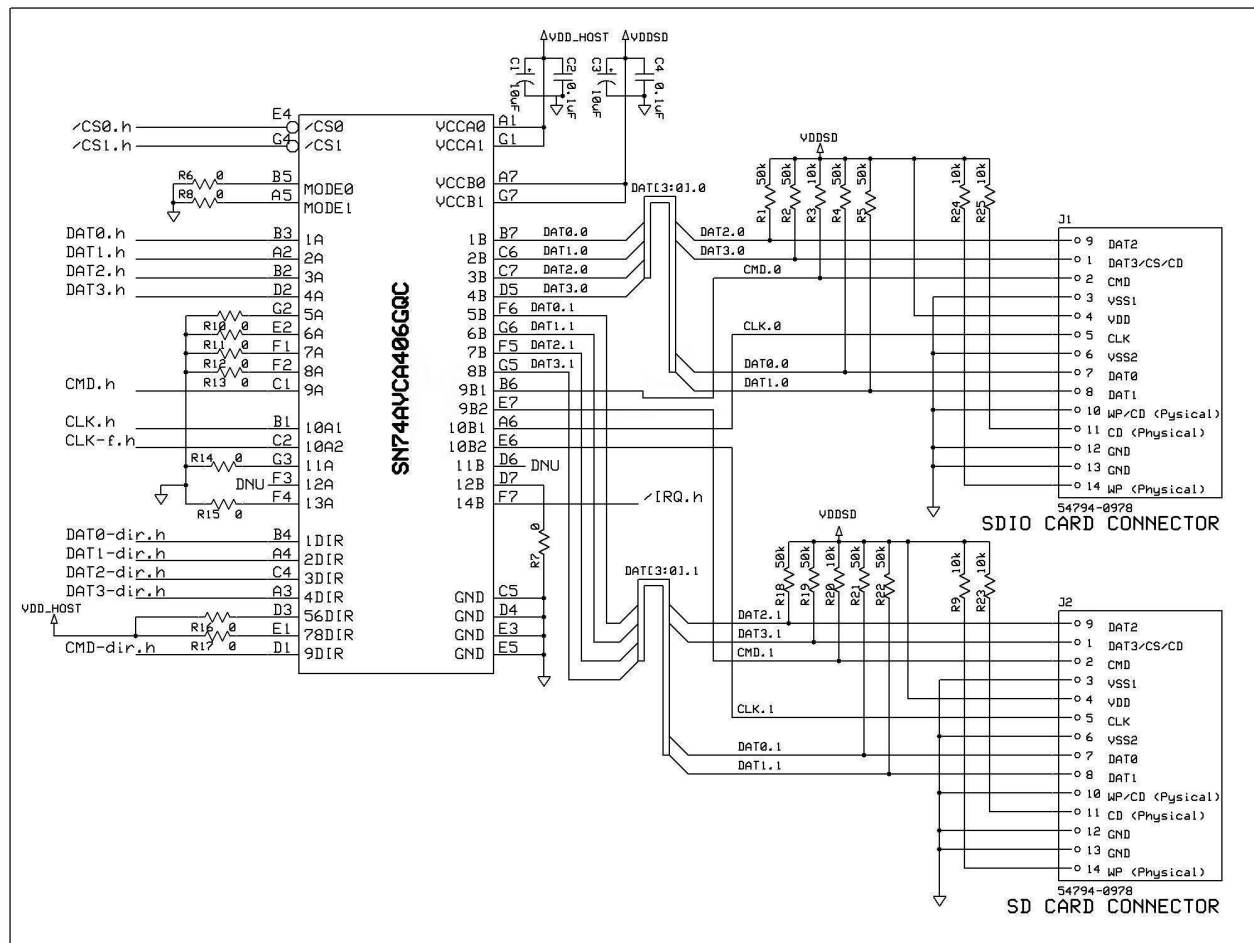


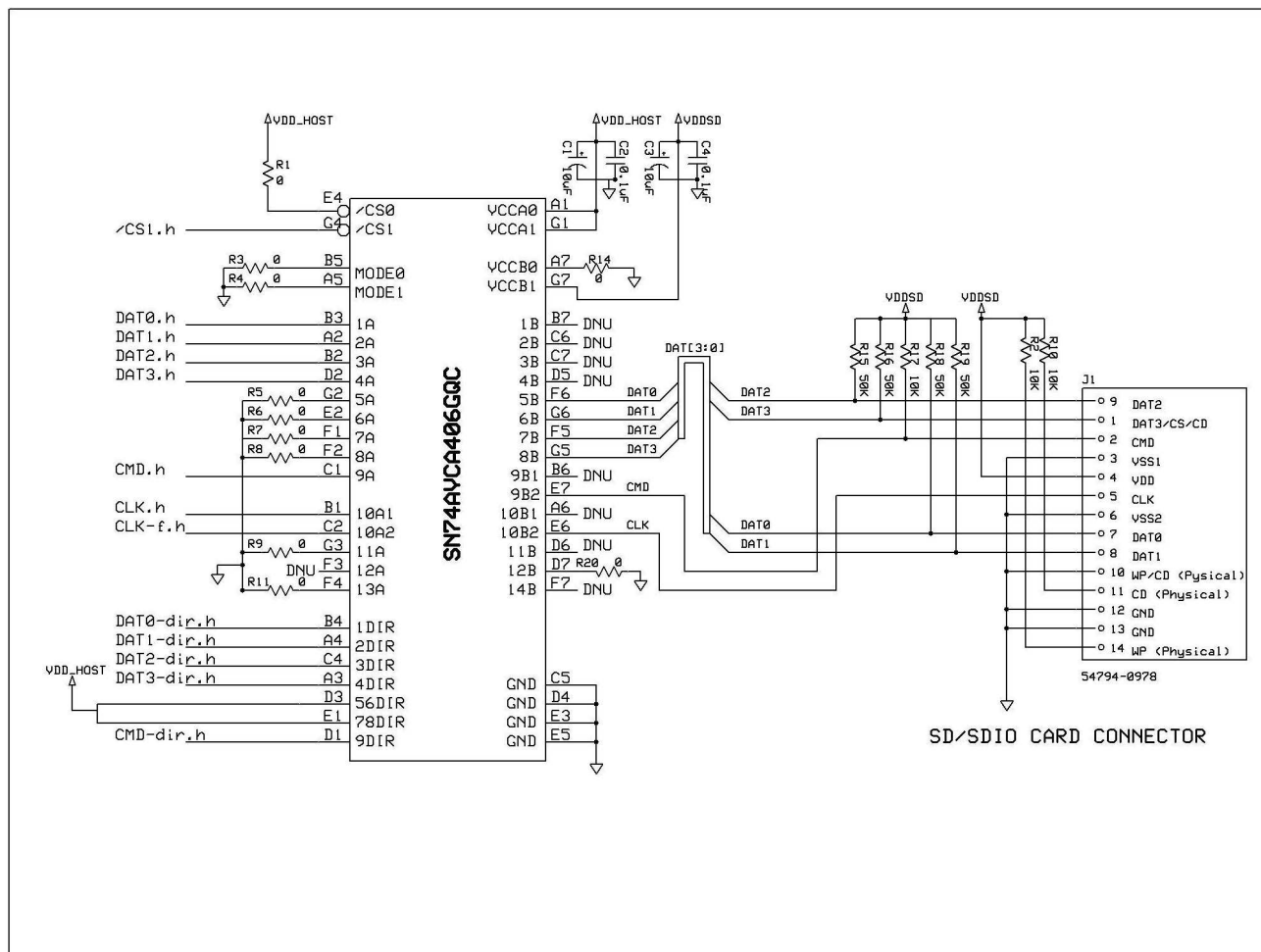
Table 5. SDIO Card (Slot 0) and SD Card (Slot 1)

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	CLK.h	Clock signal from host	Input
C1	9A	CMD.h	Command signal connected to host	I/O
D1	9DIR	CMD-dir.h	Direction control for 9A/9B connected to host	Input
E1	78DIR	(tie-high)	Direction control for 7A/7B and 8A/8B. Not used in this mode. Tie to V <sub>CCA</sub> .	Input
F1	7A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	DAT1.h	Data bit 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	DAT2.h	Data bit 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	CLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	DAT3.h	Data bit 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
F2	8A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G2	5A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
A3	4DIR	DAT3-dir.h	Direction control for 4A/4B	Input

**Table 5. SDIO Card (Slot 0) and SD Card (Slot 1) (continued)**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
B3	1A	DAT0.h	Data bit 1 connected to host. Referenced to $V_{CCA}$ .	I/O
C3			Depopulated ball	
D3	56DIR	(tie-high)	Direction control for 5A/5B and 6A/6B. Not used in this mode. Tie to $V_{CCA}$ .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND	Input
A4	2DIR	DAT1-dir.h	Direction control for 2A/2B connected to host	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	DAT2-dir.h	Direction control for 3A/3B connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CS0}.h$	Card select from host. Active low. When $\overline{CS0}$ = high, 1A, 2A, 3A, 4A, 1B, 2B, 3B, 4B, and 9B1 are placed in Hi Z, and 10B1 is low.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	$\overline{CS1}.h$	Card select from host. Active low. When $\overline{CS1}$ = high, 5A, 6A, 7A, 8A, 5B, 6B, 7B, 8B, 7B, and 9B2 are placed in Hi Z, and 10B2 is low.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see Table 1). Tie to GND in this mode.	Input
B5	MODE0	(tie-low)		Input
C5	GND	GND	Ground	
D5	4B	DAT3.0	Data bit 4 connected to card in slot 0. Referenced to $V_{CCB0}$ .	I/O
E5	GND	GND	Ground	
F5	7B	DAT2.1	Data bit 3 connected to card in slot 1. Referenced to $V_{CCB1}$ .	I/O
G5	8B	DAT3.1	Data bit 4 connected to card in slot 1. Referenced to $V_{CCB1}$ .	I/O
A6	10B1	CLK.0	Clock signal connected to card in slot 0	Output
B6	9B1	CMD.0	Command signal connected to card in slot 0	Output
C6	2B	DAT1.0	Data bit 2 connected to card in slot 0. Referenced to $V_{CCB0}$ .	I/O
D6	11B	DNU	Output pin not used in this mode. Leave unconnected.	Output
E6	10B2	CLK.1	Clock signal connected to card in slot 1	Output
F6	5B	DAT0.1	Data bit 1 connected to card in slot 1. Referenced to $V_{CCB1}$ .	I/O
G6	6B	DAT1.1	Data bit 2 connected to card in slot 1. Referenced to $V_{CCB1}$ .	I/O
A7	$V_{CCB0}$	$V_{CCB0}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DAT0.0	Data bit 1 connected to card in slot 0. Referenced to $V_{CCB0}$ .	I/O
C7	3B	DAT2.0	Data bit 3 connected to card in slot 0. Referenced to $V_{CCB0}$ .	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	CMD.1	Command signal connected to card in slot 1	I/O
F7	14B	$\overline{IRQ}.h$	Open-drain interrupt output for dual SDIO cards configuration. DAT1 is the input for interrupt.	Output
G7	$V_{CCB1}$	$V_{CCB1}$	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.	Power

**Configuration 1e - Alternate Method of Interfacing With SD/SDIO Card**  
**(SD Mode or SD 4-bit Mode)**

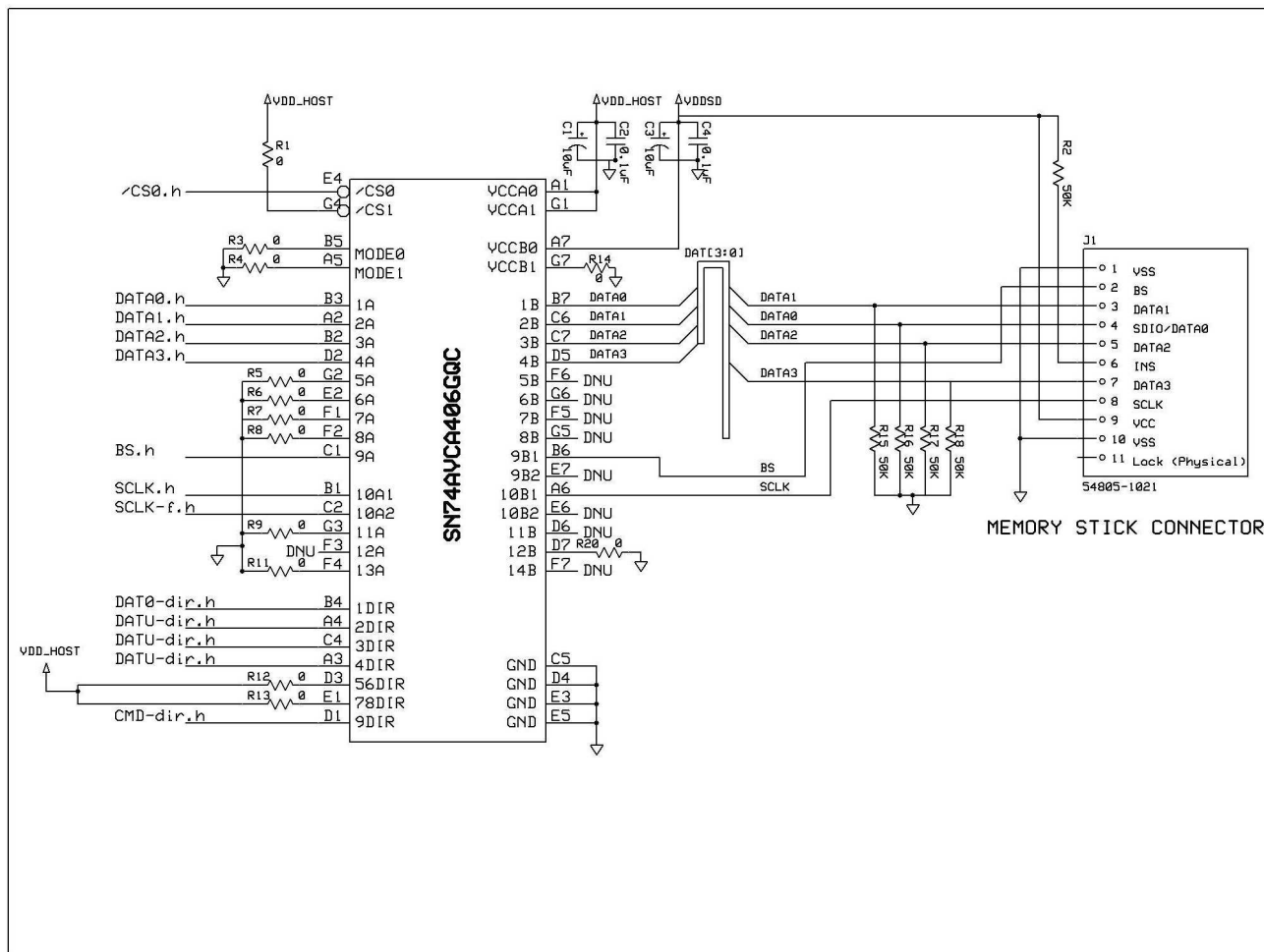


**Table 6. Alternate SD/SDIO Card**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	CLK.h	Clock signal from host	Input
C1	9A	CMD.h	Command signal connected to host	I/O
D1	9DIR	CMD-dir.h	Direction control for 9A/9B connected to host	Input
E1	78DIR	(tie-high)	Direction control for 7A/7B and 8A/8B. Not used in this mode. Tie to V <sub>CCA</sub> .	Input
F1	7A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	DAT1.h	Data bit 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	DAT2.h	Data bit 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	CLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	DAT3.h	Data bit 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
F2	8A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G2	5A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O

**Table 6. Alternate SD/SDIO Card (continued)**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A3	4DIR	DAT3-dir.h	Direction control for 4A/4B	Input
B3	1A	DAT0.h	Data bit 1 connected to host. Referenced to $V_{CCA}$ .	I/O
C3			Depopulated ball	
D3	56DIR	(tie-high)	Direction control for 5A/5B and 6A/6B. Not used in this mode. Tie to $V_{CCA}$ .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
A4	2DIR	DAT1-dir.h	Direction control for 2A/2B connected to host	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	DAT2-dir.h	Direction control for 3A/3B connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	(tie-high)	Card select signal. Not used in this mode. Tie to $V_{CCA}$ for proper operation.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	$\overline{CS1}$	Card select from host. Active low. When $\overline{CS1}$ = high, 1A, 2A, 3A, 4A, 5B, 6B, 7B, 8B, 9A, 9B2, and 10A2 are placed in Hi Z, and 10B1 is low.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see Table 1). Tie to GND in this mode.	Input
B5	MODE0	(tie-low)		Input
C5	GND	GND	Ground	
D5	4B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
E5	GND	GND	Ground	
F5	7B	DAT2	Data bit 3 connected to card. Referenced to $V_{CCB1}$ .	I/O
G5	8B	DAT3	Data bit 4 connected to card. Referenced to $V_{CCB1}$ .	I/O
A6	10B1	DNU	Output pin not used in this mode. Leave unconnected.	Output
B6	9B1	DNU	Output pin not used in this mode. Leave unconnected.	Output
C6	2B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
D6	11B	DNU	Output pin not used in this mode. Leave unconnected.	Output
E6	10B2	CLK	Clock signal connected to card	Output
F6	5B	DAT0	Data bit 1 connected to card. Referenced to $V_{CCB1}$ .	I/O
G6	6B	DAT1	Data bit 2 connected to card. Referenced to $V_{CCB1}$ .	I/O
A7	$V_{CCB0}$	(tie-low)	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1. Not used in this mode. Tie to GND.	Power
B7	1B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
C7	3B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	CMD	Command signal connected to card	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	$V_{CCB1}$	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.	Power

**Configuration 1f - Interfacing With Memory Stick**

**Table 7. Memory Stick**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	SCLK.h	Clock signal from host	Input
C1	9A	BS.h	Bus state connected to host	I/O
D1	9DIR	(tie-high)	Direction control for 9A/9B connected to host. Tie high to make 9A an input, 9B an output.	Input
E1	78DIR	(tie-high)	Direction control for 7A/7B and 8A/8B. Not used in this mode. Tie to V <sub>CCA</sub> .	Input
F1	7A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	DATA1.h	Data bit 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	DATA2.h	Data bit 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	SCLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	DATA3.h	Data bit 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
F2	8A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O
G2	5A	(tie-low)	I/O pin not used in this mode. Tie to GND.	I/O

**Table 7. Memory Stick (continued)**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A3	4DIR	DATU-dir.h	Direction control for 4A/4B	Input
B3	1A	DATA0.h	Data bit 1 connected to host. Referenced to $V_{CCA}$ .	I/O
C3			Depopulated ball	
D3	56DIR	(tie-high)	Direction control for 5A/5B and 6A/6B. Not used in this mode. Tie to $V_{CCA}$ .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
A4	2DIR	DATU-dir.h	Direction control for 2A/2B connected to host	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	DATU-dir.h	Direction control for 3A/3B connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CS0}$ .h	Card select from host. Active low. When $\overline{CS0}$ = high, 1A, 2A, 3A, 4A, 1B, 2B, 3B, 4B, 9A, 9B1, and 10A2 are placed in Hi Z, and 10B1 is low.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	(tie-high)	Card select signal. Not used in this mode. Tie to $V_{CCA}$ for proper operation.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see Table 1). Tie to GND in this mode.	Input
B5	MODE0	(tie-low)		Input
C5	GND	GND	Ground	
D5	4B	DATA3	Data bit 4 connected to card. Referenced to $V_{CCB0}$ .	I/O
E5	GND	GND	Ground	
F5	7B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G5	8B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A6	10B1	SCLK	Clock signal connected to card	Output
B6	9B1	BS	Bus state signal connected to card	Output
C6	2B	DATA1	Data bit 2 connected to card. Referenced to $V_{CCB0}$ .	I/O
D6	11B	DNU	Output pin not used in this mode. Leave unconnected.	Output
E6	10B2	DNU	Output pin not used in this mode. Leave unconnected.	Output
F6	5B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
G6	6B	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
A7	$V_{CCB0}$	$V_{CCB0}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DATA0	Data bit 1 connected to card. Referenced to $V_{CCB0}$ .	I/O
C7	3B	DATA2	Data bit 3 connected to card. Referenced to $V_{CCB0}$ .	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	(tie-low)	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B. Not used in this mode. Tie to GND.	Power

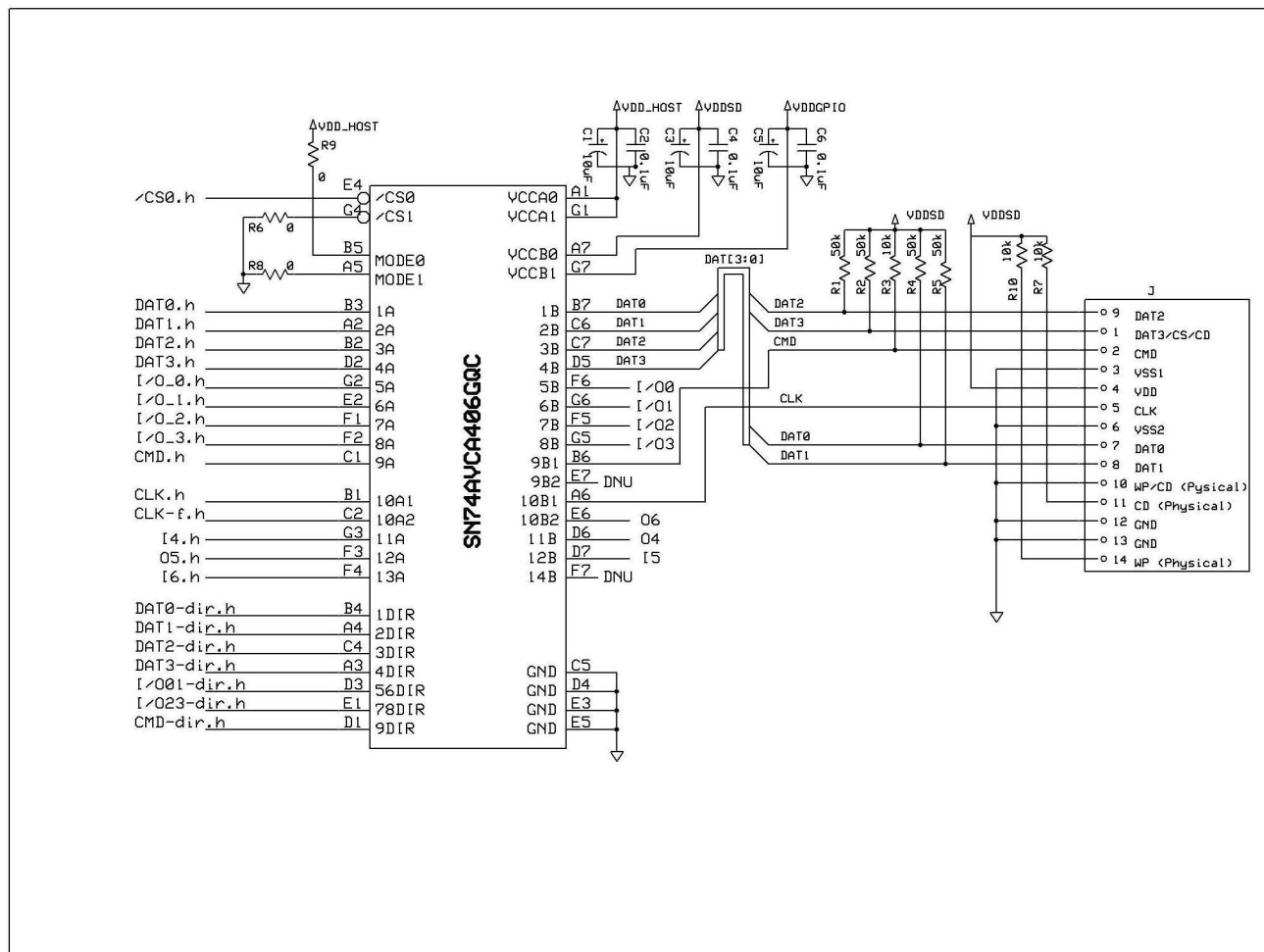


**CONFIGURATION 1 FUNCTION TABLE**  
(MODE0 = L, MODE1 = L)

SIGNAL	INPUTS				OPERATION	
	$\overline{CS0}$	$\overline{CS1}$	9DIR	(1-4)DIR	MMC/SD	Memory Stick/Memory Stick PRO
Clock	H	H	X	X	CLK.0 and CLK.1 forced low, CLK-f.h forced Hi Z	SCLK.0 and SCLK.1 forced low, SCLK-f.h forced Hi Z
	L	L	X	X	CLK.h to CLK.0 and CLK.1, CLK.0 to CLK-f.h	SCLK.h to SCLK.0 and SCLK.1, SCLK.0 to SCLK-f.h
	L	H	X	X	CLK.h to CLK.0, CLK.0 to CLK-f.h, CLK.1 forced low	SCLK.h to SCLK.0, SCLK.0 to SCLK-f.h, SCLK.1 forced low
	H	L	X	X	CLK.h to CLK.1, CLK.1 to CLK-f.h, CLK.0 forced low	SCLK.h to SCLK.1, SCLK.1 to SCLK-f.h, SCLK.0 forced low
Data	H	H	X	X	All data I/Os are Hi Z (isolation mode).	All data I/Os are Hi Z (isolation mode).
	L <sup>(1)</sup>	L <sup>(1)</sup>	X	L	DAT0.0 and DAT0.1 to DAT0.h, DAT1.0 and DAT1.1 to DAT1.h, DAT2.0 and DAT2.1 to DAT2.h, DAT3.0 and DAT3.1 to DAT3.h	DATA0.0 and DATA0.1 to DATA0.h, DATA1.0 and DATA1.1 to DATA1.h, DATA2.0 and DATA2.1 to DATA2.h, DATA3.0 and DATA3.1 to DATA3.h
	L <sup>(1)</sup>	L <sup>(1)</sup>	X	H	DAT0.h to DAT0.0 and to DAT0.1, DAT1.h to DAT1.0 and to DAT1.1, DAT2.h to DAT2.0 and to DAT2.1, DAT3.h to DAT3.0 and to DAT3.1	DATA0.h to DATA0.0 and to DATA0.1, DATA1.h to DATA1.0 and to DATA1.1, DATA2.h to DATA2.0 and to DATA2.1, DATA3.h to DATA3.0 and to DATA3.1
	L	H	X	L	DAT0.0 to DAT0.h, DAT1.0 to DAT1.h, DAT2.0 to DAT2.h, DAT3.0 to DAT3.h	DATA0.0 to DATA0.h, DATA1.0 to DATA1.h, DATA2.0 to DATA2.h, DATA3.0 to DATA3.h
	L	H	X	H	DAT0.h to DAT0.0, DAT1.h to DAT1.0, DAT2.h to DAT2.0, DAT3.h to DAT3.0	DATA0.h to DATA0.0, DATA1.h to DATA1.0, DATA2.h to DATA2.0, DATA3.h to DATA3.0
	H	L	X	L	DAT0.1 to DAT0.h, DAT1.1 to DAT1.h, DAT2.1 to DAT2.h, DAT3.1 to DAT3.h	DATA0.1 to DATA0.h, DATA1.1 to DATA1.h, DATA2.1 to DATA2.h, DATA3.1 to DATA3.h
	H	L	X	H	DAT0.h to DAT0.1, DAT1.h to DAT1.1, DAT2.h to DAT2.1, DAT3.h to DAT3.1	DATA0.h to DATA0.1, DATA1.h to DATA1.1, DATA2.h to DATA2.1, DATA3.h to DATA3.1
Command	H	H	X	X	CMD.h, CMD.0, and CMD.1 are Hi Z (isolation mode).	BS.h, BS.0, and BS.1 are Hi Z (isolation mode).
	L	L	H	X	CMD.h to CMD.0 and CMD.1	BS.h to BS.0 and BS.1
	L	L	L	X	CMD.0 and CMD.1 to CMD.h	BS.0 and BS.1 to BS.h
	L	H	H	X	CMD.h to CMD.0	BS.h to BS.0
	L	H	L	X	CMD.0 to CMD.h	BS.0 to BS.h
	H	L	H	X	CMD.h to CMD.1	BS.h to BS.1
	H	L	L	X	CMD.1 to CMD.h	BS.1 to BS.h
Interrupt request	H	H	X	X	DAT1.0 and DAT1.1 to $\overline{IRQ}$ . $\overline{IRQ}$ is an open-drain output.	DATA1.0 and DATA1.1 to $\overline{IRQ}$ . $\overline{IRQ}$ is an open-drain output.
	L	H	X	X	DAT1.1 to $\overline{IRQ}$ . $\overline{IRQ}$ is an open-drain output.	DATA1.1 to $\overline{IRQ}$ . $\overline{IRQ}$ is an open-drain output.
	H	L	X	X	DAT1.0 to $\overline{IRQ}$ . $\overline{IRQ}$ is an open-drain output.	DATA1.0 to $\overline{IRQ}$ . $\overline{IRQ}$ is an open-drain output.
	L	L	X	X	$\overline{IRQ}$ is Hi Z.	$\overline{IRQ}$ is Hi Z.

(1) Broadcast mode in which the host writes to or reads from both cards in parallel

## Configuration 2 - Interfacing With SD/SDIO Card and Using GPIOs for Level Shifting



**Table 8. SD/SDIO Card Using GPIOs for Level Shifting**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	CLK.h	Clock signal from host	Input
C1	9A	CMD.h	Command signal connected to host	I/O
D1	9DIR	CMD-dir.h	Direction control for 9A/9B connected to host	Input
E1	78DIR	I/O23-dir.h	Direction control for 7A/7B and 8A/8B. Connected to host. Tie to V <sub>CCA</sub> if unused.	Input
F1	7A	I/O2.h	General-purpose I/O. Referenced to V <sub>CCA</sub> . Tie to V <sub>CCA</sub> or GND if unused.	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	DAT1.h	Data bit 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	DAT2.h	Data bit 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	CLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	DAT3.h	Data bit 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	I/O1.h	General-purpose I/O. Referenced to V <sub>CCA</sub> . Tie to V <sub>CCA</sub> or GND if unused.	I/O
F2	8A	I/O3.h	General-purpose I/O. Referenced to V <sub>CCA</sub> . Tie to V <sub>CCA</sub> or GND if unused.	I/O
G2	5A	I/O0.h	General-purpose I/O. Referenced to V <sub>CCA</sub> . Tie to V <sub>CCA</sub> or GND if unused.	I/O

Table 8. SD/SDIO Card Using GPIOs for Level Shifting (continued)

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A3	4DIR	DAT3-dir.h	Direction control for 4A/4B	Input
B3	1A	DAT0.h	Data bit 1 connected to host. Referenced to $V_{CCA}$ .	I/O
C3			Depopulated ball	
D3	56DIR	I/O01-dir.h	Direction control for 5A/5B and 6A/6B. Referenced to $V_{CCA}$ . Tie to $V_{CCA}$ if unused.	Input
E3	GND	GND	Ground	
F3	12A	O5.h	General-purpose output connected to host. Referenced to $V_{CCA}$ .	Output
G3	11A	I4.h	General-purpose input connected to host. Referenced to $V_{CCA}$ .	Input
A4	2DIR	DAT1-dir.h	Direction control for 2A/2B connected to host	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	DAT2-dir.h	Direction control for 3A/3B connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CS0}$ .h	Card select from host. Active low. When $\overline{CS0}$ = high, 1A, 2A, 3A, 4A, 1B, 2B, 3B, 4B, 9A, 9B, and 10A2 are placed in Hi Z, and 10B1 is low.	Input
F4	13A	I6.h	General-purpose input connected to host. Referenced to $V_{CCA}$ .	Input
G4	$\overline{CS1}$	(tie-low)	Card select. Tie to GND for proper operation.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see Table 1).	Input
B5	MODE0	(tie-high)	Tie MODE0 to $V_{CCA}$ . Tie MODE1 to GND.	Input
C5	GND	GND	Ground	
D5	4B	DAT3	Data bit 4 connected to card. Referenced to $V_{CCB0}$ .	I/O
E5	GND	GND	Ground	
F5	7B	I/O2	General-purpose I/O. Referenced to $V_{CCB1}$ .	I/O
G5	8B	I/O3	General-purpose I/O. Referenced to $V_{CCB1}$ .	I/O
A6	10B1	CLK	Clock signal connected to card	Output
B6	9B1	CMD	Command signal connected to card	Output
C6	2B	DAT1	Data bit 2 connected to card. Referenced to $V_{CCB0}$ .	I/O
D6	11B	O4	General-purpose output. Referenced to $V_{CCB1}$ .	Output
E6	10B2	O6	General-purpose output. Referenced to $V_{CCB1}$ .	Output
F6	5B	I/O0	General-purpose I/O. Referenced to $V_{CCB1}$ .	I/O
G6	6B	I/O1	General-purpose I/O. Referenced to $V_{CCB1}$ .	I/O
A7	$V_{CCB0}$	$V_{CCB0}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DAT0	Data bit 1 connected to card. Referenced to $V_{CCB0}$ .	I/O
C7	3B	DAT2	Data bit 3 connected to card. Referenced to $V_{CCB0}$ .	I/O
D7	12B	I5	General-purpose input. Referenced to $V_{CCB1}$ .	Input
E7	9B2	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	$V_{CCB1}$	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.	Power

**CONFIGURATION 2 FUNCTION TABLE**  
(MODE0 = H, MODE1 = L)

SIGNAL	INPUTS						OPERATION	
	$\overline{CS0}$	$\overline{CS1}$	9DIR	(1-4)DIR	56DIR	78DIR	MMC/SD	Memory Stick/ Memory Stick PRO
Clock	H	H	X	X	X	X	CLK forced low, CLK-f.h forced Hi Z	SCLK forced low, SCLK-f.h forced Hi Z
	L	L	X	X	X	X	CLK.h to CLK, CLK to CLK-f.h	SCLK.h to SCLK, SCLK to SCLK-f.h
Data	H	H	X	X	X	X	All data I/Os are Hi Z (isolation mode).	All data I/Os are Hi Z (isolation mode).
	L	L	X	L	X	X	DAT0 to DAT0.h, DAT1 to DAT1.h, DAT2 to DAT2.h, DAT3 to DAT3.h	DATA0 to DATA0.h, DATA1 to DATA1.h, DATA2 to DATA2.h, DATA3 to DATA3.h
	L	L	X	H	X	X	DAT0.h to DAT0, DAT1.h to DAT1, DAT2.h to DAT2, DAT3.h to DAT3	DATA0.h to DATA0, DATA1.h to DATA1, DATA2.h to DATA2, DATA3.h to DATA3
Command	H	H	X	X	X	X	CMD.h and CMD are Hi Z (isolation mode).	BS.h and BS are Hi Z (isolation mode).
	L	L	L	X	X	X	CMD to CMD.h	BS to BS.h
	L	L	H	X	X	X	CMD.h to CMD	BS.h to BS
GPIO	H	H	X	X	X	X	All GPIOs are Hi Z.	All GPIOs are Hi Z.
	L	L	X	X	X	X	I4 to O4, I5 to O5, I6 to O6	I4 to O4, I5 to O5, I6 to O6
	L	L	X	X	L	X	I/O0 to I/O0.h, I/O1 to I/O1.h	I/O0 to I/O0.h, I/O1 to I/O1.h
	L	L	X	X	H	X	I/O0.h to I/O0, I/O1.h to I/O1	I/O0.h to I/O0, I/O1.h to I/O1
	L	L	X	X	X	L	I/O2 to I/O2.h, I/O3 to I/O3.h	I/O2 to I/O2.h, I/O3 to I/O3.h
	L	L	X	X	X	H	I/O2.h to I/O2, I/O3.h to I/O3	I/O2.h to I/O2, I/O3.h to I/O3

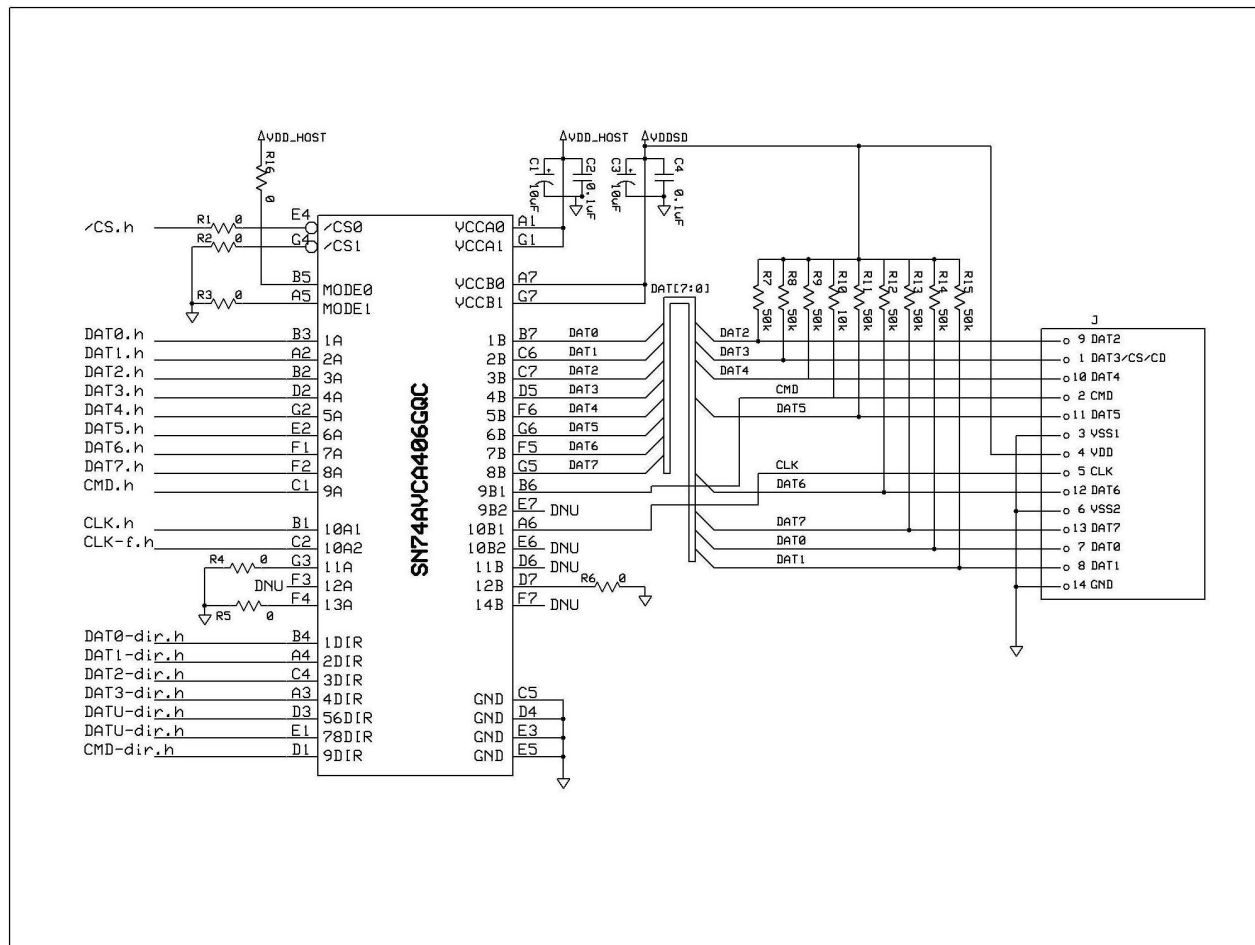
# SN74AVCA406

## MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card

### ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANSCEIVER

SCES615H—OCTOBER 2004—REVISED JANUARY 2007

#### Configuration 3 - Interfacing With 8-Bit MMC



**Table 9. 8-Bit MMC**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	CLK.h	Clock signal from host	Input
C1	9A	CMD.h	Command signal connected to host	I/O
D1	9DIR	CMD-dir.h	Direction control for 9A/9B connected to host	Input
E1	78DIR	DATU-dir.h	Direction control for 7A/7B and 8A/8B. Connected to host.	Input
F1	7A	DAT6.h	General-purpose I/O. Referenced to V <sub>CCA</sub> .	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	DAT1.h	Data bit 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	DAT2.h	Data bit 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	CLK-f.h	Clock feedback to host for resynchronizing data. Used in OMAP processors. Optional on other processors. Leave unconnected if not used.	Output
D2	4A	DAT3.h	Data bit 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	DAT5.h	General-purpose I/O. Referenced to V <sub>CCA</sub> .	I/O
F2	8A	DAT7.h	General-purpose I/O. Referenced to V <sub>CCA</sub> .	I/O
G2	5A	DAT4.h	General-purpose I/O. Referenced to V <sub>CCA</sub> .	I/O
A3	4DIR	DAT3-dir.h	Direction control for 4A/4B	Input
B3	1A	DAT0.h	Data bit 1 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C3	Depopulated ball			
D3	56DIR	DATU-dir.h	Direction control for 5A/5B and 6A/6B. Referenced to V <sub>CCA</sub> .	Input
E3	GND	GND	Ground	
F3	12A	DNU	Output pin not used in this mode. Do not use. Leave unconnected.	Output
G3	11A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
A4	2DIR	DAT1-dir.h	Direction control for 2A/2B connected to host	Input
B4	1DIR	DAT0-dir.h	Direction control for 1A/1B connected to host	Input
C4	3DIR	DAT2-dir.h	Direction control for 3A/3B connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CS0}$ .h	Card select from host. Active low. When $\overline{CS0}$ = high, 1A, 2A, 3A, 4A, 1B, 2B, 3B, 4B, and 9B1 are placed in Hi Z, and 10B1 is low.	Input
F4	13A	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
G4	$\overline{CS1}$	(tie-low)	Card select signal. For proper operation, tie to GND.	Input
A5	MODE1	(tie-low)	MODE1, MODE0 determine mode of operation (see Table 1).	Input
B5	MODE0	(tie-high)	Tie MODE0 to V <sub>CCA</sub> . Tie MODE1 to GND.	Input
C5	GND	GND	Ground	
D5	4B	DAT3	Data bit 4 connected to card. Referenced to V <sub>CCB</sub> .	I/O
E5	GND	GND	Ground	
F5	7B	DAT6	Data bit 6 connected to card. Referenced to V <sub>CCB</sub> .	I/O
G5	8B	DAT7	Data bit 7 connected to card. Referenced to V <sub>CCB</sub> .	I/O
A6	10B1	CLK	Clock signal connected to card	Output
B6	9B1	CMD	Command signal connected to card	Output
C6	2B	DAT1	Data bit 2 connected to card. Referenced to V <sub>CCB0</sub> .	I/O
D6	11B	DNU	Output pin not used in this mode. Leave unconnected.	Output
E6	10B2	DNU	Output pin not used in this mode. Leave unconnected.	Output
F6	5B	DAT4	Data bit 4 connected to card. Referenced to V <sub>CCB</sub> .	I/O
G6	6B	DAT5	Data bit 5 connected to card. Referenced to V <sub>CCB</sub> .	I/O
A7	V <sub>CCB0</sub>	V <sub>CCB0</sub>	B-port supply voltage. V <sub>CCB0</sub> powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	DAT0	Data bit 1 connected to card. Referenced to V <sub>CCB0</sub> .	I/O

Table 9. 8-Bit MMC (continued)

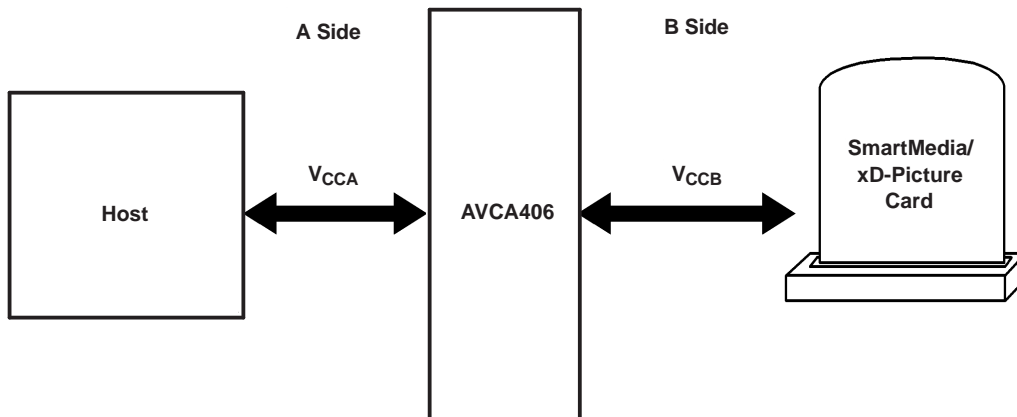
PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
C7	3B	DAT2	Data bit 3 connected to card. Referenced to $V_{CCB0}$ .	I/O
D7	12B	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E7	9B2	DNU	I/O pin not used in this mode. Leave unconnected.	I/O
F7	14B	DNU	Open-drain output not used in this mode. Leave unconnected.	Output
G7	$V_{CCB1}$	$V_{CCB1}$	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B and 14B. Not used in this mode. Tie to GND.	Power

CONFIGURATION 3 FUNCTION TABLE  
(MODE0 = H, MODE1 = L, 8-BIT MMC)

SIGNAL	INPUTS						OPERATION
	$\overline{CS0}$	$\overline{CS1}$	9DIR	(1-4)DIR	56DIR	78DIR	
Clock	L	X	X	X	X	X	CLK.h to CLK, CLK to CLK-f.h
Data	H	X	X	X	X	X	DAT0.h, DAT1.h, DAT2.h, DAT3.h, DAT0, DAT1, DAT2, and DAT3 are Hi Z.
	X	H	X	X	X	X	DAT4.h, DAT5.h, DAT6.h, DAT7.h, DAT4, DAT5, DAT6, and DAT7 are Hi Z.
	L	L	X	L	L	L	DAT0 to DAT0.h, DAT1 to DAT1.h, DAT2 to DAT2.h, DAT3 to DAT3.h, DAT4 to DAT4.h, DAT5 to DAT5.h, DAT6 to DAT6.h, DAT7 to DAT7.h
	L	L	X	H	H	H	DAT0.h to DAT0, DAT1.h to DAT1, DAT2.h to DAT2, DAT3.h to DAT3, DAT4.h to DAT4, DAT5.h to DAT5, DAT6.h to DAT6, DAT7.h to DAT7
Command	H	X	X	X	X	X	CMD.h and CMD are Hi Z (isolation mode).
	L	X	L	X	X	X	CMD to CMD.h
	L	X	H	X	X	X	CMD.h to CMD



**Configuration 4 - Interfacing With SmartMedia or xD-Picture Card**



**Table 10. SmartMedia or xD-Picture Card**

PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
A1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
B1	10A1	$\overline{RE}.h$	Read enable connected to host	Input
C1	9A	CLE.h	Command latch enable connected to host	I/O
D1	9DIR	(tie-low)	Input pin not used in this mode. Tie to GND.	Input
E1	78DIR	I/O-dir.h	Data direction control from host	Input
F1	7A	I/O7.h	Data I/O 7 connected to host. Referenced to V <sub>CCA</sub> .	I/O
G1	V <sub>CCA</sub>	V <sub>CCA</sub>	A-port supply voltage. V <sub>CCA</sub> powers all A-port I/Os and control inputs.	Power
A2	2A	I/O2.h	Data I/O 2 connected to host. Referenced to V <sub>CCA</sub> .	I/O
B2	3A	I/O3.h	Data I/O 3 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C2	10A2	$\overline{RE}.f.h$	Read enable feedback to host. Used with OMAP processors. Use with other processors is optional. Leave unconnected if not used.	Output
D2	4A	I/O4.h	Data I/O 4 connected to host. Referenced to V <sub>CCA</sub> .	I/O
E2	6A	I/O6.h	Data I/O 6 connected to host. Referenced to V <sub>CCA</sub> .	I/O
F2	8A	I/O8.h	Data I/O 8 connected to host. Referenced to V <sub>CCA</sub> .	I/O
G2	5A	I/O5.h	Data I/O 5 connected to host. Referenced to V <sub>CCA</sub> .	I/O
A3	4DIR	I/O-dir.h	Data direction control connected to host	Input
B3	1A	I/O1.h	Data I/O 1 connected to host. Referenced to V <sub>CCA</sub> .	I/O
C3	Depopulated ball			
D3	56DIR	I/O-dir.h	Data direction control connected to host	Input
E3	GND	GND	Ground	
F3	12A	R/B.h	Read/busy connected to host. Open-drain output.	Output
G3	11A	$\overline{WP}.h$	Write protect connected to host	Input
A4	2DIR	I/O-dir.h	Data direction control connected to host	Input
B4	1DIR	I/O-dir.h	Data direction control connected to host	Input
C4	3DIR	I/O-dir.h	Data direction control connected to host	Input
D4	GND	GND	Ground	
E4	$\overline{CS0}$	$\overline{CE}.h$	Chip enable from host	Input
F4	13A	$\overline{WE}.h$	Write enable from host	Input
G4	$\overline{CS1}$	ALE.h	Address latch enable connected to host	Input
A5	MODE1	(tie-high)	MODE1, MODE0 determine mode of operation (see Table 1). Tie to V <sub>CCA</sub> .	Input
B5	MODE0	(tie-high)		Input

Table 10. SmartMedia or xD-Picture Card (continued)

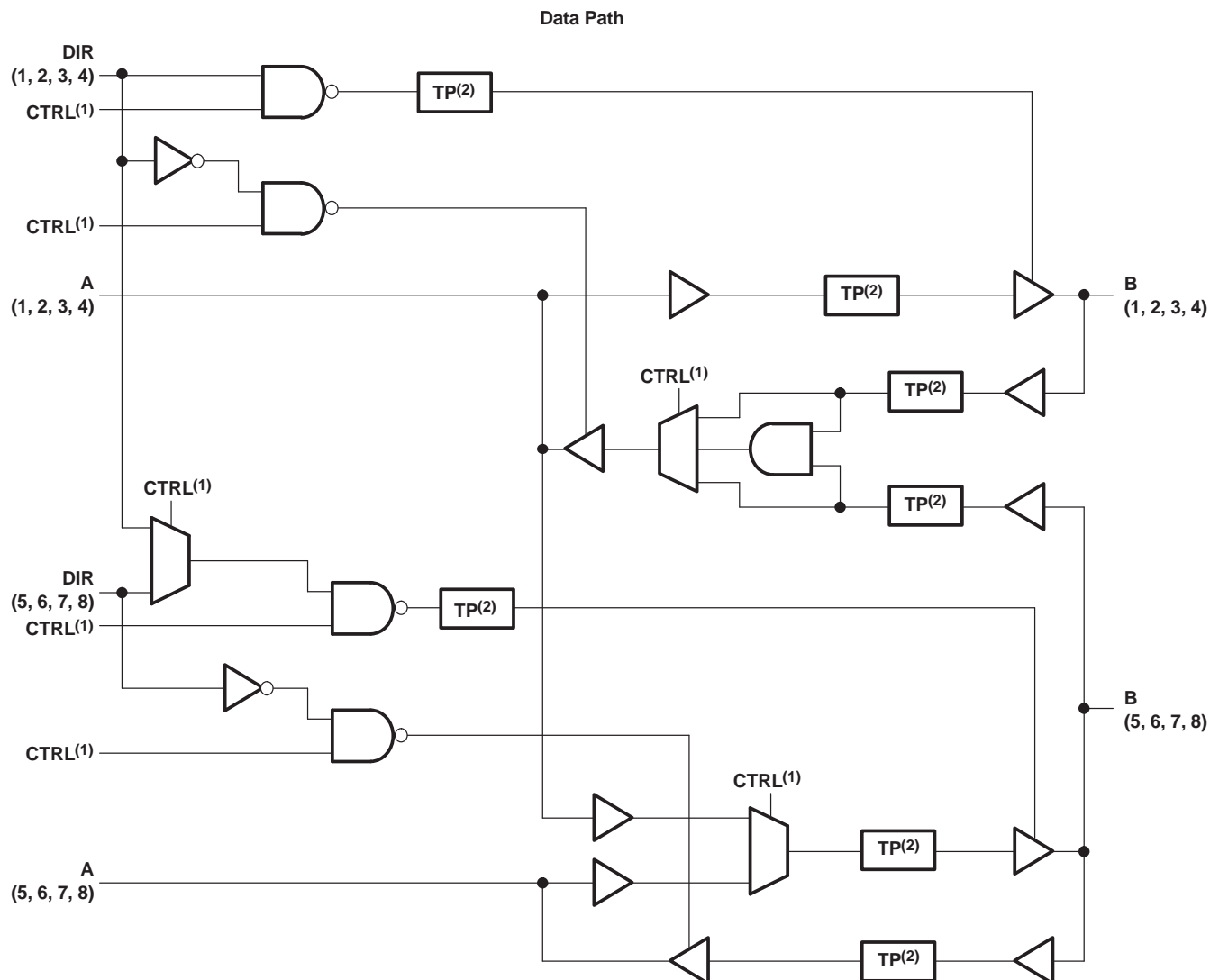
PIN NO.	PIN NAME	SIGNAL NAME OR (CONNECTION)	PIN FUNCTION	PIN TYPE
C5	GND	GND	Ground	
D5	4B	I/O4	Data I/O 4 connected to card. Referenced to $V_{CCB}$ .	I/O
E5	GND	GND	Ground	
F5	7B	I/O7	Data I/O 7 connected to card. Referenced to $V_{CCB}$ .	I/O
G5	8B	I/O8	Data I/O 8 connected to card. Referenced to $V_{CCB}$ .	I/O
A6	10B1	$\overline{RE}$	Read enable connected to card	Output
B6	9B1	CLE	Command latch enable connected to card	Output
C6	2B	I/O2	Data I/O 2 connected to card. Referenced to $V_{CCB}$ .	I/O
D6	11B	$\overline{WP}$	Write protect connected to card	Output
E6	10B2	$\overline{WE}$	Write enable connected to card	Output
F6	5B	I/O5	Data I/O 5 connected to card. Referenced to $V_{CCB}$ .	I/O
G6	6B	I/O6	Data I/O 6 connected to card. Referenced to $V_{CCB}$ .	I/O
A7	$V_{CCB0}$	$V_{CCB}$	B-port supply voltage. $V_{CCB0}$ powers 1B, 2B, 3B, 4B, 9B1, and 10B1.	Power
B7	1B	I/O1	Data I/O 1 connected to card. Referenced to $V_{CCB}$ .	I/O
C7	3B	I/O3	Data I/O 3 connected to card. Referenced to $V_{CCB}$ .	I/O
D7	12B	R/B	Read/busy connected to card	Input
E7	9B2	ALE	Address latch enable connected to host	I/O
F7	14B	$\overline{CE}$	Chip enable connected to card	Output
G7	$V_{CCB1}$	$V_{CCB}$	B-port supply voltage. $V_{CCB1}$ powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.	Power

**CONFIGURATION 4 FUNCTION TABLE**  
**(MODE0 = H, MODE1 = H, 8-BIT SmartMedia/xD-Picture Card)**

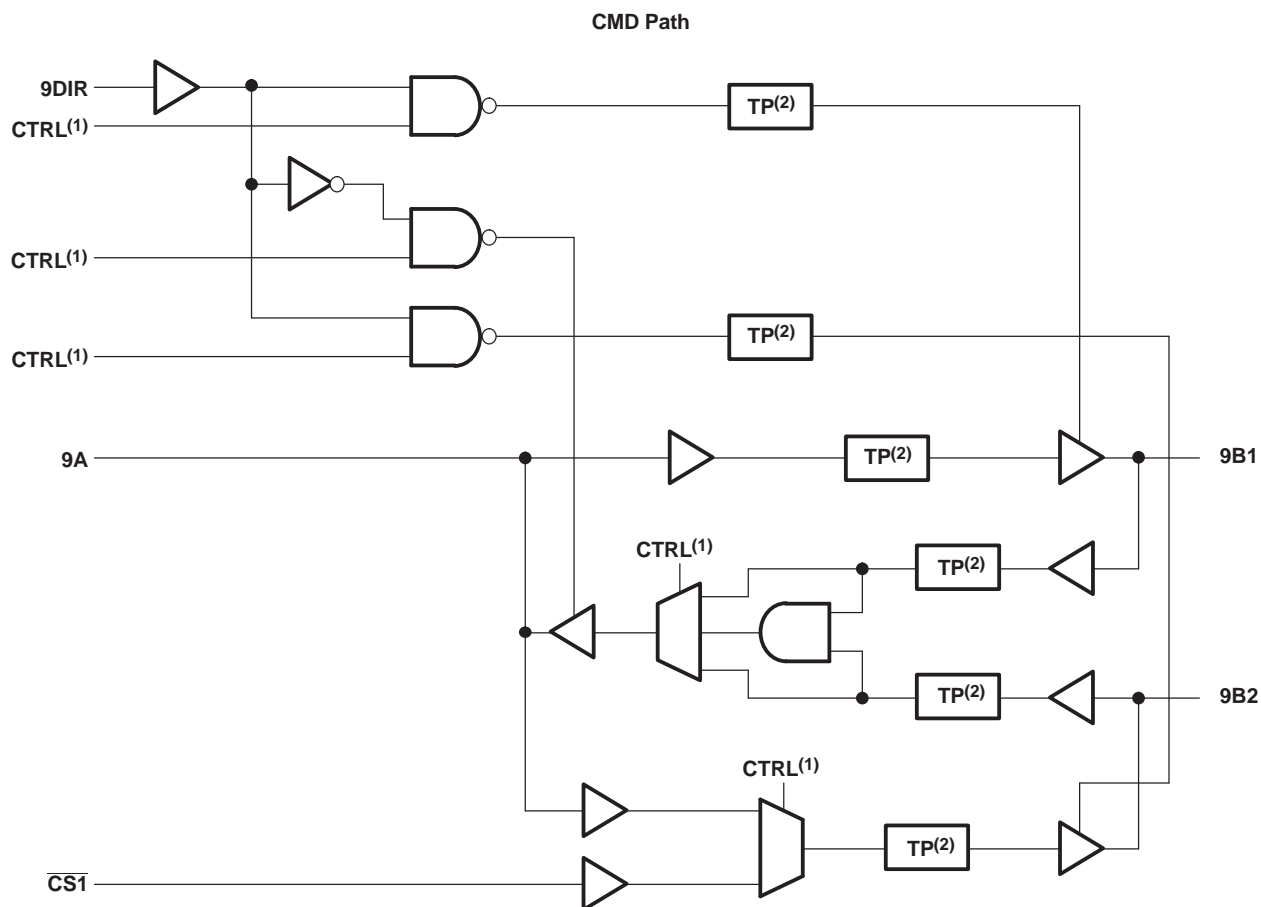
SIGNAL	INPUTS						OPERATION
	$\overline{CS0}$	$\overline{CS1}$	9DIR	(1-4)DIR	56DIR	78DIR	
Clock	X	X	X	X	X	X	$\overline{WE}.h$ to $\overline{WE}$
	L	X	X	X	X	X	$\overline{RE}.h$ to $\overline{RE}$ , $\overline{RE}$ to $\overline{RE}.f.h$
Data	H	X	X	X	X	X	All data I/Os are Hi Z (isolation mode).
	LX	X	X	L	L	L	I/O(1-8) to I/O(1-8).h
	L	X	X	H	H	H	I/O(1-8).h to I/O(1-8)
Command	X	X	X	X	X	X	CLE.h to CLE, ALE.h to ALE
Interrupt request	X	X	X	X	X	X	CE.h to CE
Others	X	X	X	X	X	X	$\overline{WP}.h$ to $\overline{WP}$ , R/B to R/B.h (R/B.h is an open-drain output)



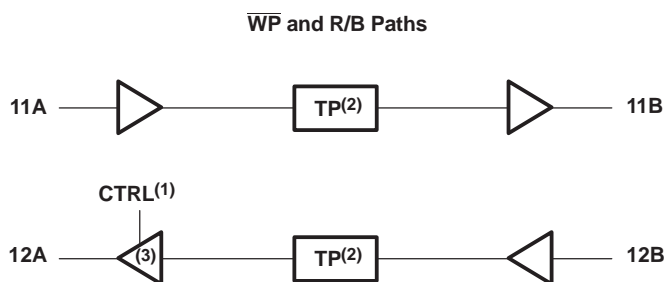
SCES615H–OCTOBER 2004–REVISED JANUARY 2007



(2) Translation point



- (1) CTRL represents a decoded MODE0, MODE1,  $\overline{CS0}$ , and  $\overline{CS1}$  state.  
(2) Translation point

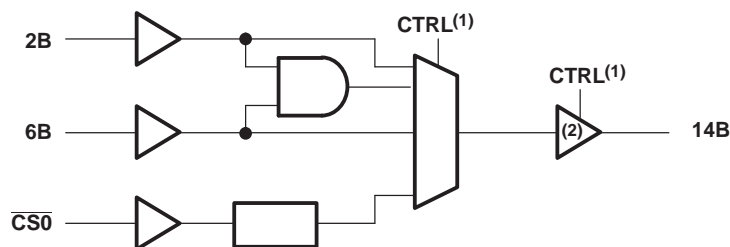


- (1) CTRL represents a decoded MODE0, MODE1,  $\overline{CS0}$ , and  $\overline{CS1}$  state.  
(2) Translation point  
(3) 12A is open drain in NAND (XD) mode and push-pull in other modes.

**SN74AVCA406**  
**MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card**  
**±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANSCEIVER**

SCES615H—OCTOBER 2004—REVISED JANUARY 2007

**$\overline{\text{IRQ}}$  and CEout Paths**



(1) CTRL represents a decoded MODE0, MODE1,  $\overline{\text{CS0}}$ , and  $\overline{\text{CS1}}$  state.

(2) Push-pull in NAND flash (XD) mode and open drain in other modes

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	$V_{CCA}, V_{CCB}$	–0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	I/O ports (A port)	–0.5	$V_{CCA} + 0.5$	V
		I/O ports (B port)	–0.5	$V_{CCB} + 0.5$	
		Control inputs	–0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	–0.5	$V_{CCA} + 0.5$	V
		B port	–0.5	$V_{CCB} + 0.5$	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	A port	–0.5	$V_{CCA} + 0.5$	V
		B port	–0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$		–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	GQC/ZQC package		34	°C/W
$T_{stg}$	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.



**Recommended Operating Conditions**<sup>(1)(2)(3)(4)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.4	V <sub>CCB</sub>	V
V <sub>CCB</sub>	Supply voltage				1.4	3.6	V
V <sub>IH</sub>	High-level input voltage	All inputs <sup>(5)</sup>	1.4 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	All inputs <sup>(5)</sup>	1.4 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	V <sub>CCI</sub>	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	V <sub>CCO</sub>	
I <sub>OH</sub>	High-level output current (A port)			1.4 V to 1.6 V		–1	mA
				1.65 V to 1.95 V		–2	
				2.3 V to 2.7 V		–4	
				3 V to 3.6 V		–8	
I <sub>OL</sub>	Low-level output current (A port)			1.4 V to 1.6 V		1	mA
				1.65 V to 1.95 V		2	
				2.3 V to 2.7 V		4	
				3 V to 3.6 V		8	
I <sub>OH</sub>	High-level output current (B port)			1.4 V to 1.6 V		–2	mA
				1.65 V to 1.95 V		–4	
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–16	
I <sub>OL</sub>	Low-level output current (B port)			1.4 V to 1.6 V		2	mA
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		16	
Δt/Δt	Input transition rise or fall rate					5	ns/V
T <sub>A</sub>	Operating free-air temperature				–40	85	°C

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.(3) V<sub>CCB</sub> must be greater than or equal to V<sub>CCA</sub>, except when V<sub>CCB</sub> = 0 V.(4) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.(5) All A-port I/Os and control inputs are powered by V<sub>CCA</sub>.1B, 2B, 3B, 4B, 9B1, and 10B1 are powered by V<sub>CCB0</sub>.5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B are powered by V<sub>CCB1</sub>.

## Electrical Characteristics<sup>(1)(2)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(3)</sup>	MAX	UNIT
V <sub>OH</sub> (A port)		I <sub>OH</sub> = −100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.4 V to 3.6 V	1.4 V to 3.6 V	V <sub>CCO</sub> − 0.2			V
		I <sub>OH</sub> = −1 mA		1.4 V	1.4 V	1.05			
		I <sub>OH</sub> = −2 mA		1.65 V	1.65 V	1.2			
		I <sub>OH</sub> = −4 mA		2.3 V	2.3 V	1.75			
		I <sub>OH</sub> = −8 mA		3 V	3 V	2.3			
V <sub>OL</sub> (A port)		I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 1 mA		1.4 V	1.4 V			0.35	
		I <sub>OL</sub> = 2 mA		1.65 V	1.65 V			0.45	
		I <sub>OL</sub> = 4 mA		2.3 V	2.3 V			0.55	
		I <sub>OL</sub> = 8 mA		3 V	3 V			0.7	
		I <sub>OL</sub> = 2 mA	Open-drain output (12A)	3 V	3 V			0.45	
V <sub>OH</sub> (B port)		I <sub>OH</sub> = −100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.4 V to 3.6 V	1.4 V to 3.6 V	V <sub>CCO</sub> − 0.2			V
		I <sub>OH</sub> = −2 mA		1.4 V	1.4 V	1.05			
		I <sub>OH</sub> = −4 mA		1.65 V	1.65 V	1.2			
		I <sub>OH</sub> = −8 mA		2.3 V	2.3 V	1.75			
		I <sub>OH</sub> = −16 mA		3 V	3 V	2.3			
V <sub>OL</sub> (B port)		I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 2 mA		1.4 V	1.4 V			0.35	
		I <sub>OL</sub> = 4 mA		1.65 V	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA		2.3 V	2.3 V			0.55	
		I <sub>OL</sub> = 16 mA		3 V	3 V			0.7	
		I <sub>OL</sub> = 2 mA	Open-drain output (14B)	3 V	3 V			0.45	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND		1.4 V to 3.6 V	3.6 V			±2.5	μA
I <sub>off</sub>	14B	V <sub>O</sub> = V <sub>CCA</sub>		0 to 3.6 V	0 V			±10	μA
I <sub>OZ</sub> <sup>(4)</sup>	A or B ports	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	See function table for input states when outputs are Hi Z	3.6 V	3.6 V			±10	μA
	A port			3.6 V	0 V			±10	
I <sub>CCA</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0			1.6 V	1.6 V			4.5	μA
				1.95 V	1.95 V			5	
				1.95 V	0 V			5	
				2.7 V	2.7 V			5.5	
				3.6 V	0 V			10	
				3.6 V	3.6 V			10	
I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0			1.6 V	1.6 V			6.5	μA
				1.95 V	1.95 V			7	
				1.95 V	0 V			0.5	
				2.7 V	2.7 V			7.5	
				3.6 V	0 V			1	
				3.6 V	3.6 V			10	

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.

(3) All typical values are at T<sub>A</sub> = 25°C.

(4) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**Electrical Characteristics (continued)**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(3)</sup>	MAX	UNIT
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.8 V	3 V	3.5			pF
	Clock input				4			
C <sub>o</sub>	14B	V <sub>O</sub> = V <sub>CCB</sub> or GND	1.8 V	3 V	17.5			pF
C <sub>io</sub>	A port	V <sub>O</sub> = V <sub>CCA</sub> or GND	1.8 V	3 V	4.5			pF
	B port	V <sub>O</sub> = V <sub>CCB</sub> or GND			11			

**Output Slew Rates<sup>(1)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	$V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V},$ $V_{CCB} = 3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	
$t_r$	10%	90%	3 <sup>(2)</sup>		ns
$t_f$	90%	10%	3 <sup>(2)</sup>		ns

(1) Values are characterized, but not production tested.

(2) Using  $C_L = 15\text{ pF}$  on the B side and  $C_L = 7\text{ pF}$  on the A side. See derating curves for other load conditions.

## Switching Characteristics

$V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ , over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1	7.7	1	4.9	1	4.7	1	4.4	ns
	B	A	1	6.3	1	5	1	5	1	5	
	CLK.h or SCLK.h	CLK.0 or SCLK.0	1	7.7	1	5	1	4.9	1	4.9	
	CLK.h or SCLK.h	CLK-f.h or SCLK-f.h	2	19	2	12	2	10	2	9.7	
	CMD.h	CMD.0	1	7.1	1	4.1	1	3.9	1	3.6	
	CMD.h	CMD.1	1	7	1	4.6	1	4.1	1	4.2	
	CMD.0	CMD.h	1	6.2	1	4.9	1	4.8	1	4.7	
	$\overline{CS0}$	B	1	6	1	4.2	1	4.2	1	3.9	
	R/B	R/B.h	1	5.7	1	4.8	1	4.7	1	4.8	
	$\overline{WE}$	$\overline{WE}.h$	1	7.4	1	4.3	1	4.3	1	4.2	
	$\overline{WP}$	$\overline{WP}.h$	1	6.6	1	4.5	1	4.4	1	4.3	
$t_{en}$	DAT1.0 or DATA1.0	$\overline{IRQ}$	1	4.8	1	3.3	1	3.3	1	3.3	ns
	DAT1.1 or DATA1.1	$\overline{IRQ}$	1	4.9	1	3.4	1	3.3	1	3.3	
	DIR	B	1	6.7	1	4.5	1	4.4	1	4.6	
	DIR	A	1	10.3	1	9.6	1	9.6	1	9.5	
	R/B	R/B.h (open drain)	1	5.9	1	5.4	1	5.4	1	5.4	
$t_{dis}$	DAT1.0 or DATA1.0	$\overline{IRQ}$	1	6.7	1	4.9	1	5.5	1	5.5	ns
	DAT1.1 or DATA1.1	$\overline{IRQ}$	1	6.5	1	4.7	1	5.4	1	5.4	
	DIR	B	1	6.9	1	6.4	1	6.4	1	6.3	
	DIR	A	1	5.3	1	5.3	1	5.3	1	5.2	
	R/B	R/B.h (open drain)	1	16.9	1	17.4	1	5.3	1	4.1	

## Maximum Frequency and Output Skew

$V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ , over recommended operating free-air temperature range (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 3 V ± 0.3 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
f <sub>max</sub>	Clock	A	B	52		52		MHz
		B	A	52		52		
	Data	A	B	26		26		
		B	A	26		26		
t <sub>sk(o)</sub>		A	B	1.5		1.5		ns

**Switching Characteristics**
 $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ , over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1	7.5	1	4.6	1	4.1	1	3.7	ns
	B	A	1	4.6	1	4.2	1	4.1	1	4	
	CLK.h or SCLK.h	CLK.0 or SCLK.0	1	8	1	4.8	1	4.3	1	4.2	
	CLK.h or SCLK.h	CLK-f.h or SCLK-f.h	2	17.9	2	9.4	2	8.7	2	8.3	
	CMD.h	CMD.0	1	7.4	1	3.7	1	3.3	1	3.3	
	CMD.h	CMD.1	1	6.2	1	4.4	1	3.7	1	3.5	
	CMD.0	CMD.h	1	4.5	1	4	1	3.8	1	3.8	
	$\overline{CS0}$	B	1	6.6	1	4	1	4	1	3.8	
	R/B	R/B.h	1	4.4	1	4	1	3.8	1	3.8	
	$\overline{WE}$	$\overline{WE}.h$	1	7.3	1	3.9	1	3.8	1	3.7	
	$\overline{WP}$	$\overline{WP}.h$	1	5.6	1	4	1	3.6	1	3.8	
$t_{en}$	DAT1.0 or DATA1.0	$\overline{TRQ}$	1	5	1	3.3	1	3.3	1	3.3	ns
	DAT1.1 or DATA1.1	$\overline{TRQ}$	1	4.6	1	3.1	1	3.1	1	3.1	
	DIR	B	1	6.4	1	3.8	1	3.6	1	3.6	
	DIR	A	1	7.7	1	6.9	1	6.9	1	6.9	
	R/B	R/B.h (open drain)	1	4.4	1	4.1	1	4.1	1	4.1	
$t_{dis}$	DAT1.0 or DATA1.0	$\overline{TRQ}$	1	6.5	1	4.8	1	5.5	1	5.5	ns
	DAT1.1 or DATA1.1	$\overline{TRQ}$	1	6.6	1	4.8	1	5.3	1	5.3	
	DIR	B	1	6.3	1	5.4	1	5.7	1	5.7	
	DIR	A	1	5.2	1	5.3	1	5.2	1	5.2	
	R/B	R/B.h (open drain)	1	15.9	1	19.5	1	5.6	1	3.8	

**Maximum Frequency and Output Skew**
 $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ , over recommended operating free-air temperature range (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 3 V ± 0.3 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
f <sub>max</sub>	Clock	A	B	52		52		MHz
		B	A	52		52		
	Data	A	B	26		26		
		B	A	26		26		
t <sub>sk(o)</sub>		A	B	0.8		0.8		ns

## Switching Characteristics

$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ , over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1	4	1	3.4	1	3.1	ns
	B	A	1	3.7	1	3.5	1	3.6	
	CLK.h or SCLK.h	CLK.0 or SCLK.0	1	3.9	1	3.5	1	3.5	
	CLK.h or SCLK.h	CLK-f.h or SCLK-f.h	2	8.3	2	7.3	2	7	
	CMD.h	CMD.0	1	3.2	1	3.1	1	2.7	
	CMD.h	CMD.1	1	3.6	1	3	1	2.8	
	CMD.0	CMD.h	1	3	1	3	1	3	
	$\overline{CS0}$	B	1	4.2	1	3.7	1	3.3	
	R/B	R/B.h	1	3.1	1	3	1	2.9	
	$\overline{WE}$	$\overline{WE}.h$	1	3.6	1	3.4	1	3	
	$\overline{WP}$	$\overline{WP}.h$	1	3.5	1	3.1	1	2.9	
$t_{en}$	DAT1.0 or DATA1.0	$\overline{IRQ}$	1	3.3	1	3.3	1	3.2	ns
	DAT1.1 or DATA1.1	$\overline{IRQ}$	1	3.6	1	3.4	1	3.2	
	DIR	B	1	4.7	1	4.4	1	3.6	
	DIR	A	1	5.3	1	5.3	1	5.1	
	R/B	R/B.h (open drain)	1	3.2	1	3.1	1	3	
$t_{dis}$	DAT1.0 or DATA1.0	$\overline{IRQ}$	1	7.2	1	5.4	1	5.4	ns
	DAT1.1 or DATA1.1	$\overline{IRQ}$	1	7	1	5.4	1	5.4	
	DIR	B	1	4.5	1	5.1	1	5.1	
	DIR	A	1	3.7	1	3.7	1	3.7	
	R/B	R/B.h (open drain)	1	3.2	1	3.9	1	3.9	

## Maximum Frequency and Output Skew

$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ , over recommended operating free-air temperature range (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 3 V ± 0.3 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
f <sub>max</sub>	Clock	A	B	52		52		MHz
		B	A	52		52		
	Data	A	B	26		26		
		B	A	26		26		
t <sub>sk(o)</sub>		A	B	0.7		0.7		ns

**Switching Characteristics**
 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ , over recommended operating free-air temperature range (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	
$t_{pd}$	A	B	1	2.9	ns
	B	A	1	3.8	
	CLK.h or SCLK.h	CLK.0 or SCLK.0	1	3.3	
	CLK.h or SCLK.h	CLK-f.h or SCLK-f.h	2	6.1	
	CMD.h	CMD.0	1	2.7	
	CMD.h	CMD.1	1	2.7	
	CMD.0	CMD.h	1	2.6	
	$\overline{CS0}$	B	1	3.7	
	R/B	R/B.h	1	2.5	
	$\overline{WE}$	$\overline{WE}.h$	1	3	
	$\overline{WP}$	$\overline{WP}.h$	1	2.8	
$t_{en}$	DAT1.0 or DATA1.0	$\overline{IRQ}$	1	3.2	ns
	DAT1.1 or DATA1.1	$\overline{IRQ}$	1	3.2	
	DIR	B	1	3.7	
	DIR	A	1	4.7	
	R/B	R/B.h (open drain)	1	4.9	
$t_{dis}$	DAT1.0 or DATA1.0	$\overline{IRQ}$	1	5.3	ns
	DAT1.1 or DATA1.1	$\overline{IRQ}$	1	5.2	
	DIR	B	1	5	
	DIR	A	1	4.7	
	R/B	R/B.h (open drain)	1	6	

**Maximum Frequency and Output Skew**
 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ , over recommended operating free-air temperature range (see [Figure 1](#))

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	
f <sub>max</sub>	Clock	A	B	52		MHz
		B	A	52		
	Data	A	B	26		
		B	A	26		
t <sub>sk(o)</sub>		A	B	0.7		ns

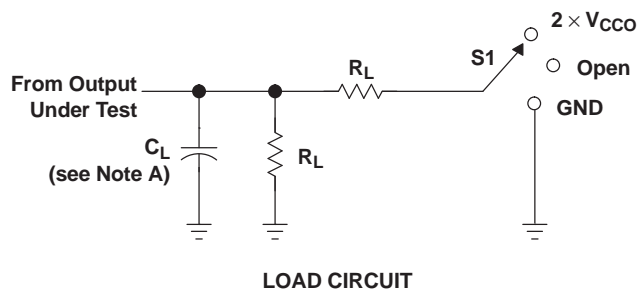


## Operating Characteristics

$V_{CCA} = 1.8\text{ V}$ ,  $V_{CCB} = 3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

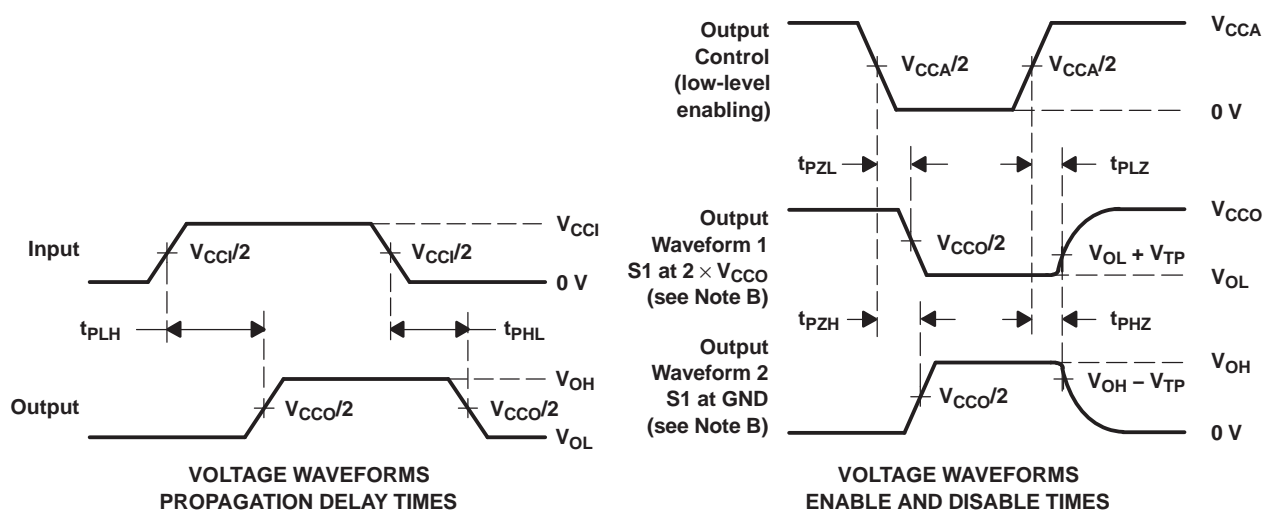
PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{pdA}$	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	9	pF
		Outputs disabled		0.1	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		16	
		Outputs disabled		7.5	
$C_{pdB0}$	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	16.5	pF
		Outputs disabled		0.1	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		4	
		Outputs disabled		2	
$C_{pdB1}$	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	18	pF
		Outputs disabled		0.1	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		6	
		Outputs disabled		3	

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PHL}$	GND
$t_{PLZ}/t_{PZL}$ (OD)	$2 \times V_{CCO}$

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.5 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k $\Omega$	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	15 pF	2 k $\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	15 pF	2 k $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	15 pF	2 k $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1 \text{ V/ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AVCA406DGGR</a>	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCA406
SN74AVCA406DGGR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCA406

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

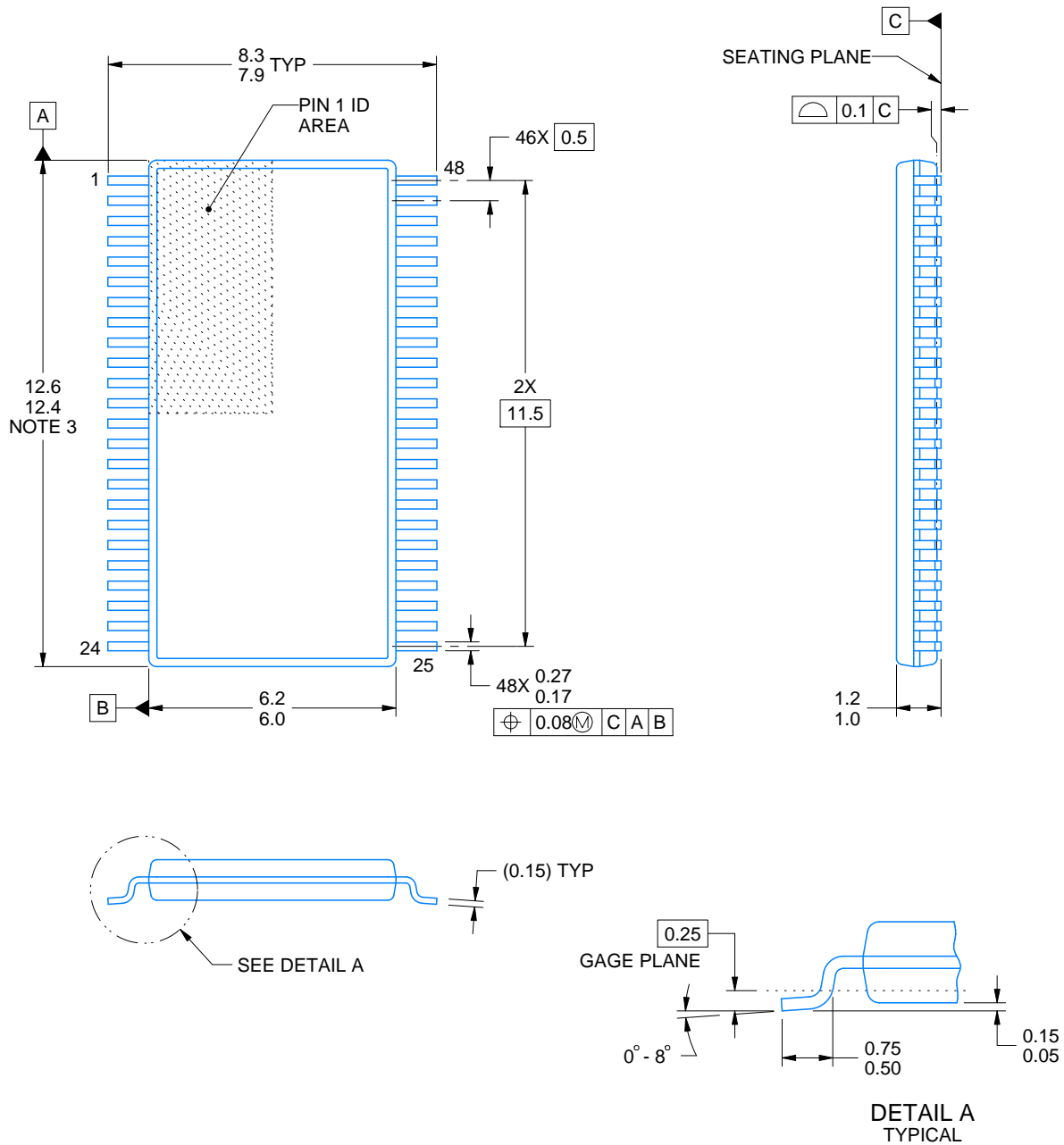
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCA406DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCA406DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0



4214859/B 11/2020

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

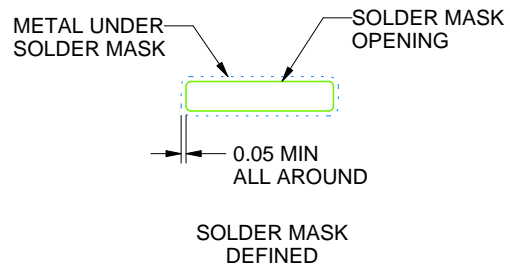
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

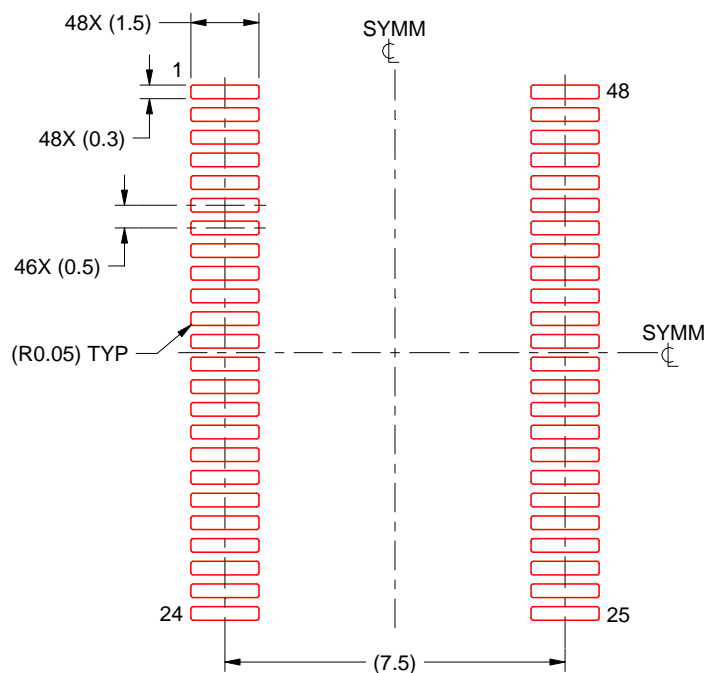
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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