

SN74AVC32T245 32-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation, Level-Shifting, and Tri-State Outputs

1 Features

- Member of the Texas Instruments Widebus+™
- Control Inputs V_{IH}/V_{II} Levels Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature If Either V_{CC} Input is at GND, Both Ports are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.2 V to 3.6 V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- 4.6 V Tolerant I/Os
- Max Data Rates
 - 380 Mbps (1.8 V to 3.3 V Level-Shifting)
 - 200 Mbps (< 1.8 V to 3.3 V Level-Shifting)
 - 200 Mbps (Translate to 2.5 V or 1.8 V)
 - 150 Mbps (Translate to 1.5 V)
 - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 4000 V Human-Body Model (A114-A)
 - 1000 V Charged-Device Model (C101)

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

3 Description

This 32-bit noninverting bus transceiver uses two separate, configurable power-supply rails. SN74AVC32T245 device is optimized to operate with V_{CCA}/V_{CCB} set from 1.4 V to 3.6 V. It is operational with V _{CCA}/V _{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} and accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

The SN74AVC32T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the outputs so the buses are effectively isolated.

The SN74AVC32T245 is designed so that the control pins (1DIR, 2DIR, 3DIR, 4DIR, 1 OE, 2 OE, 3 OE, and $4 \overline{OE}$) are supplied by V_{CCA} .

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)					
SN74AVC32T245ZKE/ GKE	LFBGA (96)	13.50 mm × 5.50 mm					
SN74AVC32T245ZRL	BGA MICROSTAR JUNIOR (96)	8.50 mm × 3.50 mm					
SN74AVC32T245NMJ	nFBGA (96)	13.50 mm × 5.50 mm					

For all available packages, see the orderable addendum at the end of the data sheet.

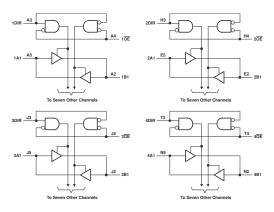


Figure 3-1. Logic Diagram



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	(November 2020) Page and cross-references throughout the document1
` , ,	ize from 8.50 mm × 3.50 mm to 13.50 mm × 5.50 mm in1
Changes from Revision F (July 2015) to Revision G	
· Added NMJ package option to Device Information ta	ble1
	4
	table8
	0
Changes from Revision E (August 2007) to Revision	ı F (July 2015) Page

• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information

Product Folder Links: SN74AVC32T245

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5 Description (continued)

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6 Pin Configuration and Functions

	1	2	3	4	5	6
Α (0	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\circ
В	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
С	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
D	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Е	()	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
F	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
G	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
н	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
J	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
к	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
L	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
М	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
N	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Р	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
R	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
т	\mathcal{C}	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
	\					

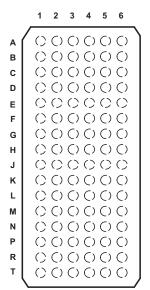


Figure 6-1. GKE, ZKE Package 96-Pin LFBGA Top View

Figure 6-2. ZRL Package 96-Pin BGA MICROSTAR JUNIOR Top View

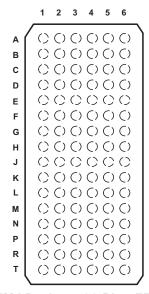


Figure 6-3. NMJ Package 96-Pin nFBGA Top View

Table 6-1. Pin Assignments

	1	2	3	4	5	6
Α	1B2	1B1	1DIR	1 OE	1A1	1A2
В	1B4	1B3	GND	GND	1A3	1A4
С	1B6	1B5	V_{CCB}	V _{CCA}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
Е	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V _{CCB}	V _{CCA}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
Н	2B7	2B8	2DIR	2 OE	2A8	2A7
J	3B2	3B1	3DIR	3 OE	3A1	3A2

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Table 6-1. Pin Assignments (continued)

	1	2	3	4	5	6
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V _{CCB}	V _{CCA}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
Р	4B4	4B3	V _{CCB}	V _{CCA}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
Т	4B7	4B8	4DIR	4 OE	4A8	4A7

Table 6-2. Pin Functions

PIN		1/0	DESCRIPTION			
NO.	NAME	I/O	DESCRIPTION			
A1	1B2	Input/Output	Referenced to V _{CCB}			
A2	1B1	Input/Output	Referenced to V _{CCB}			
A3	1DIR	Input	Direction-control signal			
A4	1 ŌĒ	Input	Tri-State output-mode enables. Pull \overline{OE} high to place all outputs in Tri-State mode. Referenced to V _{CCA}			
A5	1A1	Input/Output	Referenced to V _{CCA}			
A6	1A2	Input/Output	Referenced to V _{CCA}			
B1	1B4	Input/Output	Referenced to V _{CCB}			
B2	1B3	Input/Output	Referenced to V _{CCB}			
B3	GND	_	Ground			
B4	GND	_	Ground			
B5	1A3	Input/Output	Referenced to V _{CCA}			
B6	1A4	Input/Output	Referenced to V _{CCA}			
C1	1B6	Input/Output	Referenced to V _{CCB}			
C2	1B5	Input/Output	Referenced to V _{CCB}			
C3	V _{CCB}	_	B-port supply voltage. 1.2 V ≤ V _{CCB} ≤ 3.6 V			
C4	V _{CCA}	_	A-port supply voltage. 1.2 V ≤ V _{CCA} ≤ 3.6 V			
C5	1A5	Input/Output	Referenced to V _{CCA}			
C6	1A6	Input/Output	Referenced to V _{CCA}			
D1	1B8	Input/Output	Referenced to V _{CCB}			
D2	1B7	Input/Output	Referenced to V _{CCB}			
D3	GND	_	Ground			
D4	GND	_	Ground			
D5	1A7	Input/Output	Referenced to V _{CCA}			
D6	1A8	Input/Output	Referenced to V _{CCA}			
E1	2B2	Input/Output	Referenced to V _{CCB}			
E2	2B1	Input/Output	Referenced to V _{CCB}			
E3	GND	_	Ground			
E4	GND	_	Ground			
E5	2A1	Input/Output	Referenced to V _{CCA}			
E6	2A2	Input/Output	Referenced to V _{CCA}			
F1	2B4	Input/Output	Referenced to V _{CCB}			
F2	2B3	Input/Output	Referenced to V _{CCB}			
F3	V _{CCB}	_	B-port supply voltage. 1.2 V ≤ V _{CCB} ≤ 3.6 V			
F4	V _{CCA}	_	A-port supply voltage. 1.2 V ≤ V _{CCA} ≤ 3.6 V			



Table 6-2. Pin Functions (continued)

PIN			Table 6-2. Pin Functions (continued)			
NO.	NAME	I/O	DESCRIPTION			
F5	2A3	Input/Output	Referenced to V _{CCA}			
F6	2A4	Input/Output	Referenced to V _{CCA}			
G1	2B6	Input/Output	Referenced to V _{CCB}			
G2	2B5	Input/Output	Referenced to V _{CCB}			
G3	GND	_	Ground			
G4	GND	_	Ground			
G5	2A5	Input/Output	Referenced to V _{CCA}			
G6	2A6	Input/Output	Referenced to V _{CCA}			
H1	2B7	Input/Output	Referenced to V _{CCB}			
H2	2B8	Input/Output	Referenced to V _{CCB}			
H3	2DIR	Input	Direction-control signal			
H4	2 OE	Input	Tri-State output-mode enables. Pull \overline{OE} high to place all outputs in Tri-State mode. Referenced to V _{CCA}			
H5	2A8	Input/Output	Referenced to V _{CCA}			
H6	2A7	Input/Output	Referenced to V _{CCA}			
J1	3B2	Input/Output	Referenced to V _{CCB}			
J2	3B1	Input/Output	Referenced to V _{CCB}			
J3	3DIR	Input	Direction-control signal			
J4	3 ŌE	Input	Tri-State output-mode enables. Pull \overline{OE} high to place all outputs in Tri-State mode. Referenced to V _{CCA}			
J5	3A1	Input/Output	Referenced to V _{CCA}			
J6	3A2	Input/Output	Referenced to V _{CCA}			
K1	3B4	Input/Output	Referenced to V _{CCB}			
K2	3B3	Input/Output	Referenced to V _{CCB}			
K3	GND	_	Ground			
K4	GND	_	Ground			
K5	3A3	Input/Output	Referenced to V _{CCA}			
K6	3A4	Input/Output	Referenced to V _{CCA}			
L1	3B6	Input/Output	Referenced to V _{CCB}			
L2	3B5	Input/Output	Referenced to V _{CCB}			
L3	V _{CCB}	_	B-port supply voltage. 1.2 V ≤ V _{CCB} ≤ 3.6 V			
L4	V _{CCA}	_	A-port supply voltage. 1.2 V ≤ V _{CCA} ≤ 3.6 V			
L5	3A5	Input/Output	Referenced to V _{CCA}			
L6	3A6	Input/Output	Referenced to V _{CCA}			
M1	3B8	Input/Output	Referenced to V _{CCB}			
M2	3B7	Input/Output	Referenced to V _{CCB}			
М3	GND	_	Ground			
M4	GND	_	Ground			
M5	3A7	Input/Output	Referenced to V _{CCA}			
M6	3A8	Input/Output	Referenced to V _{CCA}			
N1	4B2	Input/Output	Referenced to V _{CCB}			
N2	4B1	Input/Output	Referenced to V _{CCB}			
N3	GND	_	Ground			
N4	GND	_	Ground			
N5	4A1	Input/Output	Referenced to V _{CCA}			

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Table 6-2. Pin Functions (continued)

	PIN	1/0	DESCRIPTION		
NO.	NAME	- I/O	DESCRIPTION		
N6	4A2	Input/Output	Referenced to V _{CCA}		
P1	4B4	Input/Output	Referenced to V _{CCB}		
P2	4B3	Input/Output	Referenced to V _{CCB}		
P3	V _{CCB}	_	A-port supply voltage. 1.2 V ≤ V _{CCB} ≤ 3.6 V		
P4	V _{CCA}	_	A-port supply voltage. 1.2 V ≤ V _{CCA} ≤ 3.6 V		
P5	4A3	Input/Output	Referenced to V _{CCA}		
P6	4A4	Input/Output	Referenced to V _{CCA}		
R1	4B6	Input/Output	Referenced to V _{CCB}		
R2	4B5	Input/Output	Referenced to V _{CCB}		
R3	GND	_	Ground		
R4	GND	_	Ground		
R5	4A5	Input/Output	Referenced to V _{CCA}		
R6	4A6	Input/Output	Referenced to V _{CCA}		
T1	4B7	Input/Output	Referenced to V _{CCB}		
T2	4B8	Input/Output	Referenced to V _{CCB}		
Т3	4DIR	Input	Direction-control signal		
T4	4 ŌĒ	Input	Tri-State output-mode enables. Pull \overline{OE} high to place all outputs in Tri-State mode. Referenced to V _{CCA}		
T5	4A8	Input/Output	Referenced to V _{CCA}		
T6	4A7	Input/Output	Referenced to V _{CCA}		



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT	
V _{CCA} V _{CCB}	Supply voltage		-0.5	4.6	V	
		I/O ports (A port)	-0.5	4.6		
V_{I}	Input voltage ⁽²⁾		V			
		Control inputs	-0.5	4.6		
V	Valtage applied to any output in the high impedance or never off state(2)	A port	-0.5	0.5 4.6 0.5 4.6	V	
V _O Voltage applied to any output in the high	voltage applied to any output in the high-impedance of power-on state	B port	-0.5	4.6	\ \	
\/	Voltage range applied to any output in the high or low state ^{(2) (3)}	A port	-0.5	0.5 V _{CCA} + 0.5	V	
Vo	voltage range applied to any output in the high of low state	B port	-0.5	V _{CCB} + 0.5	\ \ \	
I _{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current	'		±50	mA	
	Continuous current through each V _{CCA} , V _{CCB} , and GND			±100	mA	
T _{stg}	Storage temperature		-65	150	°C	

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

7.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000	
V _{(ESI}	D) Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

	THERMAL METRIC ⁽¹⁾	GKE/ZKE (LFBGA)	ZRL (MICROSTAR JUNIOR)	NMJ (nFBGA)	UNIT
		96 PINS	96 PINS	96 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.7	105.8	26.7	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	34.0	1.6	14.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	10.8	10.7	°C/W
ΨЈТ	Junction-to-top characterization parameter	3.5	3.1	1.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	43.5	10.8	10.5	°C/W

 For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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7.4 Recommended Operating Conditions

See (1) (2) (3)

			V _{CCI}	V _{cco}	MIN	MAX	UNIT	
V _{CCA}	Supply voltage				1.2	3.6	V	
V _{CCB}	Supply voltage				1.2	3.6	V	
	High-level input voltage		1.2 V to 1.95 V		V _{CCI} × 0.65			
V_{IH}		Data inputs ⁽⁴⁾	1.95 V to 2.7 V		1.6		V	
			2.7 V to 3.6 V		2			
			1.2 V to 1.95 V			V _{CCI} × 0.35		
V_{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.95 V to 2.7 V			0.7	V	
			2.7 V to 3.6 V			3.6 3.6 V _{CCI} × 0.35		
			1.2 V to 1.95 V		V _{CCA} × 0.65			
V_{IH}	High-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.95 V to 2.7 V		1.6		V	
		(Totolonood to VCCA)	2.7 V to 3.6 V		2	3.6 3.6 3.6 3.6 V _{CCI} × 0.35 0.7 0.8 V _{CCA} × 0.35 0.7 0.8 3.6 V _{CCO} 3.6 -3 -6 -8 -9 -12 3 6 8 9 12		
			1.2 V to 1.95 V			V _{CCA} × 0.35		
V_{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.95 V to 2.7 V			0.7	V	
			2.7 V to 3.6 V			0.8		
VI	Input voltage	'			0	3.6	V	
.,		Active state			0	V _{CCO}	V	
Vo	Output voltage	3-state			0	2 3.6 5 3 2 V _{CCI} × 0.35 0.7 0.8 5 3 2 V _{CCA} × 0.35 0.7 0.8 0 V _{CCO} 0 3.6 -3 -6 -8 -9 -12 3 6 8 9 12	V	
		'		1.2 V		-3		
				1.4 V to 1.6 V		-6		
I _{OH}	High-level output current			1.65 V to 1.95 V		3.6 3.6 3.6 3.6 V _{CCI} × 0.35 0.7 0.8 V _{CCA} × 0.35 0.7 0.8 3.6 V _{CCO} 3.6 -3 -6 -8 -9 -12 3 6 8 9 12 5	mA	
				2.3 V to 2.7 V				
				3 V to 3.6 V				
				1.2 V		3		
				1.4 V to 1.6 V		6		
I _{OL}	Low-level output current	Low-level output current		1.65 V to 1.95 V		8	mA	
				2.3 V to 2.7 V		9		
				3 V to 3.6 V		12		
Δt/Δν	Input transition rise or fall ra	ite				5	ns/V	
T _A	Operating free-air temperate	ure			-40	85	°C	

- (1) V_{CCI} is the V_{CC} associated with the data input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.
- (5) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V.



7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(2) (3)

DAD	AMETER	TEST CONDIT	TIONS	V	V	TA	= 25°C		-40°C TO 85	°C	UNIT
PAR	AWEIEK	IEST CONDIT	IONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	MIN	MAX	UNII
		I _{OH} = -100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V				V _{CCO} – 0.2 V		
		I _{OH} = -3 mA		1.2 V	1.2 V		0.95				
.,		I _{OH} = -6 mA],, _,,	1.4 V	1.4 V				1.05		.,
V _{OH}		I _{OH} = -8 mA	$V_{I} = V_{IH}$	1.65 V	1.65 V				1.2		V
		I _{OH} = -9 mA		2.3 V	2.3 V				1.75		
		I _{OH} = -12 mA	1	3 V	3 V				2.3		
		I _{OL} = 100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	
		I _{OL} = 3 mA	1	1.2 V	1.2 V		0.15				
. ,		I _{OL} = 6 mA],, ,,	1.4 V	1.4 V					0.35	.,
V _{OL}		I _{OL} = 8 mA	$V_{I} = V_{IL}$	1.65 V	1.65 V					0.45	V
		I _{OL} = 9 mA	1	2.3 V	2.3 V					0.55	
		I _{OL} = 12 mA		3 V	3 V					0.7	
l ₁	Control inputs	V _I = V _{CCA} or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	:	±0.025	±0.25		±1	μA
	A or B port	$-V_1$ or $V_0 = 0$ to 3.6 V		0 V	0 to 3.6 V		±0.1	±2.5		±5	μA
l _{off}	A or B port	V ₁ OI V ₀ = 0 to 3.6 V		0 to 3.6 V	0 V		±0.1	±2.5		±5	μА
I _{OZ} (1)	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5	μΑ
				1.2 V to 3.6 V	1.2 V to 3.6 V					50	
I _{CCA}		$V_I = V_{CCI}$ or GND,	I _O = 0	0 V	3.6 V					-10	μA
				3.6 V	0 V					50	
				1.2 V to 3.6 V	1.2 V to 3.6 V					50	
I _{CCB}		$V_I = V_{CCI}$ or GND,	I _O = 0	0 V	3.6 V					50	μA
				3.6 V	0 V					-10	
I _{CCA} + I	ССВ	$V_I = V_{CCI}$ or GND,	I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					90	μA
Ci	Control inputs	V _I = 3.3 V or GND		3.3 V	3.3 V		3.5				pF
C _{io}	A or B port	V _O = 3.3 V or GND		3.3 V	3.3 V		7				pF

⁽¹⁾ For I/O ports, the parameter $I_{\mbox{\scriptsize OZ}}$ includes the input leakage current.

⁽²⁾ V_{CCO} is the V_{CC} associated with the output port.

⁽³⁾ V_{CCI} is the V_{CC} associated with the input port.



7.6 Switching Characteristics: $V_{CCA} = 1.2 \text{ V}$

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 8-1)

PARAMETER	FROM	то	V _{CCB} = 1.2 V	V _{CCB} = 1.5 V	V _{CCB} = 1.8 V	V _{CCB} = 2.5 V	V _{CCB} = 3.3 V	UNIT				
PARAMETER	(INPUT)	(OUTPUT)	TYP	TYP	TYP	TYP	TYP	UNII				
t _{PLH}	А	В	4.1	3.3	3	2.8	3.2	no				
t _{PHL}	A	Б	4.1	3.3	3	2.8	3.2	ns				
t _{PLH}	В	Α	4.4	4	3.8	3.6	3.5	ns				
t _{PHL}	Б	A	4.4	4	3.8	3.6	3.5	115				
t _{PZH}	ŌE ŌE	А	6.4	6.4	6.4	6.4	6.4	no				
t _{PZL}		A	6.4	6.4	6.4	6.4	6.4	ns				
t _{PZH}		В	6	4.6	4	3.4	3.2	no				
t _{PZL}	OE	Б	6	4.6	4	3.4	3.2	ns				
t _{PHZ}	OF.	OF.	OF	OF	ŌĒ	А	6.6	6.6	6.6	6.6	6.8	ns
t _{PLZ}	OE	_ ^	6.6	6.6	6.6	6.6	6.8	115				
t _{PHZ}	ŌĒ	ŌĒ B	6	4.9	4.9	4.2	5.3	no				
t _{PLZ}	UE		6	4.9	4.9	4.2	5.3	ns				

7.7 Switching Characteristics: $V_{CCA} = 1.5 V \pm 0.1 V$

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 8-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = ± 0.1		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	А	В	3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
t _{PHL}	^	ь	3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	115
t _{PLH}	В	А	3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t _{PHL}	Б	A	3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	115
t _{PZH}	ŌĒ	Α	4.3	1	10.1	1	10.1	1	10.1	1	10.1	ns
t _{PZL}	OL	^	4.3	1	10.1	1	10.1	1	10.1	1	10.1	115
t _{PZH}	ŌĒ	В	5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
t _{PZL}	OL	ь	5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	115
t _{PHZ}	ŌĒ	Α	4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
t _{PLZ}	OE	^	4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	115
t _{PHZ}	<u>∩</u> E	R	5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	ns
t _{PLZ}	ŌE B —	В	5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	115



7.8 Switching Characteristics: $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 8-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = ± 0.1		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT		
	(INFOI)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
t _{PLH}	А	В	3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns		
t _{PHL}	^		3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	115		
t _{PLH}	В	Α	3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns		
t _{PHL}	Б	A	3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	115		
t _{PZH}	ŌĒ	А	3.4	1	7.8	1	7.8	1	7.8	1	7.8	ns		
t _{PZL}	OE	A	3.4	1	7.8	1	7.8	1	7.8	1	7.8	115		
t _{PZH}	ŌĒ	В	5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	no		
t _{PZL}	OE	Б	5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns		
t _{PHZ}	ŌĒ	Α	4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	no		
t _{PLZ}	OE	^	4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns		
t _{PHZ}	∩E	D	5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7			
t _{PLZ}	ŌĒ	В -	В	Е В —	5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	ns

7.9 Switching Characteristics: $V_{CCA} = 2.5 V \pm 0.2 V$

over recommended operating free-air temperature range, V_{CCA} = 2.5 V \pm 0.2 V (see Figure 8-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = ± 0.1		V _{CCB} = ± 0.1	1.8 V	V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT
	(INPUT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Α	В	3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	ns
t _{PHL}	^	ь	3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	115
t _{PLH}	В	А	2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	ns
t _{PHL}	Ь	A	2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	115
t _{PZH}	ŌĒ	Α	2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
t _{PZL}	OL	A	2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	115
t _{PZH}	ŌĒ	В	5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
t _{PZL}	OL	ь	5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	115
t _{PHZ}	ŌĒ	Α	3	1	6.1	1	6.1	1	6.1	1	6.1	ns
t _{PLZ}	OL	A	3	1	6.1	1	6.1	1	6.1	1	6.1	115
t _{PHZ}	ŌĒ	В	5	1	7.9	1	6.6	1	6.1	1	5.2	ns
t _{PLZ}	<u> </u>	O D	5	1	7.9	1	6.6	1	6.1	1	5.2	115

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7.10 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V \pm 0.3 V (see Figure 8-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = ± 0.1		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT
	(INFOT)	(001101)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Α	В	3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
t _{PHL}	^	Ь	3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	115
t _{PLH}	В	Α	2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	ns
t _{PHL}	Ь	A	2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	115
t _{PZH}	ŌĒ	Α	2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	ns
t _{PZL}	OL	A	2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	115
t _{PZH}	ŌĒ	В	5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	ns
t _{PZL}	OE	Б	5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	115
t _{PHZ}	ŌĒ	Α	3.4	0.5	5	0.5	5	0.5	5	0.5	5	ns
t _{PLZ}	OL	A	3.4	0.5	5	0.5	5	0.5	5	0.5	5	115
t _{PHZ}	ŌĒ	В	4.9	1	7.7	1	6.5	1	5.2	0.5	5	ns
t _{PLZ}	OL .	D	4.9	1	7.7	1	6.5	1	5.2	0.5	5	115

7.11 Operating Characteristics

 $T_A = 25^{\circ}C$

1 _A = 25	PARAME	TER	TEST CONDITIONS	V _{CCA} = V _{CCB} = 1.2 V	V _{CCA} = V _{CCB} = 1.5 V	V _{CCA} = V _{CCB} = 1.8 V	V _{CCA} = V _{CCB} = 2.5 V	V _{CCA} = V _{CCB} = 3.3 V	UNIT	
			CONDITIONS	TYP	TYP	TYP	TYP	TYP		
	A to B	Outputs enabled		1	1	1	1	2		
C _{pdA} ⁽¹⁾	Alob	Outputs disabled	$C_L = 0,$ f = 10 MHz,	1	1	1	1	1	pF	
OpdA	B to A	Outputs enabled	$t_r = t_f = 1 \text{ ns}$	13	13	14	15	16	P'	
	BIOA	Outputs disabled		1	1	1	1	1		
	A to B	Outputs enabled		13	13	14	15	16		
C _{pdB} ⁽¹⁾	7 10 5	Outputs disabled	$C_L = 0,$	1	1	1	1	1	pF	
OpdB (*)	B to A	Outputs enabled	enabled	1	1	1	1	1	2	ρı
	D to A	Outputs disabled		1	1	1	1	1		

Power dissipation capacitance per transceiver. Refer to the TI application report, CMOS Power Consumption and C_{pd} Calculation SCAA035.



Table 7-1. Typical Total Static Power Consumption (I _{CCA} +	Iccs))
---	-------	---

		, .				,	
V			UNIT				
V _{CCB}	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	ONII
0 V	0	<1	<1	<1	<1	<1	
1.2 V	<1	<2	<2	<2	<2	2	
1.5 V	<1	<2	<2	<2	<2	2	
1.8 V	<1	<2	<2	<2	<2	<2	μA
2.5 V	<1	2	<2	<2	<2	<2	
3.3 V	<1	2	<2	<2	<2	<2	

7.12 Typical Characteristics

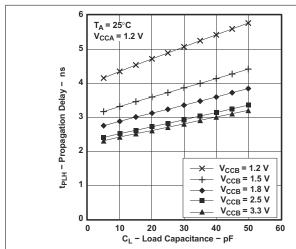


Figure 7-1. Propagation Delay vs Load Capacitance

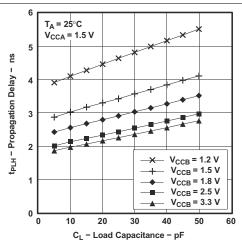


Figure 7-3. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

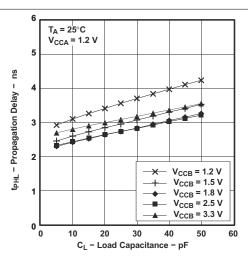


Figure 7-2. Propagation Delay vs Load Capacitance

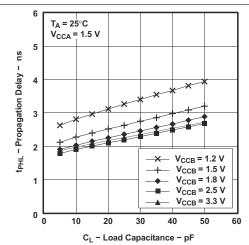


Figure 7-4. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

7.12 Typical Characteristics (continued)

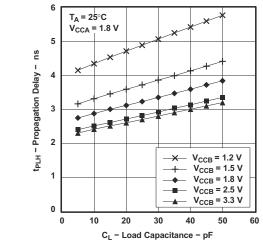


Figure 7-5. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

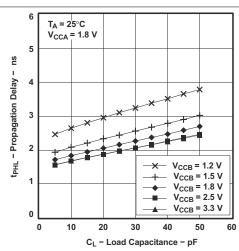


Figure 7-6. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

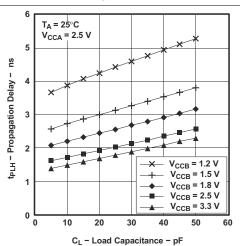


Figure 7-7. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

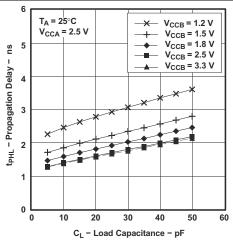


Figure 7-8. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

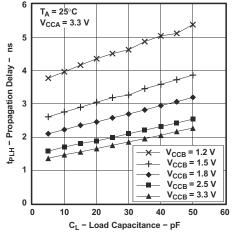


Figure 7-9. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

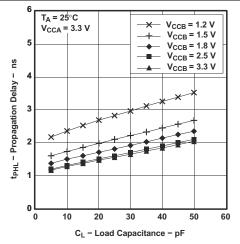
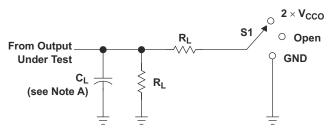


Figure 7-10. Propagation Delay vs Load Capacitance



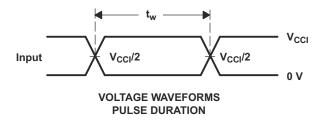
8 Parameter Measurement Information

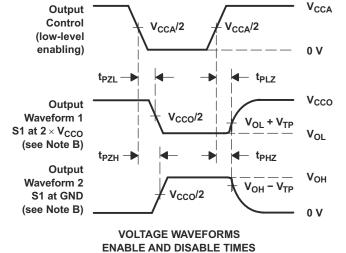


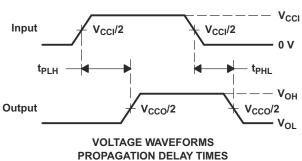
TEST	S 1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 × V _{CCO} GND

LOAD CIRCUIT

V _{CCO}	CL	R _L	V _{TP}
1.2 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V







NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , dv/dt \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. $\,t_{PZL}$ and t_{PZH} are the same as $t_{en}.$
- $\begin{array}{ll} \text{G.} & t_{PLH} \text{ and } t_{PHL} \text{ are the same as } t_{pd}. \\ \text{H.} & V_{CCI} \text{ is the } V_{CC} \text{ associated with the input port.} \end{array}$
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 8-1. Load Circuit and Voltage Waveforms

9 Detailed Description

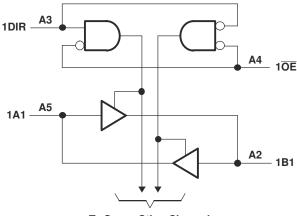
9.1 Overview

The SN74AVC32T245 is a 32-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and $\overline{\text{OE}}$) are supported by V_{CCA} and pins B are supported by V_{CCB}. The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{\text{OE}}$ is set to low. When $\overline{\text{OE}}$ is set to high, both A and B are in the high-impedance state.

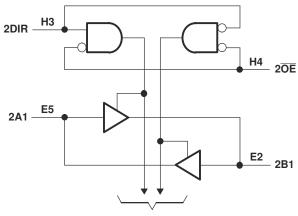
This device is fully specified for partial-power-down applications using off output current (I_{off}).

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state

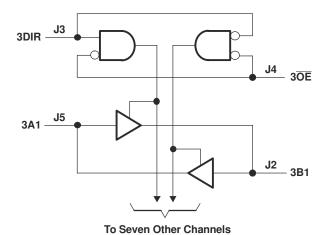
9.2 Functional Block Diagram



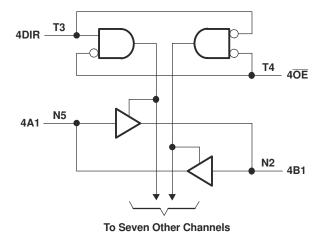
To Seven Other Channels



To Seven Other Channels



Logic diagram (positive logic)



9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2 V to 3.6 V which makes the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

9.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

9.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ}). This prevents false logic levels from being presented to either bus.

9.4 Device Functional Modes

The SN74AVC32T245 is a voltage level translator that can operate from 1.2 V to 3.6 V (V_{CCA}) and 1.2 V to 3.6 V (V_{CCB}). The signal translation between 1.2 V and 3.6 V requires direction control and output enable control. When \overline{OE} is low and DIR is high, data transmission is from A to B. When \overline{OE} is low and DIR is low, data transmission is from B to A. When \overline{OE} is high, both output ports will be high-impedance.

Table 9-1. Function Table (Each 8-Bit Section)

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

Product Folder Links: SN74AVC32T245

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVC32T245 device can be used in level-shifting applications for interfacing devices and addressing mixed voltage incompatibility. The SN74AVC32T245 device is ideal for data transmission where direction is different for each channel.

10.2 EnableTimes

Calculate the enable times for the SN74AVC32T245 using the following formulas:

$$t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)$$
(1)

$$t_{PZL}$$
 (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A) (2)

$$t_{PZH}$$
 (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B) (3)

$$t_{PZL}$$
 (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B) (4)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC32T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.



10.3 Typical Application

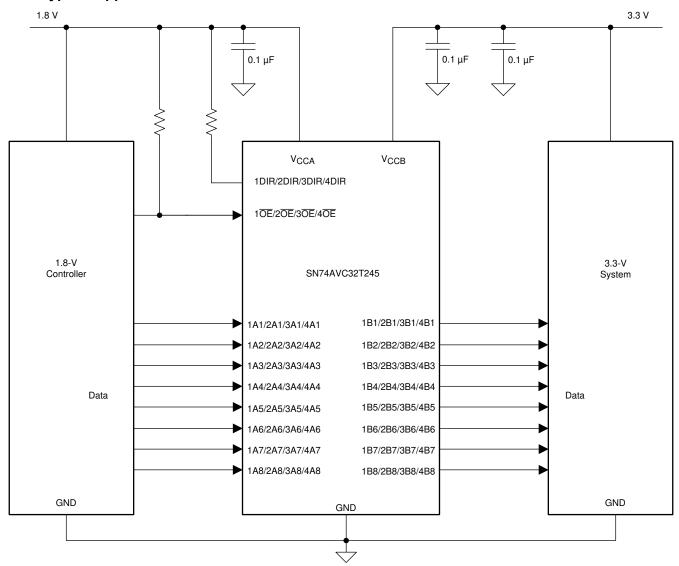


Figure 10-1. Application Schematic

10.3.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in the *Electrical Characteristics*.

Table 10-1. Design Parameters

rabio io ii booigii i aramotoro						
DESIGN PARAMETER	EXAMPLE VALUE					
Input voltage range	1.2 V to 3.6 V					
Output voltage range	1.2 V to 3.6 V					

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10.3.2 Detailed Design Procedure

See Section 10.3.2.1 and Section 10.3.2.2 for information about how to begin the design process.

10.3.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVC32T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

10.3.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVC32T245 device is driving to determine the output voltage range.

10.3.3 Application Curve

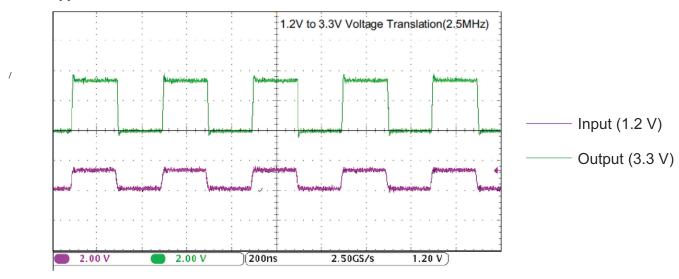


Figure 10-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVC32T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB} . VCCA accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} , respectively, allowing for low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V voltage nodes.

The output-enable \overline{OE} input circuit is designed so that it is supplied by V_{CCA} and when the \overline{OE} input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the \overline{OE} input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

12.2 Layout Example

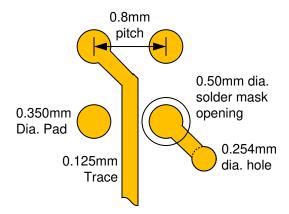


Figure 12-1. BGA Layout Example

Submit Document Feedback

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

http://www.ti.com/lit/an/scea014/scea014.pdf

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 9-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74AVC32T245NMJR	Active	Production	NFBGA (NMJ) 96	1000 LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	29UW
SN74AVC32T245NMJR.B	Active	Production	NFBGA (NMJ) 96	1000 LARGE T&R	-	Call TI	Call TI	-40 to 85	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 1-Apr-2023

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC32T245NMJR	NFBGA	NMJ	96	1000	330.0	24.4	5.85	13.85	1.8	8.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

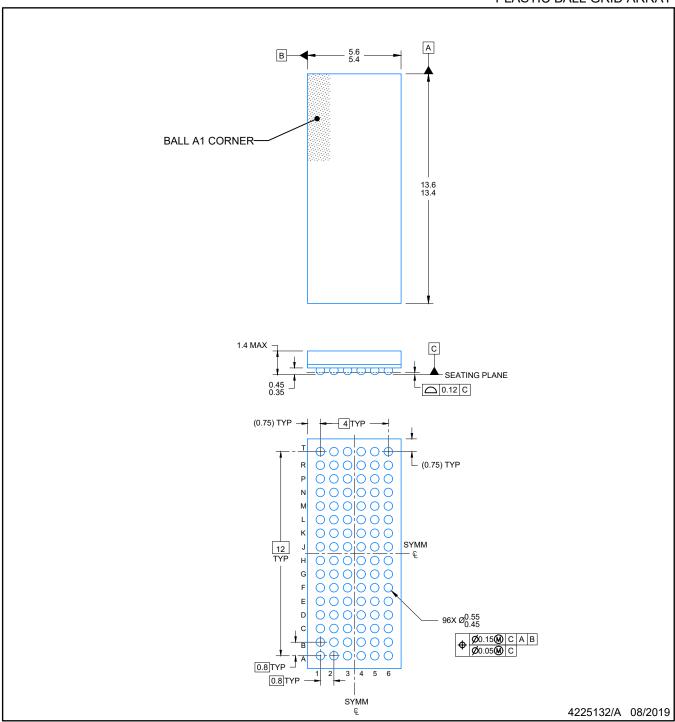
www.ti.com 1-Apr-2023



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC32T245NMJR	NFBGA	NMJ	96	1000	336.6	336.6	41.3

PLASTIC BALL GRID ARRAY



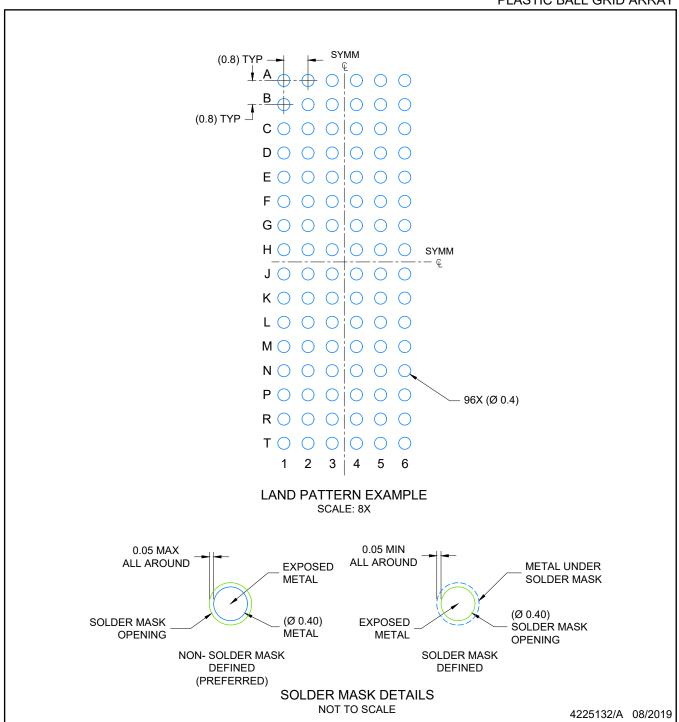
NOTES:

NanoFree is a trademark of Texas Instruments.

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.



PLASTIC BALL GRID ARRAY

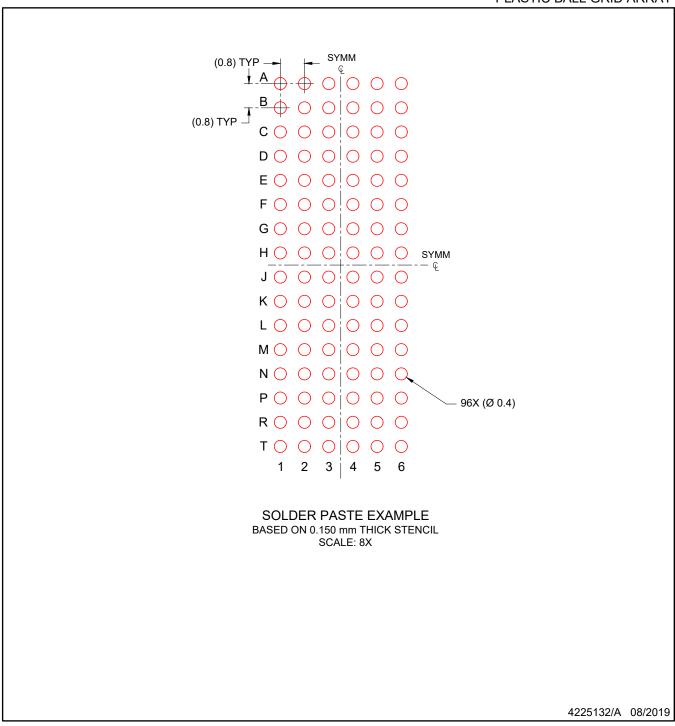


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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