

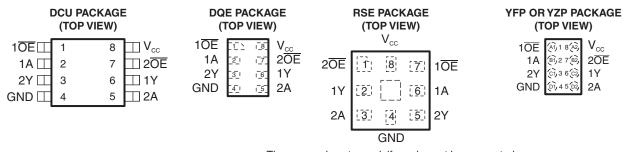
LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Check for Samples: SN74AUP2G125

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption (I_{CC} = 0.9 μA Max)
- Low Dynamic-Power Consumption (C_{pd} = 4 pF Typ at 3.3 V)
- Low Input Capacitance (C_I = 1.5 pF Typ)
- Low Noise Overshoot and Undershoot <10% of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input

- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.4 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



The exposed center pad, if used, must be connected only as a secondary GND or left electrically open.

See mechanical drawings for dimensions.

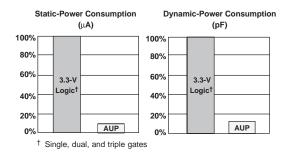
DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





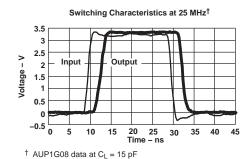


Figure 1. AUP - The Lowest-Power Family

Figure 2. Excellent Signal Integrity

The SN74AUP2G125 is a dual bus buffer gate designed for 0.8-V to 3.6-V V_{CC} operation. This device features dual line drivers with 3-state outputs. Each output is disabled when the corresponding output-enable (OE) input is high. This device has the input-disable feature, which allows floating input signals.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G125YFPR	HM_
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP2G125YZPR	HM_
40 0 10 00 0	uQFN – DQE	Reel of 5000	SN74AUP2G125DQER	PV
	QFN - RSE	Reel of 5000	SN74AUP2G125RSER	PV
	VSSOP - DCU	Reel of 3000	SN74AUP2G125DCUR	H25_

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLE

INP	INPUTS				
ŌĒ	Α	Υ			
L	Н	Н			
L	L	L			
Н	X ⁽¹⁾	Z			

(1) Floating inputs allowed.

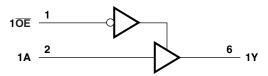
⁽²⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

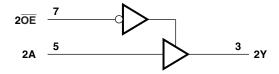
⁽³⁾ YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free). DCU: The actual top-side marking has one additional character to designate the wafer fab/assembly site.



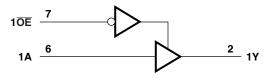
LOGIC DIAGRAM (POSITIVE LOGIC)

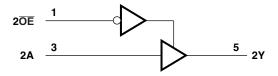
DCU, YFP, and YZP Packages





RSE Package





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_{I}	Input voltage range (2)			4.6	V
Vo	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾			4.6	V
Vo	Output voltage range in the high or low state ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		– 50	mA
Io	Continuous output current		±20	mA	
	Continuous current through V _{CC} or GND			±50	mA
		DCU package		227	
		DQE package		261	
θ_{JA}	Package thermal impedance (3)	RSE package		253	°C/W
		YFP package		132	
		YZP package		102	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.



RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		0.8	3.6	V	
		V _{CC} = 0.8 V	V _{CC}	3.6		
. ,	High level input values	V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	3.6	\ /	
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	3.6	V	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2	3.6		
		V _{CC} = 0.8 V		0		
.,	Lavo laval importo dila ma	V _{CC} = 1.1 V to 1.95 V	0	0.35 × V _{CC}	V	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7	V	
		V _{CC} = 3 V to 3.6 V	0	0.9		
\/	Output valtage	Active state	0	V _{CC}	V	
V _O	Output voltage	3-state	0	3.6	V	
		V _{CC} = 0.8 V		-20	μА	
		V _{CC} = 1.1 V		-1.1		
	High level entent engage	V _{CC} = 1.4 V		-1.7		
l _{OH}	High-level output current	V _{CC} = 1.65 V		-1.9	mA	
		V _{CC} = 2.3 V		-3.1		
		V _{CC} = 3 V		-4		
		$V_{CC} = 0.8 \text{ V}$		20	μΑ	
		V _{CC} = 1.1 V		1.1		
	Lour loval output ourrent	V _{CC} = 1.4 V		1.7		
l _{OL}	Low-level output current	V _{CC} = 1.65 V		1.9 3.1		
		V _{CC} = 2.3 V				
		V _{CC} = 3 V		4		
Δt/Δν	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report Implications of Slow of Floating CMOS Inputs, literature number SCBA004.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

DAE	AMETER	TEST COMPITIONS	V	T,	_A = 25°C	$T_A = -40^{\circ}C t$	o 85°C	LINUT	
PAR	RAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP MAX	MIN	MAX	UNIT	
		I _{OH} = -20 μA	0.8 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1			
		I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}			
W		$I_{OH} = -1.7 \text{ mA}$	1.4 V	1.11		1.03		V	
		I _{OH} = −1.9 mA	1.65 V	1.32		1.3			
V _{OH}		I _{OH} = -2.3 mA	221/	2.05		1.97		V	
		$I_{OH} = -3.1 \text{ mA}$	2.3 V	1.9		1.85			
		$I_{OH} = -2.7 \text{ mA}$	0.1/	2.72		2.67			
		$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55			
		I _{OL} = 20 μA	0.8 V to 3.6 V		0.1		0.1		
		I _{OL} = 1.1 mA	1.1 V		0.3 × V _{CC}	().3 × V _{CC}		
		I _{OL} = 1.7 mA	1.4 V		0.31		0.37		
		I _{OL} = 1.9 mA	1.65 V		0.31		0.35	.,	
V_{OL}		I _{OL} = 2.3 mA	0.01/		0.31		0.33	V	
		I _{OL} = 3.1 mA	2.3 V		0.44		0.45		
		I _{OL} = 2.7 mA	0.1/		0.31		0.33		
		I _{OL} = 4 mA	3 V		0.44		0.45		
I _I	A or OE input	V _I = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	μА	
I _{off}		V_I or $V_O = 0$ V to 3.6 V	0 V		0.2		0.6	μΑ	
Δl _{off}		V_I or $V_O = 0$ V to 3.6 V	0 V to 0.2 V		0.2		0.9	μА	
loz		$V_O = V_{CC}$ or GND	3.6 V		0.1		0.5	μΑ	
I _{CC}		$\frac{V_I}{OE}$ = GND or (V _{CC} to 3.6 V), $\frac{V_I}{OE}$ = GND, I _O = 0	0.8 V to 3.6 V		0.5		0.9	μА	
	A input	$V_{I} = V_{CC} - 0.6 V^{(1)},$	221/		40		50		
ΔI _{CC}	OE input	I _O = 0	3.3 V		110		120	μΑ	
 100	All inputs	$\frac{V_I}{OE} = GND \text{ to } 3.6 \text{ V},$ $\frac{V_I}{OE} = \frac{V_{CC}}{V_{CC}}$	0.8 V to 3.6 V		0		0	μ, .	
0	•	W W as OND	0 V		2			pF	
CI		$V_I = V_{CC}$ or GND	3.6 V		2				
C _o		$V_O = V_{CC}$ or GND	3.6 V		3			pF	

 $[\]begin{array}{ll} \hbox{(1)} & \hbox{One input at $V_{CC}-0.6$ V, other input at V_{CC} or GND} \\ \hbox{(2)} & \hbox{To show I_{CC} is very low when the input-disable feature is enabled} \end{array}$



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5 pF$ (unless otherwise noted) (see Figure 3 and Figure 4)

DADAMETER	FROM	то	V	T,	4 = 25°C	;	$T_A = -40$ °C 1	o 85°C	LINUS
PARAMETER	(INPUT)	(OUTPUT)	V _{cc}	MIN	TYP	MAX	MIN	MAX	UNI
			0.8 V		23.0				
			1.2 V ± 0.1 V	0.5	7.8	19.5	0.5	20.7	
	^	Υ	1.5 V ± 0.1 V	0.5	5.2	11.1	0.5	13.5	
t_{pd}	A	Y	1.8 V ± 0.15 V	0.6	4.0	8.1	0.5	10.5	ns
			$2.5 \text{ V} \pm 0.2 \text{ V}$	0.9	2.8	5.0	0.5	7.1	
			3.3 V ± 0.3 V	0.9	2.3	3.7	0.5	5.4	
			0.8 V		32.5				
			1.2 V ± 0.1 V	0.5	8.5	21.7	0.5	23.1	ns
	ŌĒ	Υ	1.5 V ± 0.1 V	0.7	5.5	11.6	0.5	14.2	
t _{en}	OE .	ĭ	1.8 V ± 0.15 V	1.0	4.3	8.6	0.5	11.1	
			2.5 V ± 0.2 V	1.3	3.0	5.4	0.5	7.6	
			3.3 V ± 0.3 V	1.3	2.4	4.0	0.5	5.8	
			0.8 V		13.0				
			1.2 V ± 0.1 V	1.8	5.0	9.8	1.5	10.2	
	0 -	V	1.5 V ± 0.1 V	0.5	3.6	7.3	0.5	7.6	ns
t _{dis}	ŌĒ	Y	1.8 V ± 0.15 V	0.5	3.3	5.9	0.5	6.3	
		2.5 V ± 0.2 V	0.5	2.2	3.7	0.5	4.1	1	
			3.3 V ± 0.3 V	1.5	2.6	4.3	1.1	4.6	1

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C₁ = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

DADAMETED	FROM	то	V	T,	4 = 25°C	;	$T_A = -40$ °C 1	o 85°C	UNI
PARAMETER	(INPUT)	(OUTPUT)	V _{cc}	MIN	TYP	MAX	MIN	MAX	UNII
			0.8 V		26.0				
			1.2 V ± 0.1 V	0.5	8.8	21.5	0.5	22.7	
	^	Υ	1.5 V ± 0.1 V	1.2	6.0	12.4	0.5	14.7	
t _{pd}	Α	Ť	1.8 V ± 0.15 V	1.2	4.7	9.2	0.5	11.5	ns
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.4	3.3	5.8	0.5	7.8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.4	2.7	4.3	0.5	6.0	
		Y	0.8 V		35.7				
			1.2 V ± 0.1 V	0.5	9.6	23.8	0.5	25.1	ns
	ŌĒ		1.5 V ± 0.1 V	1.5	6.4	12.9	0.5	15.5	
t _{en}	OE	Ť	1.8 V ± 0.15 V	1.5	5.0	9.8	0.5	12.2	ns
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.6	3.5	9.6	0.5	12.3	
			3.3 V ± 0.3 V	1.6	2.9	4.7	0.5	6.4	
			0.8 V		14.5				
			1.2 V ± 0.1 V	0.9	5.8	11.2	0.8	11.5	
	ŌĒ	Υ	1.5 V ± 0.1 V	0.5	4.1	9.0	0.5	9.2	
t _{dis}	OE	Y	1.8 V ± 0.15 V	1.3	4.4	7.5	1.1	7.8	ns
			2.5 V ± 0.2 V	1.2	2.9	4.7	1.0	5.0	
			3.3 V ± 0.3 V	1.9	3.8	6.1	1.7	6.3	

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T,	λ = 25°C	;	$T_A = -40^{\circ}C$	to 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNIT
			0.8 V		28.6				
			1.2 V ± 0.1 V	0.5	9.8	23.5	0.5	24.6	
	t _{pd} A	Υ	1.5 V ± 0.1 V	1.7	4.1	13.5	0.5	15.7	
^L pd		Ť	1.8 V ± 0.15 V	1.6	5.3	10.2	0.5	12.4	ns
			2.5 V ± 0.2 V	1.8	3.8	6.4	0.5	8.4	
			3.3 V ± 0.3 V	1.7	3.1	4.8	0.5	6.4	
	t _{en} <u>Ō</u> E	Y	0.8 V		38.9				ns
			1.2 V ± 0.1 V	0.5	10.7	24.7	0.5	26.0	
			1.5 V ± 0.1 V	1.7	7.2	14.1	0.5	16.5	
t _{en}	OE .		1.8 V ± 0.15 V	2.0	5.6	10.3	0.5	12.7	
			2.5 V ± 0.2 V	2.0	4.0	6.8	0.5	8.9	
			3.3 V ± 0.3 V	1.9	3.3	5.2	0.5	6.8	
			0.8 V		14.8				
			1.2 V ± 0.1 V	0.5	6.3	13.7	0.5	14.0	
4	ŌĒ	V	1.5 V ± 0.1 V	0.5	4.6	8.8	0.5	9.1	
t _{dis}	OE	Y	1.8 V ± 0.15 V	0.7	4.9	8.1	0.6	8.4	
			2.5 V ± 0.2 V	1.1	3.7	6.5	1.0	6.7	
		3.3 V ± 0.3 V	1.3	4.8	7.6	1.2	7.7		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	Т,	4 = 25°C	;	$T_A = -40^{\circ}C$ t	o 85°C	UNI
PARAMETER	(INPUT)	(OUTPUT)	V _{cc}	MIN	TYP	MAX	MIN	MAX	UNI
			0.8 V		37.9				
			1.2 V ± 0.1 V	0.5	13.0	30.2	0.5	31.1	
	^	Y	1.5 V ± 0.1 V	3.2	8.9	17.2	0.9	19.2	Ī
t _{pd}	A	Y	1.8 V ± 0.15 V	3.0	7.1	13.0	0.8	15.0	ns
			2.5 V ± 0.2 V	3.0	5.2	8.3	1.2	10.2	
			3.3 V ± 0.3 V	2.7	4.3	6.5	1.3	7.9	
		ŌĒ Y	0.8 V		49.9				
			1.2 V ± 0.1 V	0.5	14.1	31.7	0.5	32.8	-
	ŌĒ		1.5 V ± 0.1 V	2.7	9.6	17.8	0.6	20.0	
t _{en}	OE	Y	1.8 V ± 0.15 V	2.5	7.5	13.2	0.5	15.4	n
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.9	5.5	8.6	1.2	10.6	
			3.3 V ± 0.3 V	2.7	4.6	6.7	1.4	8.3	
			0.8 V		17.9				
			1.2 V ± 0.1 V	0.5	8.7	17.4	0.5	17.6	
4	ŌĒ	Y	1.5 V ± 0.1 V	0.5	6.5	14.0	0.5	14.0	
$t_{\sf dis}$	OE	r	1.8 V ± 0.15 V	2.4	8.1	12.9	2.3	13.0	ns
			2.5 V ± 0.2 V	1.8	5.7	10.4	1.7	10.6	
			3.3 V ± 0.3 V	3.9	8.6	13.5	3.8	13.6	

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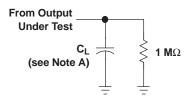
OPERATING CHARACTERISTICS

 $T_A = 25$ °C

	PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
				0.8 V	3.8	
				1.2 V ± 0.1 V	3.7	
		Outputs enabled	f = 10 MHz	1.5 V ± 0.1 V	3.7	pF
			T = 10 MHZ	1.8 V ± 0.15 V	3.7	
				$2.5 \text{ V} \pm 0.2 \text{ V}$	3.9	
_	Dower discination consistence			$3.3 \text{ V} \pm 0.3 \text{ V}$	4	
C_{pd}	Power dissipation capacitance			0.8 V	0	
				1.2 V ± 0.1 V	0	
		Outrote disabled	4 40 MH-	1.5 V ± 0.1 V	0	
		Outputs disabled	f = 10 MHz	1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

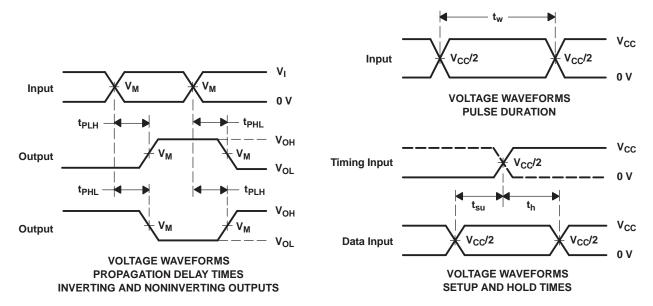


PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L V _M	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}



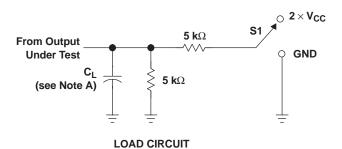
NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , t_{r}/t_{f} = 3 ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

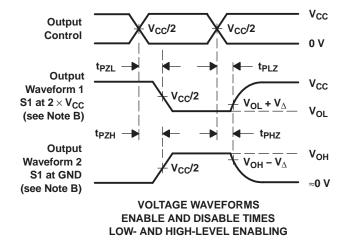


PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S 1
t _{PLZ} /t _{PZL}	$2 \times \mathbf{V_{CC}}$
t _{PHZ} /t _{PZH}	GND

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V \pm 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _∆	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f = 3$ ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
1B2G125DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R
1B2G125DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R
SN74AUP2G125DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R
SN74AUP2G125DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R
SN74AUP2G125DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PV
SN74AUP2G125DQER.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PV
SN74AUP2G125RSER	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PV
SN74AUP2G125RSER.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PV
SN74AUP2G125YFPR	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HMN
SN74AUP2G125YFPR.B	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HMN
SN74AUP2G125YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HMN
SN74AUP2G125YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HMN

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1B2G125DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G125DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G125DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G125RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP2G125YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
SN74AUP2G125YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1B2G125DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G125DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G125DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G125RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP2G125YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
SN74AUP2G125YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



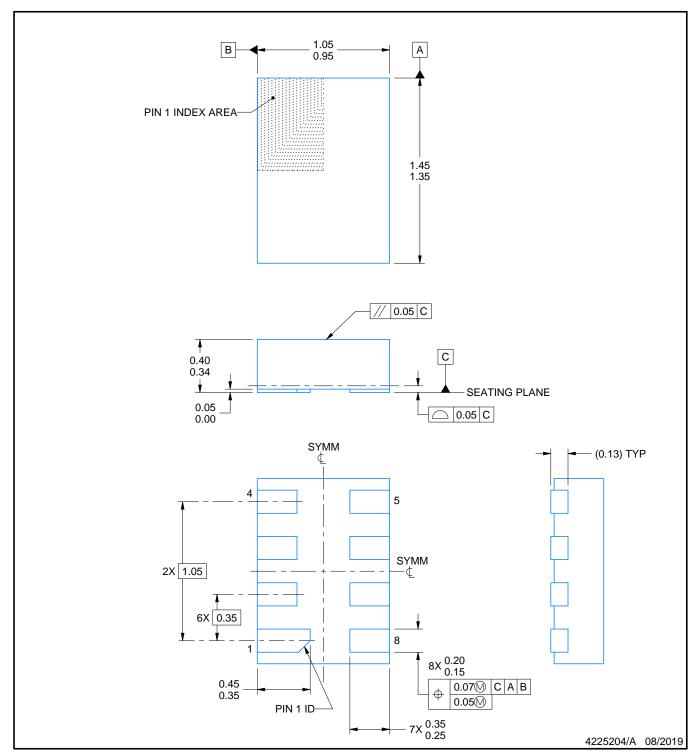
NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

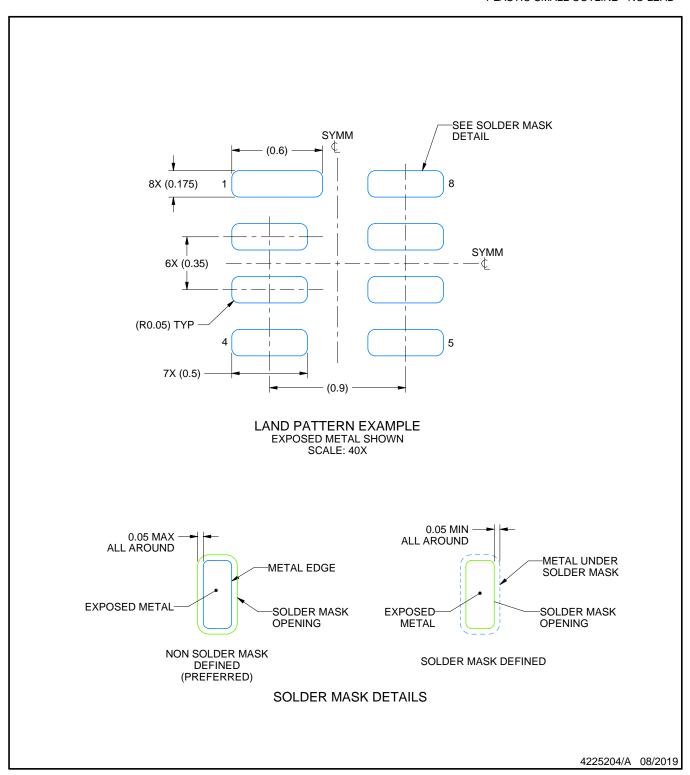
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This package complies to JEDEC MO-287 variation X2EAF.



PLASTIC SMALL OUTLINE - NO LEAD

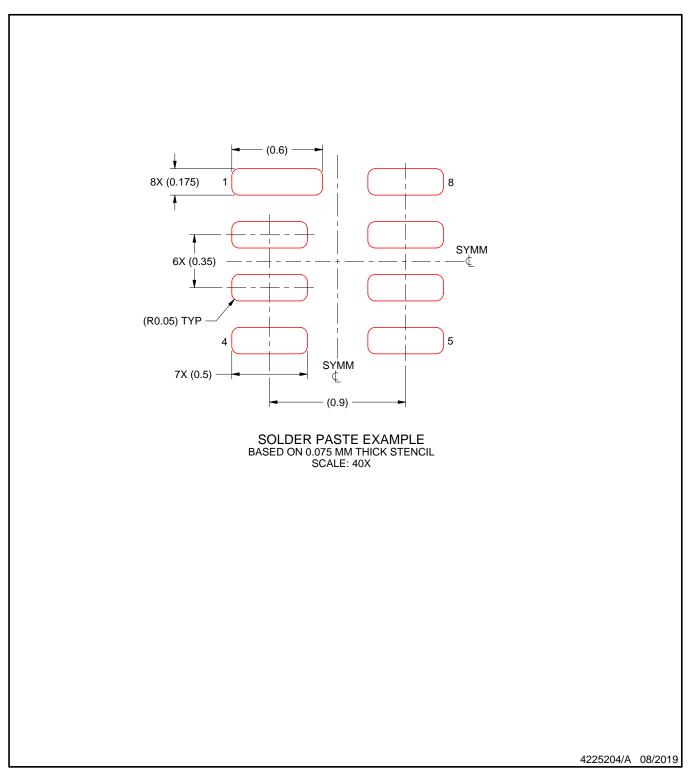


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC SMALL OUTLINE - NO LEAD

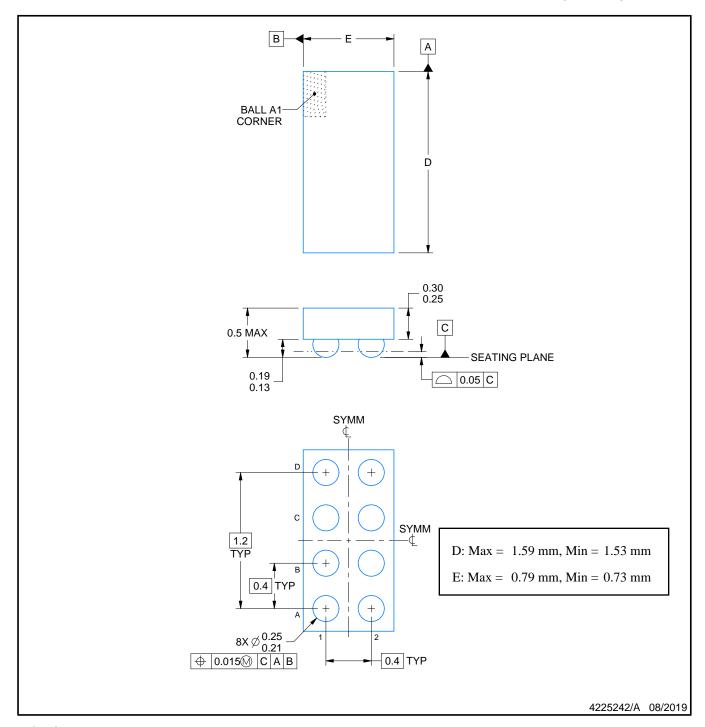


NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





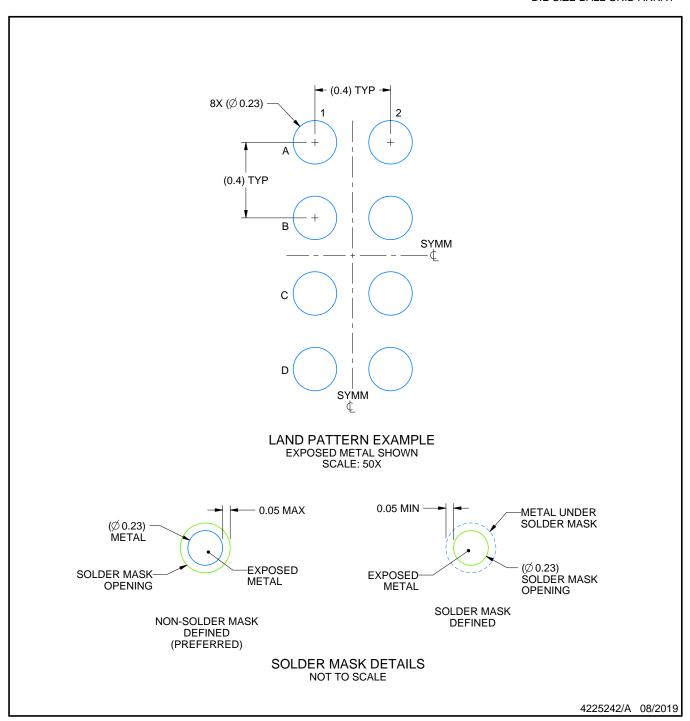


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

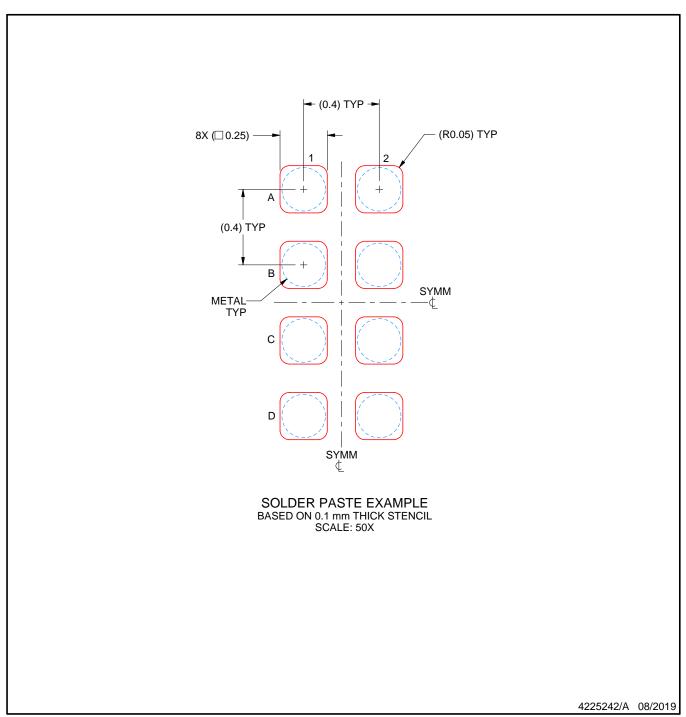




NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).





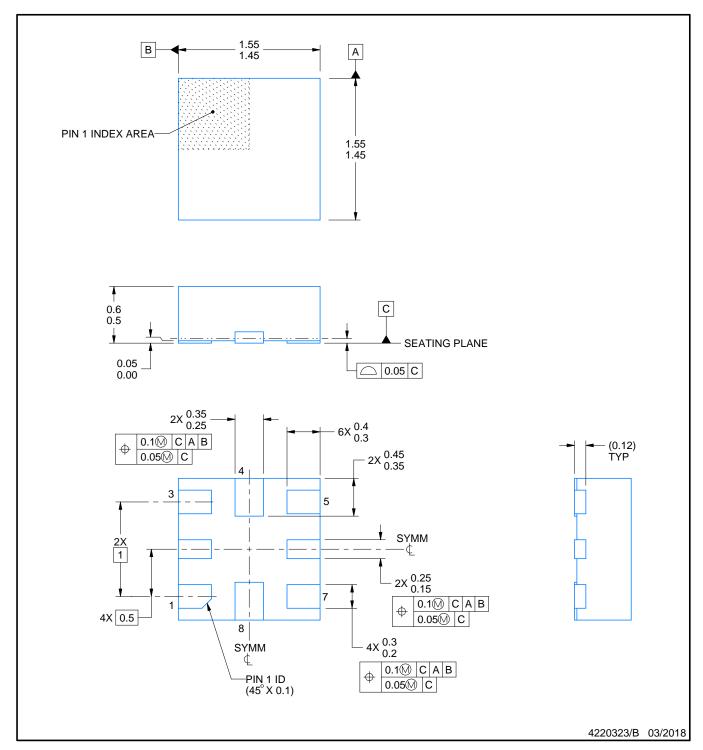
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.





PLASTIC QUAD FLATPACK - NO LEAD

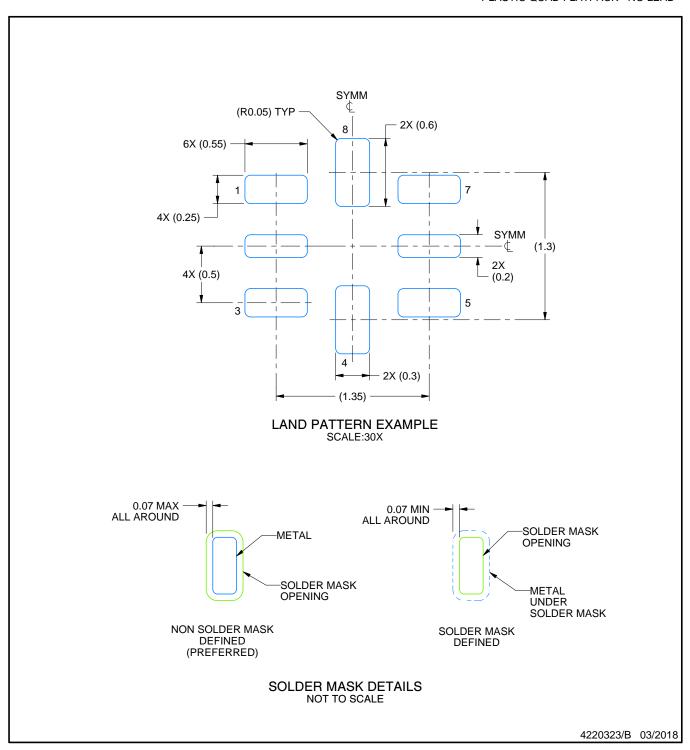


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC QUAD FLATPACK - NO LEAD

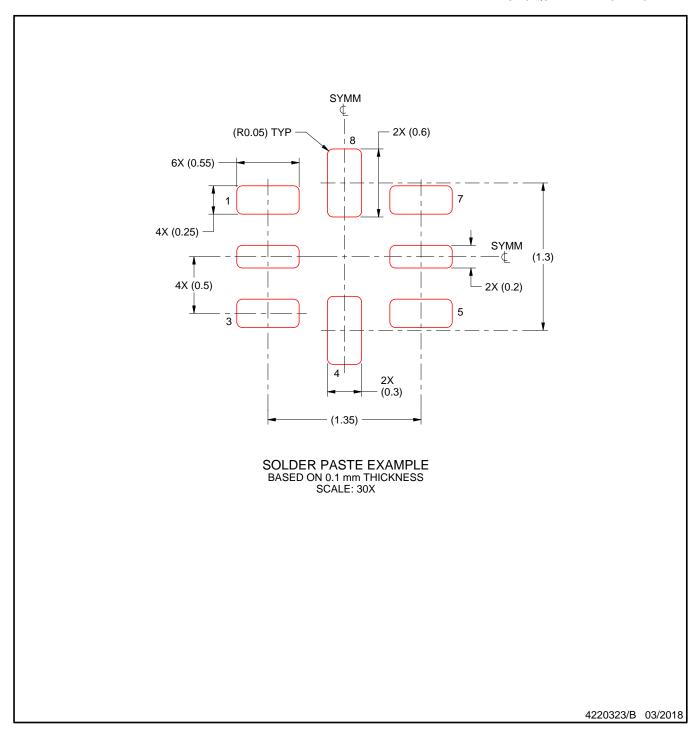


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.





NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).





NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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