

SN74AUP1G32 Low-Power Single 2-Input Positive-OR Gate

1 Features

- Available in the ultra-small 0.64 mm² package (DPW) with 0.5-mm pitch
- Low static-power consumption $(I_{CC} = 0.9 \, \mu A \, Max)$
- Low dynamic-power consumption $(C_{pd} = 4.3 pF Typ at 3.3 V)$
- Low input capacitance ($C_1 = 1.5 pF Typ$)
- Low noise overshoot and undershoot <10% of V_{CC}
- I_{off} Supports live insertion, partial-power-down mode, and back drive protection
- Input hysteresis allows slow input transition and better switching noise immunity at the input ($V_{hys} = 250 \text{ mV typ at } 3.3 \text{ V}$)
- Wide operating V_{CC} range of 0.8 V to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O Tolerant to support mixed-mode signal operation
- t_{pd} = 4.6 ns Max at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD performance tested Per JESD 22
 - 2000-V Human-body model (A114-B, Class II)
 - 1000-V Charged-device model (C101)

2 Applications

- ATCA solutions
- Active noise cancellation (ANC)
- Barcode scanner the end of the datasheet.
- Blood pressure monitor
- **CPAP** machine
- Cable solutions
- DLP 3D machine vision, hyperspectral imaging, optical networking, and spectroscopy
- E-Book
- Embedded PC
- Field transmitter: temperature or pressure sensor
- Fingerprint biometrics
- HVAC: heating, ventilating, and air conditioning
- Network-attached storage (NAS)
- Server motherboard and PSU
- Software defined radio (SDR)
- TV: high-definition (HDTV), LCD, and Digital
- Video communications system
- Wireless data access card, headset, keyboard, mouse, and LAN card
- X-ray: baggage scanner, medical, and dental

3 Description

This single 2-input positive-OR gate performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
	SOT (5)	1.60 mm × 1.20 mm
	USON (6)	1.45 mm × 1.00 mm
SN74AUP1G32	X2SON (4)	0.80 mm × 0.80 mm
	DSBGA (6)	1.19 mm × 0.79 mm
	DSBGA (5)	1.41 mm × 0.91 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



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5 Pin Configuration and Functions

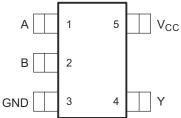


Figure 5-1. DBV Package SOT 5-pin (Top View)



Figure 5-3. DSF Package SON 6-pin (Transparent Top View)

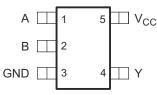
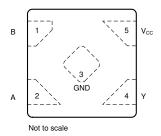


Figure 5-5. DCK Package SC70 5-pin (Top View)



See mechanical drawings at the end of the data sheet for all package dimensions

Figure 5-7. DPW Package X2SON 5-pins (Transparent Top View)

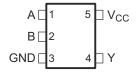


Figure 5-2. DRL Package SOT 5-pin (Top View)

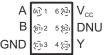


N.C. - No internal connection

Figure 5-4. DRY Package SON 6-pin (Transparent Top View)



Figure 5-6. YZP Package DSBGA 5-balls (Transparent Top View)



DNU - Do Not Use

Figure 5-8. YFP Package DSBGA 6-balls (Transparent Top View)

Pin Functions

		PIN					
NAME	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP	I/O	DESCRIPTION
Α	1	2	1	A1	A1	I	Input A
В	2	1	2	B1	B1	I	Input B
GND	3	3	3	C1	C1	-	Ground
Y	4	4	4	C2	C2	0	Output Y
V _{CC}	5	5	6	A2	A2	-	Power Pin



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high or low state ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature rang	е	-65	125	°C
\/	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
V _(ESD)	Liectiostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1)			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	3.6	V
		V _{CC} = 0.8 V	V _{cc}		
,	High level input voltage	V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.6		V
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 0.8 V		0	
.,	' _{IL} Low-level input voltage	V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}	V
VIL		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.9	
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 0.8 V		-20	μΑ
		V _{CC} = 1.1 V		-1.1	
	High lovel output ourrant	V _{CC} = 1.4 V		-1.7	
I _{OH}	High-level output current	V _{CC} = 1.65 V		-1.9	mA
		V _{CC} = 2.3 V		-3.1	
		V _{CC} = 3 V		-4	

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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see (1)			MIN MA	X UNIT
		V _{CC} = 0.8 V		20 μΑ
		V _{CC} = 1.1 V		.1
I _{OI} Low-level output current	V _{CC} = 1.4 V		.7	
IOL	Low-level output current	V _{CC} = 1.65 V	,	.9 mA
		V _{CC} = 2.3 V	3	3.1
		V _{CC} = 3 V		4
Δt/Δν	Input transition rise and fall rate	V _{CC} = 0.8 V to 1.95 V	2	00 ns/V
T _A	Operating free-air temperature	·	-40	85 °C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	DBV	DCK	DRL	DSF	DRY	DPW	UNIT
	THERMAL METRIC	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	UNII
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard data sheet value)	271.4	338.4	349.7	407.1	554.9	492.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (standard data sheet value)	213.5	110.6	120.5	232.0	385.4	232.6	°C/W
R _{θJB}	Junction-to-board thermal resistance (standard data sheet value)	108.2	118.8	171.4	306.9	388.2	355.4	°C/W
ΨЈТ	Junction-to-top characterization parameter (standard data sheet value)	89.3	3.0	10.8	40.3	159.0	37.4	°C/W
ΨЈВ	Junction-to-board characterization parameter (standard data sheet value)	107.6	117.8	169.4	306.0	384.1	353.9	°C/W
ΨJC(bot)	Junction-to-case (bottom) thermal resistance (standard data sheet value)	_	_	_	_	_	147.9	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	TA	= 25°C	$T_A = -40^{\circ}C$ to $85^{\circ}C$	LINUT
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP MAX	MIN MA	UNIT
	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1	
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}	
	I _{OH} = -1.7 mA	1.4 V	1.11		1.03	
.,	I _{OH} = -1.9 mA	1.65 V	1.32		1.3	V
V _{OH}	I _{OH} = -2.3 mA	2.3 V	2.05		1.97	v
	I _{OH} = -3.1 mA	2.3 V	1.9		1.85	
	I _{OH} = -2.7 mA	3 V	2.72		2.67	
	I _{OH} = -4 mA	3 V	2.6		2.55	
	I _{OL} = 20 μA	0.8 V to 3.6 V		0.1	0.	1
	I _{OL} = 1.1 mA	1.1 V		0.3 × V _{CC}	0.3 × V _C	С
	I _{OL} = 1.7 mA	1.4 V		0.31	0.3	7
N/	I _{OL} = 1.9 mA	1.65 V		0.31	0.3	5 V
V _{OL}	I _{OL} = 2.3 mA	2.3 V		0.31	0.3	3 V
	I _{OL} = 3.1 mA	2.3 V		0.44	0.4	5
	I _{OL} = 2.7 mA	3 V		0.31	0.3	3
	I _{OL} = 4 mA	3 V		0.44	0.4	5
I _I A or B input	V _I = GND to 3.6 V	0 V to 3.6 V		0.1	0.	5 μΑ
I _{off}	V_{I} or $V_{O} = 0 \text{ V to } 3.6 \text{ V}$	0 V		0.2	0.	6 µA
ΔI_{off}	V_{I} or $V_{O} = 0 \text{ V to } 3.6 \text{ V}$	0 V to 0.2 V		0.2	0.	6 µA
Icc	$V_I = GND \text{ or } (V_{CC} \text{ to } 3.6 \text{ V}),$ $I_O = 0$	0.8 V to 3.6 V		0.5	0.	9 μΑ
ΔI _{CC}	$V_1 = V_{CC} - 0.6 V^{(1)},$ $I_0 = 0$	3.3 V		40	5	0 μΑ
	V = V = CND	0 V		1.5		
C _i	V _I = V _{CC} or GND	3.6 V		1.5		pF
C _o	V _O = GND	0 V		3		pF

⁽¹⁾ One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

6.6 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER	PARAMETER FROM TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -4 to 85°	UNIT			
		(001701)	''	MIN	TYP	MAX	MIN	MAX		
		0.8 V		18						
		Y			1.2 V ± 0.1 V	2.6	7.3	13.5	2.1	16.8
	A D		1.5 V ± 0.1 V	1.4	5.2	9.1	0.9	11		
^L pd	t _{pd} A or B		1.8 V ± 0.15 V	1	4.2	7	0.5	8.8	ns	
		2.5 V ± 0.2 V	1	3	4.7	0.5	6			
		3.3 V ± 0.3 V	1	2.4	3.7	0.5	4.6			

6.7 Switching Characteristics, $C_L = 10 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40 to 85°	UNIT	
	(INPUT)			MIN	TYP	MAX	MIN	MAX	
			0.8 V		21				
		Y	1.2 V ± 0.1 V	1.5	8.5	15.4	1	18.4	ns
	A or D		1.5 V ± 0.1 V	1	6.2	10.4	0.5	12	
L _{pd}	t _{pd} A or B		1.8 V ± 0.15 V	1	5	8.1	0.5	9.6	
			2.5 V ± 0.2 V	1	3.6	5.5	0.5	6.6	
			3.3 V ± 0.3 V	1	2.9	4.4	0.5	5	

6.8 Switching Characteristics, $C_L = 15 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
			0.8 V		24				
		Y	1.2 V ± 0.1 V	3.6	9.9	17	3.1	21.1	ns
	A or B		1.5 V ± 0.1 V	2.3	7.2	11.5	1.8	13.9	
t _{pd}	AOIB		1.8 V ± 0.15 V	1.6	5.8	9.1	1.1	11.2	
			2.5 V ± 0.2 V	1	4.3	6.2	0.5	7.8	
			3.3 V ± 0.3 V	1	3.4	5	0.5	6.2	

6.9 Switching Characteristics, C_L = 30 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	T,	_A = 25°C		T _A = -4 to 85°	UNIT	
	(INFOT)			MIN	TYP	MAX	MIN	MAX	
			0.8 V		32.8				
		Y	1.2 V ± 0.1 V	4.9	13.1	21.6	4.4	26.7	ns
	A or B		1.5 V ± 0.1 V	3.4	9.5	14.6	2.9	17.6	
t _{pd}	AOIB		1.8 V ± 0.15 V	2.5	7.7	11.4	2	14.1	
			2.5 V ± 0.2 V	1.8	5.7	7.9	1.3	9.9	
			3.3 V ± 0.3 V	1.5	4.7	6.4	1	7.8	

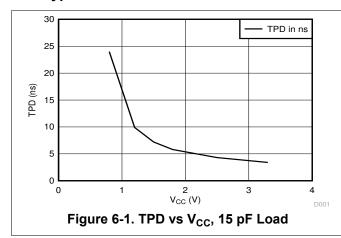


6.10 Operating Characteristics

T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT
			0.8 V	4.1	
			1.2 V ± 0.1 V	4.1	
	Power dissipation capacitance	f = 10 MHz	1.5 V ± 0.1 V	4.1	pF
C _{pd}		1 – 10 IVII 12	1.8 V ± 0.15 V	4.1	Pi
			2.5 V ± 0.2 V	4.2	
			3.3 V ± 0.3 V	4.3	

6.11 Typical Characteristics



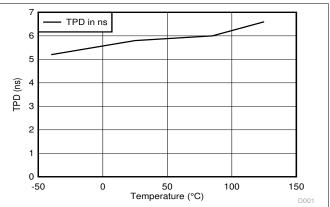
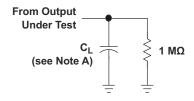


Figure 6-2. Temperature 1.8 V, 15 pF Load

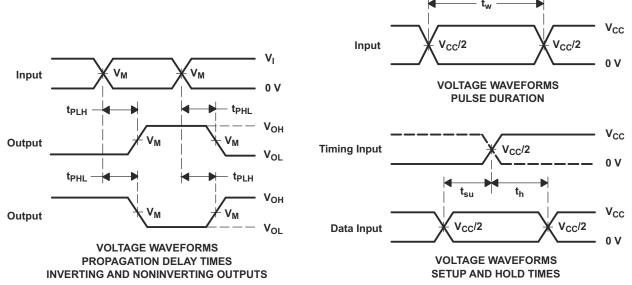
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width



LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	$V_{CC} = 2.5 V$ $\pm 0.2 V$	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}

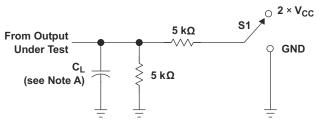


- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, t_r and $t_f = 3$ ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms



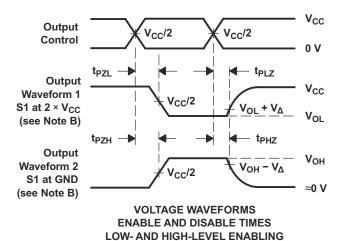
7.2 Enable and Disable Times



TEST	S1
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _D	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- A. C_L includes probe and jig capacitance.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, t_r and $t_f = 3$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 7-2. Load Circuit and Voltage Waveforms



8 Detailed Description

8.1 Overview

This single 2-input positive-OR gate that operates from 0.8 V to 3.6 V and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The AUP family of devices has quiescent power consumption less than 1 μ A and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- · Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- · Low noise due to slower edge rates

8.4 Device Functional Modes

Table 8-1. Function Table

INP	UTS	OUTPUT
Α	В	Y
L	L	L
L	Н	Н
н	L	Н
н	Н	Н

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

The AUP family of single gate logic makes excellent translators for the new lower voltage Micro- processors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

9.2 Typical Application

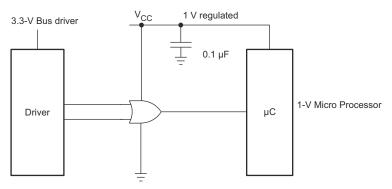


Figure 9-1. Typical Application Schematic

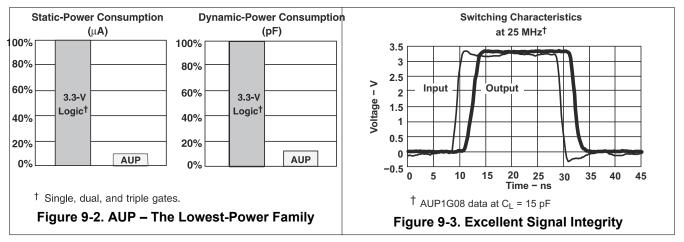
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

- 1. Recommended Input conditions
 - Rise time and fall time specifications. See (Δt/ΔV) in Recommended Operating Conditions table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
- 2. Recommend output conditions
 - Load currents should not exceed 20 mA on the output and 50 mA total for the part
 - Outputs should not be pulled above V_{CC}

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended and if there are multiple V_{CC} terminals then .01 μ F or .022 μ F is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the guick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments Incorporated.
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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AUP1G32DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HG R)
SN74AUP1G32DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HG R)
SN74AUP1G32DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGR)
SN74AUP1G32DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGR)
SN74AUP1G32DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG5
SN74AUP1G32DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG5
SN74AUP1G32DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4
SN74AUP1G32DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4
SN74AUP1G32DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HG7, HGR)
SN74AUP1G32DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HG7, HGR)
SN74AUP1G32DRY2	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRY2.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSF2	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSF2.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG





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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AUP1G32YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	HGN
SN74AUP1G32YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN
SN74AUP1G32YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN
SN74AUP1G32YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G32DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74AUP1G32DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G32DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G32DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G32DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G32DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G32DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G32DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G32DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G32DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G32DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DSF2	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0



PACKAGE MATERIALS INFORMATION

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	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	SN74AUP1G32YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4211218-3/D







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. The size and shape of this feature may vary.





NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.





NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



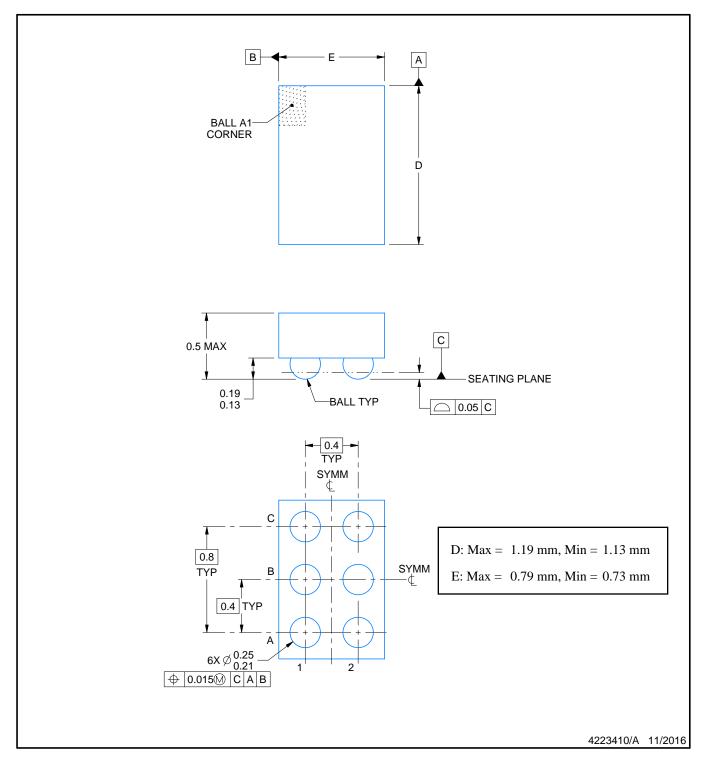


NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



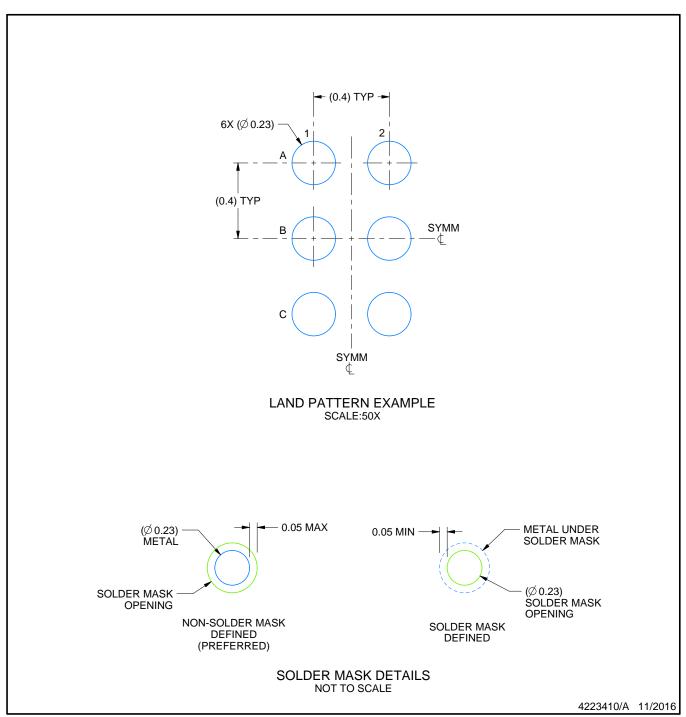




NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.

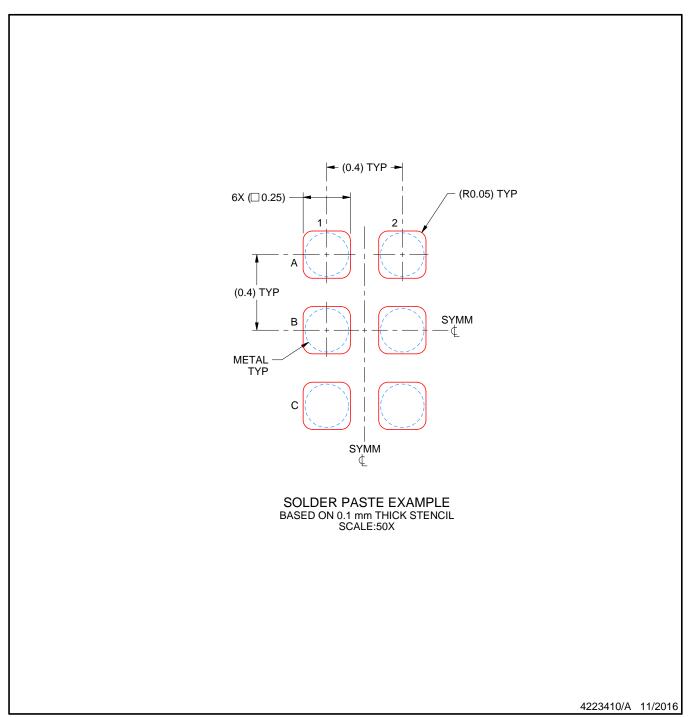




NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).





NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025