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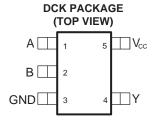
# Low-Power Single 2-Input Positive-AND Gate

Check for Samples: SN74AUP1G08-Q1

#### **FEATURES**

- **AEC-Q100 Qualified with the Following** Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Available in the Texas Instruments NanoStar™ **Package**
- **Low Static-Power Consumption:**  $I_{CC} = 0.9 \mu A Max$
- Low Dynamic-Power Consumption:  $C_{pd}$  = 4.3 pF Typ at 3.3 V
- Low Input Capacitance: C<sub>i</sub> = 1.5 pF Typ
- **Low Noise: Overshoot and Undershoot** < 10% of  $V_{CC}$
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise** Immunity at the Input ( $V_{hys} = 250 \text{ mV}$ , Typ at 3.3 V)

- Wide Operating V<sub>CC</sub> Range of 0.8 V to 3.6 V
- **Optimized for 3.3-V Operation**
- 3.6-V Input/Output (I/O) Tolerant to Support **Mixed-Mode Signal Operation**
- $t_{pd}$  = 4.3 ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD-78, Class II



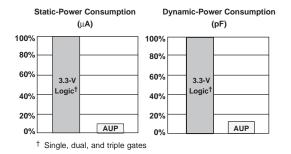
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# TEXAS INSTRUMENTS

#### DESCRIPTION

The AUP family is Tl's premier solution to the low-power needs of the industry in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).



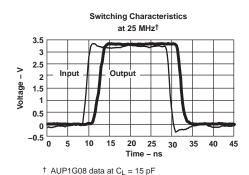


Figure 1. AUP - The Lowest-Power Family

Figure 2. Excellent Signal Integrity

This single 2-input positive-AND gate performs the Boolean function:  $Y = A \bullet B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

NanoStar package technology is a major breakthrough in integrated circuit (IC) packaging concepts, because it uses the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### ORDERING INFORMATION(1)

T <sub>A</sub>	ORDERABLE PART NUMBER (2)	TOP-SIDE MARKING
-40°C to 125°C	SN74AUP1G08QDCKRQ1	SIT

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

## **LOGIC DIAGRAM (POSITIVE LOGIC)**



## **ABSOLUTE MAXIMUM RATINGS**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
VI	Input voltage range <sup>(2)</sup>		-0.5	4.6	V
Vo	Voltage range applied to any output in the	high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
Vo	Output voltage range in the high or low sta	ate <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
lok	Output clamp current	V <sub>O</sub> < 0		-50	mA
lo	Continuous output current	•		±20	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature range		-65	150	°C
ESD	Human body model (HBM) AEC-Q100 class	ssification level H2		2	kV
ratings	Charged device model (CDM) AEC-Q100	classification level C3B		750	V

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

	TUEDAMA METDIO(1)	SN74AUP1G08-Q1	
	THERMAL METRIC <sup>(1)</sup>	DCK (5 PINS)	UNIT
$\theta_{JA}$	Junction-to-ambient thermal resistance	304.7	
$\theta_{JCtop}$	Junction-to-case (top) thermal resistance	115.3	
$\theta_{JB}$	Junction-to-board thermal resistance	80.3	00/14/
$\Psi_{JT}$	Junction-to-top characterization parameter	3.5	°C/W
ΨЈВ	Junction-to-board characterization parameter	79.4	
$\theta_{JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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Product Folder Links: SN74AUP1G08-Q1

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## **RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0.8	3.6	V
		$V_{CC} = 0.8 \text{ V}$	V <sub>CC</sub>		
.,	High level input valtage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	0.65 × V <sub>CC</sub>		V
V <sub>IH</sub>	Supply voltage  High-level input voltage  Low-level input voltage  Input voltage  Output voltage  High-level output current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6		V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> 0.65 × V <sub>CC</sub> 1.6 2		
		$V_{CC} = 0.8 \text{ V}$		0	
.,	Laur laural imputuraltana	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.9	
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	$V_{CC}$	V
		$V_{CC} = 0.8 \text{ V}$		-20	μΑ
		V <sub>CC</sub> = 1.1 V		-1.1	
	High lovel output ourrent	$V_{CC} = 1.4 \text{ V}$		-1.7	
I <sub>OH</sub>	nigii-level output current	V <sub>CC</sub> = 1.65		-1.9	mA
	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$		-3.1		
		$V_{CC} = 3 V$		0 0 0.35 × V <sub>CC</sub> 0.7 0.9 0 3.6 0 V <sub>CC</sub> -20 -1.1 -1.7 -1.9 -3.1 -4 20 1.1 1.7 1.9 3.1 4	
		$V_{CC} = 0.8 \text{ V}$		20	μA
		V <sub>CC</sub> = 1.1 V		1.1	
	Low lovel output ourrent	$V_{CC} = 1.4 \text{ V}$		1.7	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		1.9	mA
		$V_{CC} = 2.3 \text{ V}$		3.1	
		$V_{CC} = 3 V$		4	
Δt/Δν	Input transition rise or fall rate	V <sub>CC</sub> = 0.8 V to 3.6 V		200	ns/V
T <sub>A</sub>	Operating free-air temperature	·	-40	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	T <sub>A</sub>	= 25°C		$T_A = -40$ °C to	85°C	T <sub>A</sub> = 125	5°C	UNIT
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
	I <sub>OH</sub> = -20 μA	0.8 V to 3.6 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1		V <sub>CC</sub> - 0.1		
	$I_{OH} = -1.1 \text{ mA}$	1.1 V	$0.75 \times V_{CC}$			$0.7 \times V_{CC}$		$0.7 \times V_{CC}$		
	$I_{OH} = -1.7 \text{ mA}$	1.4 V	1.11			1.03		1.03		
V <sub>OH</sub>	$I_{OH} = -1.9 \text{ mA}$	1.65 V	1.32			1.3		1.3		V
	$I_{OH} = -2.3 \text{ mA}$	2.3 V	2.05			1.97		1.97		
	$I_{OH} = -3.1 \text{ mA}$	2.3 V	1.9			1.85		1.85		
	$I_{OH} = -2.7 \text{ mA}$	3 V	2.72			2.67		2.67		
	I <sub>OH</sub> = -4 mA	3 V	2.6			2.55		2.55		

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## **ELECTRICAL CHARACTERISTICS (continued)**

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C	to 85°C	T <sub>A</sub> = 125	5°C	LINUT
PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN TYP N	IAX	MIN	MAX	MIN	0.1 0.3 × V <sub>CC</sub> 0.37 0.35 0.33 0.45 0.33 0.45 0.5 0.8	UNIT
	I <sub>OL</sub> = 20 μA	0.8 V to 3.6 V		0.1		0.1		0.1	
	$I_{OL} = 1.1 \text{ mA}$	1.1 V	0.3 ×	$V_{CC}$		$0.3 \times V_{CC}$	0	$3 \times V_{CC}$	
	$I_{OL} = 1.7 \text{ mA}$	1.4 V	(	0.31		0.37		0.37	
V <sub>OL</sub>	$I_{OL} = 1.9 \text{ mA}$	1.65 V	(	0.31		0.35		0.35	V
	$I_{OL} = 2.3 \text{ mA}$	221/	(	0.31		0.33		0.33	
	$I_{OL} = 3.1 \text{ mA}$	2.3 V	(	).44		0.45		0.45	
	I <sub>OL</sub> = 2.7 mA	2.1/	(	).31		0.33		0.33	
	I <sub>OL</sub> = 4 mA	3 V	(	).44		0.45		0.45	
I <sub>I</sub> A or B input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V		0.1		0.5		0.5	μΑ
I <sub>off</sub>	$V_I$ or $V_O = 0$ V to 3.6 V	0 V		0.2		0.6		0.8	μΑ
$\Delta I_{\text{off}}$	$V_I$ or $V_O = 0$ V to 3.6 V	0 V to 0.2 V		0.2		0.6		0.8	μΑ
I <sub>CC</sub>	$V_I = GND \text{ or}$ $(V_{CC} \text{ to } 3.6 \text{ V}),$ $I_O = 0$	0.8 V to 3.6 V		0.5		0.9		1.2	μА
ΔI <sub>CC</sub>	$V_I = V_{CC} - 0.6 V^{(1)},$ $I_O = 0$	3.3 V		40		50		23	μΑ
	V – V or CND	0 V	1.5						n.E
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.6 V	1.5						pF
Co	V <sub>O</sub> = GND	0 V	3						pF

<sup>(1)</sup> One input at  $V_{CC}$  – 0.6 V, other input at  $V_{CC}$  or GND.

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 5 pF$  (unless otherwise noted) (see Figure 3 and Figure 4)

DADAMETED	FROM (INPUT)	TO (OUTPUT)	V <sub>cc</sub>	T,	λ = 25°C		$T_A = -40^{\circ}C$ to	UNIT	
PARAMETER				MIN	TYP	MAX	MIN	MAX	UNIT
		Y	0.8 V		18				
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	ns
4	A or B		1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
$t_{pd}$	AUID		1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

## **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 10 \text{ pF}$  (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	TO (OUTPUT)	V <sub>cc</sub>	T,	<sub>λ</sub> = 25°C		$T_A = -40^{\circ}C$ to	UNIT	
PARAMETER	(INPUT)			MIN	TYP	MAX	MIN	MAX	ONIT
			0.8 V		21				
		Y	1.2 V ± 0.1 V	1.5	8.5	14.7	1	17.2	ns
	A or B		1.5 V ± 0.1 V	1	6.2	10	0.5	11.3	
t <sub>pd</sub>	AUIB		1.8 V ± 0.15 V	1	5	7.7	0.5	9	
			2.5 V ± 0.2 V	1	3.6	5.2	0.5	6.1	
			3.3 V ± 0.3 V	1	2.9	4.2	0.5	4.7	

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#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 3 and Figure 4)

DADAMETED	FROM	TO (OUTPUT)	V	T <sub>A</sub> = 25°C			$T_A = -40^{\circ}C$ to	85°C	UNIT
PARAMETER	(INPUT)		V <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	UNII
		Y	0.8 V		24				
			1.2 V ± 0.1 V	3.6	9.9	16.3	3.1	19.9	
	A or B		1.5 V ± 0.1 V	2.3	7.2	11.1	1.8	13.2	
t <sub>pd</sub>	AOID		1.8 V ± 0.15 V	1.6	5.8	8.7	1.1	10.6	ns
		2.5 V ± 0.2 V	1	4.3	5.9	0.5	7.3		
			3.3 V ± 0.3 V	1	3.4	4.8	0.5	5.9	

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range, C<sub>L</sub> = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	TO (OUTPUT)	V <sub>cc</sub>	T <sub>A</sub> = 25°C		$T_A = -40^{\circ}C t$	o 85°C	T <sub>A</sub> = 125°C		UNIT	
PARAMETER	(INPUT)			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			0.8 V		32.8						
		or B Y	1.2 V ± 0.1 V	4.9	13.1	20.9	4.4	25.5	4.4	27.8	
	A or D		1.5 V ± 0.1 V	3.4	9.5	14.2	2.9	16.9	2.9	18	no
t <sub>pd</sub>	AUID		1.8 V ± 0.15 V	2.5	7.7	11	2	13.5	2	19.7	ns
			2.5 V ± 0.2 V	1.8	5.7	7.6	1.3	9.4	1.3	11	
			3.3 V ± 0.3 V	1.5	4.7	6.2	1	7.5	1	8.7	

## **OPERATING CHARACTERISTICS**

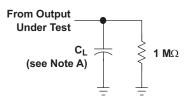
 $T_{\Delta} = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	TYP	UNIT
			0.8 V	4	
			1.2 V ± 0.1 V	4	- pF
_	Davies discination associations		1.5 V ± 0.1 V	4	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

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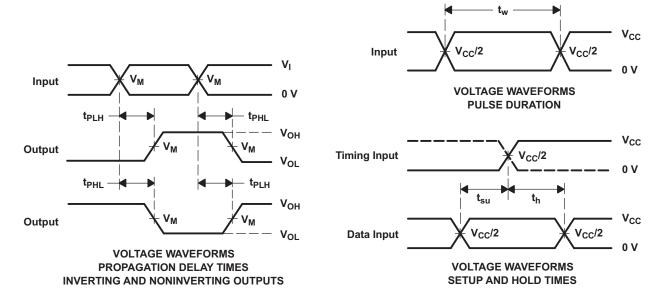
# PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

 $T_{\Delta}$  = -25°C to 85°C

	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V
C <sub>L</sub>	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V <sub>M</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>I</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>



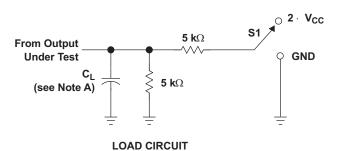
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



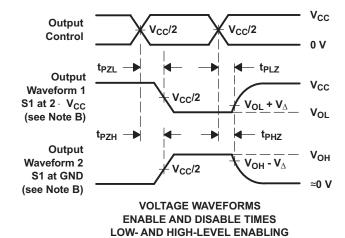
# PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 · V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

 $T_{A} = -25^{\circ}C \text{ to } 85^{\circ}C$ 

	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	$V_{CC}$ = 3.3 V $\pm$ 0.3 V
CL	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
<b>V</b> <sub>M</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2
VI	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
$oldsymbol{V}_\Delta$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AUP1G08QDCKRQ1	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(SIJ, SIT)
SN74AUP1G08QDCKRQ1.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(SIJ, SIT)

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74AUP1G08-Q1:

Catalog: SN74AUP1G08

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 11-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$  Catalog - TI's standard catalog product

## PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G08QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

# **PACKAGE MATERIALS INFORMATION**

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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G08QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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