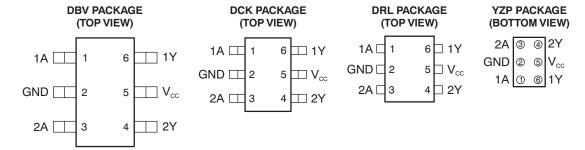


FEATURES

- Available in the Texas Instruments
 NanoFree[™] Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.6 ns at 1.8 V

- Low Power Consumption, 10 μA at 1.8 V
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This dual buffer gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC2G34 performs the Boolean function Y = A in positive logic.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoFree [™] – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G34YZPR	U9_
-40°C to 85°C	SOT-563 – DRL	Reel of 4000	SN74AUC2G34DRLR	U9_
	SOT-23 – DBV	Reel of 3000	SN74AUC2G34DBVR	U34_
	SC-70 - DCK	Reel of 3000	SN74AUC2G34DCKR	U9_

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

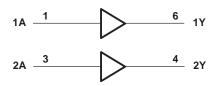
⁽²⁾ DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



FUNCTION TABLE (EACH GATE)

INPUT A	OUTPUT Y
Н	Н
L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.1	V
Vo	Voltage range applied to any output in the I	high-impedance or power-off state ⁽²⁾	-0.5	4.1	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±100	mA
		DBV package		165	
	Decline the survey line and a sec (3)	DCK package		259	°C/W
θ_{JA}	Package thermal impedance (3)	DRL package		142	C/VV
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUC2G34



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{cc}		
V_{IH}	High-level input voltage	V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 0.8 V		0	
V_{IL}	Low-level input voltage	V _{CC} = 1.1 V to 1.95 V	(0.35 × V _{CC}	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
V _I	Input voltage		0	3.6	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 0.8 V		-0.7	
		V _{CC} = 1.1 V		-3	
I_{OH}	OH High-level output current	gh-level output current $V_{CC} = 1.4 \text{ V}$			mA
		V _{CC} = 1.65 V		-8	
		V _{CC} = 2.3 V		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
I_{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		V _{CC} = 2.3 V		9	
		$V_{CC} = 0.8 \text{ V to } 1.65 \text{ V}^{(2)}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}^{(3)}$		20	ns/V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}^{(3)}$		10	
T _A	Operating free-air temperature		-40	85	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
 The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).
 The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1)	MAX	UNIT
	$I_{OH} = -100 \mu A$	0.8 V to 2.7 V	V _{CC} – 0.1		
	$I_{OH} = -0.7 \text{ mA}$	0.8 V	0.55		
V	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8		V
V _{OH}	$I_{OH} = -5 \text{ mA}$	1.4 V	1		V
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2		
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8		
	I _{OL} = 100 μA	0.8 V to 2.7 V		0.2	
	$I_{OL} = 0.7 \text{ mA}$	0.8 V	0.25		
V	I _{OL} = 3 mA	1.1 V		0.3	V
V _{OL}	I _{OL} = 5 mA	1.4 V		0.4	V
	I _{OL} = 8 mA	1.65 V		0.45	
	I _{OL} = 9 mA	2.3 V		0.6	
I _I A inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V		±5	μΑ
I _{off}	V_I or $V_O = 2.7 V$	0		±10	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V		10	μΑ
C _i	$V_I = V_{CC}$ or GND	2.5 V	2		pF

⁽¹⁾ All typical values are at $T_A = 25$ °C.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = ± 0.	1.2 V 1 V	V _{CC} = ± 0.			c = 1.8 0.15 \		V _{CC} = ± 0.		UNIT
	(INFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	А	Y	6.4	0.7	3.4	0.6	2.3	0.6	1	1.6	0.5	1.2	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		_C = 1.8 : 0.15 \		V _{CC} = ± 0.		UNIT
	(INFOT)	(001701)	MIN	TYP	MAX	MIN	MAX	
t _{pd}	А	Υ	0.7	1.3	2.4	0.6	1.8	ns

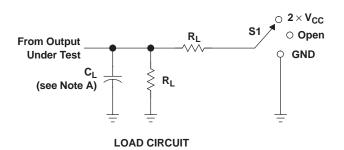
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	12	12	12	13	14	pF

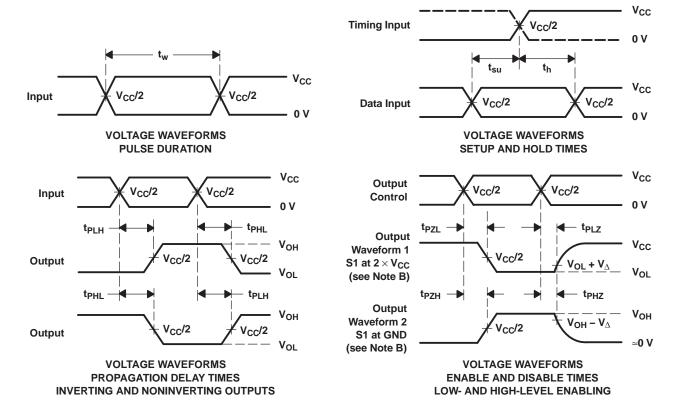


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	$2 \times V_{CC}$
t _{PHZ} /t _{PZH}	GND

V _{CC}	CL	R _L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
1.8 V ± 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74AUC2G34DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U34R
SN74AUC2G34DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U34R
SN74AUC2G34DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U95, U9F, U9R)
SN74AUC2G34DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U95, U9F, U9R)
SN74AUC2G34DCKRE4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U95, U9F, U9R)
SN74AUC2G34DRLR	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1KB, U97, U9R)
SN74AUC2G34DRLR.B	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1KB, U97, U9R)
SN74AUC2G34DRLRG4	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1KB
SN74AUC2G34DRLRG4.B	Active	Production	SOT-5X3 (DRL) 6	4000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1KB
SN74AUC2G34YZPR	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U9N
SN74AUC2G34YZPR.B	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U9N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G34DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC2G34DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74AUC2G34DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74AUC2G34YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G34DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUC2G34DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74AUC2G34DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74AUC2G34YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0



PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-293 Variation UAAD



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





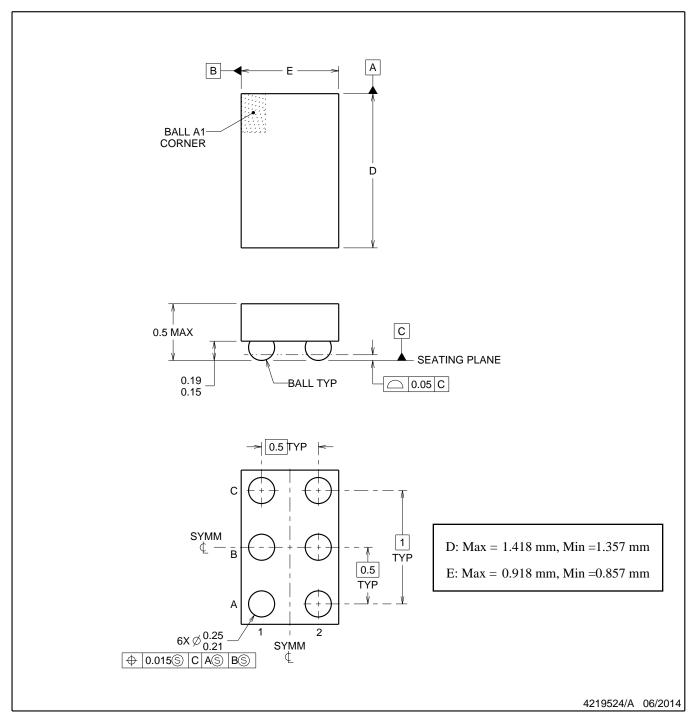
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. NanoFree[™] package configuration.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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