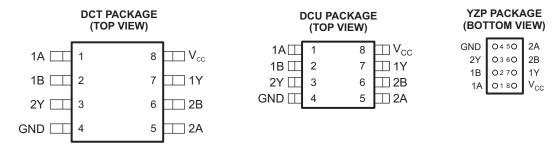


FEATURES

- Available in the Texas Instruments
 NanoFree[™] Package
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{nd} of 1.5 ns at 1.8 V

- Low Power Consumption, 10 μA at 1.8 V
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual 2-input positive-OR gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC2G32 performs the Boolean function Y = A + B or $Y = \overline{A} \times \overline{B}$ in positive logic.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
-40°C to 85°C	NanoFree – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G32YZPR	UG_
	SSOP - DCT	Reel of 3000	SN74AUC2G32DCTR	U32
	VSSOP - DCU	Reel of 3000	SN74AUC2G32DCUR	U32

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

⁽²⁾ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



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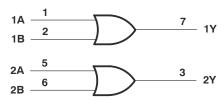
All other trademarks are the property of their respective owners.



FUNCTION TABLE (each gate)

	INPUTS		OUTPUT
1	4	В	Υ
H	1	Χ	Н
>	<	Н	Н
L	_	L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range (2)		-0.5	3.6	V
Vo	Voltage range applied to any output in the high-impe	edance or power-off state ⁽²⁾	-0.5	3.6	V
Vo	Output voltage range (2)		-0.5	V _{CC} + 0.5	V
I_{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current		–50 mA	mA	
Io	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCT package		220	°C/W
θ_{JA}	Package thermal impedance ⁽³⁾	DCU package		227	°C/W
θ_{JA}	Package thermal impedance ⁽³⁾	YZP package		102	°C/W
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT		
V _{CC}	Supply voltage		0.8	2.7	V		
		V _{CC} = 0.8 V	V _{cc}				
V _{IH}	High-level input voltage	V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		V		
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7				
		V _{CC} = 0.8 V		0			
V_{IL}	Low-level input voltage	V _{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	V		
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7			
VI	Input voltage		0	3.6	V		
Vo	Output voltage		0	V _{CC}	V		
	l _{OH} High-level output current	V _{CC} = 0.8 V		-0.7			
		V _{CC} = 1.1 V		-3			
I _{OH}		V _{CC} = 1.4 V		-5	mA		
		V _{CC} = 1.65 V		-8			
		V _{CC} = 2.3 V		-9			
		V _{CC} = 0.8 V		0.7			
		V _{CC} = 1.1 V		3			
I _{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA		
		V _{CC} = 1.65 V		8			
		V _{CC} = 2.3 V		9			
Δt/ΔV	Input transition rise or fall rate			20	ns/V		
T _A	Operating free-air temperature		-40	85	°C		

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

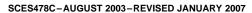
Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMET	ER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT			
		I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} - 0.1						
		$I_{OH} = -0.7 \text{ mA}$	0.8 V		0.55					
V		$I_{OH} = -3 \text{ mA}$	1.1 V	0.8			V			
V _{OH}		I _{OH} = -5 mA	1.4 V	1			V			
		$I_{OH} = -8 \text{ mA}$	1.65 V	1.2						
		$I_{OH} = -9 \text{ mA}$	2.3 V	1.8						
		I _{OL} = 100 μA	0.8 V to 2.7 V			0.2				
		$I_{OL} = 0.7 \text{ mA}$ 0.8 V			0.25					
M		I _{OL} = 3 mA	1.1 V			0.3	V			
V _{OL}		I _{OL} = 5 mA	1.4 V			0.4	V			
		I _{OL} = 8 mA	1.65 V			0.45				
		I _{OL} = 9 mA	2.3 V			0.6				
I _I A or B in	puts	V _I = V _{CC} or GND	0 V to 2.7 V			±5	μА			
I _{off}		V_I or $V_O = 2.7 \text{ V}$	0 V			±10	μΑ			
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ			
C _i		V _I = V _{CC} or GND	2.5 V		2.5		pF			

⁽¹⁾ All typical values are at $T_A = 25$ °C.

SN74AUC2G32 DUAL 2-INPUT POSITIVE-OR GATE





Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = ± 0	1.2 V .1 V	۷ _{CC} = ± 0	V _{CC} = 1.5 V ± 0.1 V					V _{CC} = 2.5 V ± 0.2 V		UNIT
	(INFOT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
t _{pd}	A or B	Υ	7.5	0.7	3.3	0.6	1.9	0.5	1	1.5	0.4	1.1	ns	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
	(INFOT)	(001F01)	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.2	1.6	2.1	1	1.7	ns

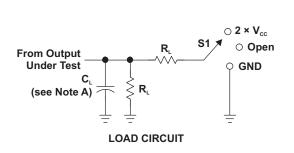
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	13	13	13	13	14	pF

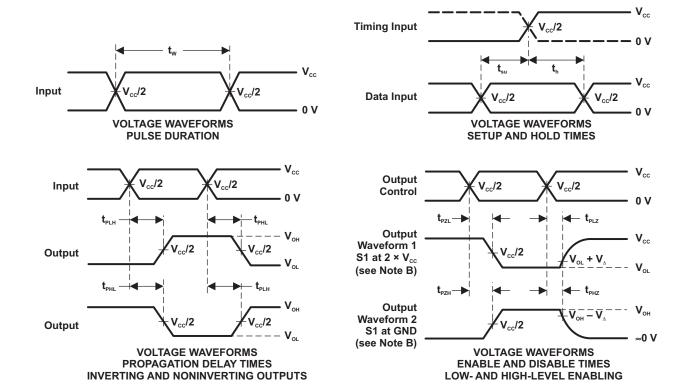


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V _{cc}
$t_{_{\mathrm{PHZ}}}/t_{_{\mathrm{PZH}}}$	GND

V _{cc}	C _L	R _L	V _Δ
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	15 pF	2 k Ω	0.15 V
$2.5~V~\pm~0.2~V$	15 pF	2 k Ω	0.15 V
1.8 V ± 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω , slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\text{\tiny PLZ}}$ and $t_{\text{\tiny PHZ}}$ are the same as $t_{\text{\tiny dis}}$.
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. $t_{Pl\,H}$ and t_{PHl} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	()	()			(-)	(4)	(5)		(-)
SN74AUC2G32DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(2XC5, U32) (R, Z)
SN74AUC2G32DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XC5, U32) (R, Z)
SN74AUC2G32DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(U32Q, U32R) UR
SN74AUC2G32DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U32Q, U32R) UR
SN74AUC2G32DCUR1G4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G32DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74AUC2G32DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G32DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G32DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74AUC2G32DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G32DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0





NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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