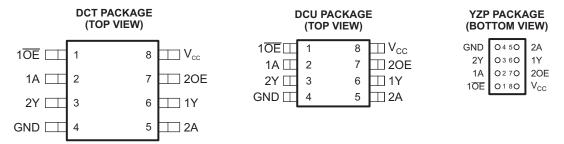
### **FEATURES**

- Available in the Texas Instruments
   NanoFree<sup>™</sup> Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t<sub>pd</sub> of 1.9 ns at 1.8 V

- Low Power Consumption, 10 μA at 1.8 V
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

### **DESCRIPTION/ORDERING INFORMATION**

This dual buffer/driver is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC2G241 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device is organized as two 1-bit line drivers with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. When  $1\overline{OE}$  is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When  $1\overline{OE}$  is high or 2OE is low, the outputs are in the high-impedance state.

NanoFree<sup>™</sup> package technology is a major breakthrough in IC packaging concepts, using the die as the package.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G241YZPR	U2_
-40°C to 85°C	SSOP - DCT	Reel of 3000	SN74AUC2G241DCTR	U41
	VSSOP - DCU	Reel of 3000	SN74AUC2G241DCUR	U2_

<sup>(1)</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

<sup>(2)</sup> DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).



## **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

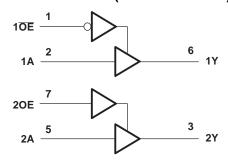
For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.

#### **FUNCTION TABLES**

INP	JTS	OUTPUT
1 <del>OE</del>	1A	1Y
L	Н	Н
L	L	L
Н	X	Z

INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	X	Z

### **LOGIC DIAGRAM (POSITIVE LOGIC)**







# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	3.6	V
VI	Input voltage range (2)	Input voltage range <sup>(2)</sup>			
Vo	Voltage range applied to any output in the h	-0.5	3.6	V	
Vo	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	amp current $V_0 < 0$		-50	mA
Io	Continuous output current			±20	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DCT package		220	
$\theta_{JA}$	Package thermal impedance (3)	Package thermal impedance (3) DCU package		227	°C/W
		YZP package		102	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

## **SN74AUC2G241 DUAL BUFFER/DRIVER** WITH 3-STATE OUTPUTS

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# Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0.8	2.7	V
		V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>		V
	High-level input voltage  Low-level input voltage  Input voltage  Output voltage  High-level output current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		$V_{CC} = 0.8 \text{ V}$		0	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 1.1 V to 1.95 V		0.35 × V <sub>CC</sub>	V
	digh-level input voltage  cow-level input voltage  Dutput voltage  digh-level output current  cow-level output current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
VI	Input voltage		0	3.6	V
\/	Output valtage	Active state	0	$V_{CC}$	V
Vo	Output voltage	3-state	0	3.6	V
		V <sub>CC</sub> = 0.8 V		-0.7	
		V <sub>CC</sub> = 1.1 V		-3	
$I_{OH}$	High-level output current	V <sub>CC</sub> = 1.4 V		-5	mA
	Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current  Input transition rise or fall rate	V <sub>CC</sub> = 1.65 V		-8	
		$V_{CC} = 2.3 \text{ V}$		-9	
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
$I_{OL}$		V <sub>CC</sub> = 1.4 V		5	mA
		V <sub>CC</sub> = 1.65 V		8	
		$V_{CC} = 2.3 \text{ V}$		9	
		V <sub>CC</sub> = 0.8 V to 1.65 V <sup>(2)</sup>		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}^{(3)}$		20	ns/V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}^{(3)}$			
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

 <sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
 (2) The data was taken at C<sub>L</sub> = 15 pF, R<sub>L</sub> = 2 kΩ (see Figure 1).
 (3) The data was taken at C<sub>L</sub> = 30 pF, R<sub>L</sub> = 500 Ω (see Figure 1).



## SN74AUC2G241 DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIO	NS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
	$I_{OH} = -100 \mu A$		0.8 V to 2.7 V	$V_{CC} - 0.1$				
V <sub>OH</sub> V <sub>OL</sub> I <sub>I</sub> All inputs I <sub>off</sub> I <sub>OZ</sub> I <sub>CC</sub>	$I_{OH} = -0.7 \text{ mA}$	0.8 V		0.55		V		
	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8					
VOH	$I_{OH} = -5 \text{ mA}$		1.4 V	1			V	
	$I_{OH} = -8 \text{ mA}$		1.65 V	1.2				
	$I_{OH} = -9 \text{ mA}$		2.3 V	1.8				
	$I_{OL} = 100 \mu A$		0.8 V to 2.7 V			0.2		
	$I_{OL} = 0.7 \text{ mA}$		0.8 V		0.25			
V <sub>OL</sub>	$I_{OL} = 3 \text{ mA}$	1.1 V			0.3	- V I		
	$I_{OL} = 5 \text{ mA}$	1.4 V			0.4			
	$I_{OL} = 8 \text{ mA}$		1.65 V			0.45		
	I <sub>OL</sub> = 9 mA		2.3 V			0.6		
I <sub>I</sub> All inputs	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	μΑ	
I <sub>off</sub>	$V_I$ or $V_O = 2.7 V$		0			±10	μΑ	
l <sub>OZ</sub>	$V_O = V_{CC}$ or GND		2.7 V			±10	μΑ	
I <sub>cc</sub>	$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	0.8 V to 2.7 V			10	μΑ	
C <sub>I</sub>	$V_I = V_{CC}$ or GND		2.5 V		2.5		pF	
C <sub>o</sub>	$V_O = V_{CC}$ or GND		2.5 V		5.5		pF	

<sup>(1)</sup> All typical values are at  $T_A = 25$ °C.

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L$  = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = ± 0.		V <sub>CC</sub> = ± 0.			<sub>C</sub> = 1.8 : 0.15 \		V <sub>CC</sub> = ± 0.		UNIT
(INPUT)		(001701)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	5.1	1	3.5	8.0	2.3	0.7	1.2	1.9	0.6	1.4	ns
t <sub>en</sub>	OE or OE	Υ	5.9	1.2	4.2	1	2.7	0.9	1.3	2	0.8	1.6	ns
t <sub>dis</sub>	OE or OE	Y	6.2	2.2	4.8	2.5	4.4	1	2.9	4.2	1.6	3.3	ns

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>C</sub>	<sub>C</sub> = 1.8 \ 0.15 V	٧	V <sub>CC</sub> = : ± 0.2	2.5 V 2 V	UNIT
	(INFOT)	(001F01)	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Υ	0.9	1.6	2.5	0.8	1.8	ns
t <sub>en</sub>	OE or OE	Υ	1.1	1.7	2.8	1	2	ns
t <sub>dis</sub>	OE or OE	Y	1.9	2.3	3.6	0.9	2.1	ns

# SN74AUC2G241 DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES535C-DECEMBER 2003-REVISED JANUARY 2007



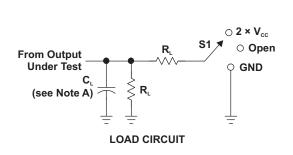
## **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 0.8 V TYP	V <sub>CC</sub> = 1.2 V TYP	V <sub>CC</sub> = 1.5 V TYP	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	UNIT
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	16	16	16	17	18	pF

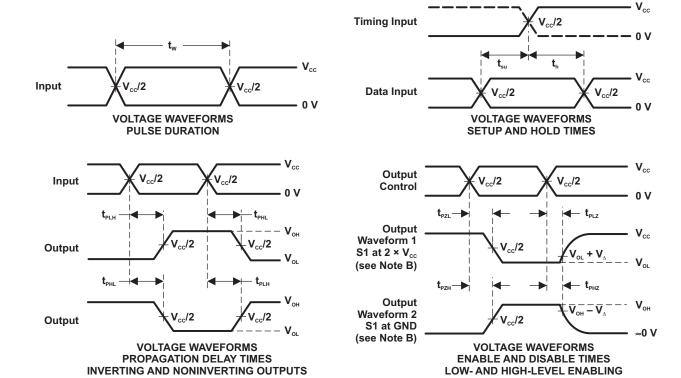


### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
$t_{PLZ}/t_{PZL}$	2 × V <sub>cc</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>cc</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V ± 0.15 V	15 pF	<b>2 k</b> Ω	0.15 V
$2.5~V~\pm~0.2~V$	15 pF	<b>2 k</b> Ω	0.15 V
1.8 V ± 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o$  = 50  $\Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\text{\tiny PLZ}}$  and  $t_{\text{\tiny PHZ}}$  are the same as  $t_{\text{\tiny dis}}$ .
- F.  $t_{\mbox{\tiny PZL}}$  and  $t_{\mbox{\tiny PZH}}$  are the same as  $t_{\mbox{\tiny en}}.$
- G.  $t_{Pl\,H}$  and  $t_{PHl}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74AUC2G241DCTR	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(2XB5, U41) (R, Z)
SN74AUC2G241DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XB5, U41) (R, Z)
SN74AUC2G241DCUR	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(U41Q, U41R)
SN74AUC2G241DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U41Q, U41R)
SN74AUC2G241DCURG4.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	-	Call TI	Call TI	-40 to 85	
SN74AUC2G241YZPR	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U2N
SN74AUC2G241YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U2N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE OPTION ADDENDUM**

www.ti.com 11-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 14-May-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G241DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G241YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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#### \*All dimensions are nominal

7 III danierie dre Herrinia										
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
SN74AUC2G241DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0			
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0			
SN74AUC2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0			
SN74AUC2G241YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0			





### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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