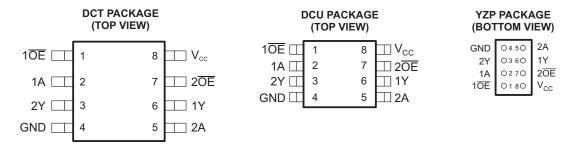


FEATURES

- Available in the Texas Instruments
 NanoFree[™] Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{nd} of 1.8 ns at 1.8 V

- Low Power Consumption, 10 μA at 1.8 V
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual bus buffer gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC2G125 features dual line drivers with 3-state outputs. The outputs are disabled when the associated output-enable (\overline{OE}) input is high.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
1000 1 000	NanoFree [™] – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G125YZPR	UM_
–40°C to 85°C	SSOP - DCT	Reel of 3000	SN74AUC2G125DCTR	U25
	VSSOP - DCU	Reel of 3000	SN74AUC2G125DCUR	U25_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).



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NanoFree is a trademark of Texas Instruments.



DESCRIPTION/ORDERING INFORMATION (CONTINUED)

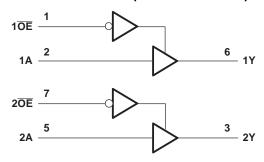
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.

FUNCTION TABLE (EACH BUFFER)

INPU	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)





SN74AUC2G125 DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range (2)		-0.5	3.6	V
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state (2)	-0.5	3.6	V
Vo	Output voltage range (2)		-0.5	V _{CC} + 0.5	V
I_{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (3)	DCU package		227	°C/W
		YZP package		102	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		V _{CC} = 0.8 V		0	
V_{IL}	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{\text{CC}}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
V_{I}	Input voltage		0	3.6	V
Vo	Output voltage	Active state	0	V_{CC}	V
۷O	Output voltage	3-state	0	3.6	V
		$V_{CC} = 0.8 \text{ V}$		-0.7	
		V _{CC} = 1.1 V		-3	
I_{OH}	High-level output current	V _{CC} = 1.4 V		- 5	mA
		V _{CC} = 1.65 V		8–	
		$V_{CC} = 2.3 \text{ V}$		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
I_{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		$V_{CC} = 2.3 \text{ V}$		9	
		$V_{CC} = 0.8 \text{ V to } 1.65 \text{ V}^{(2)}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}^{(3)}$		20	ns/V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}^{(3)}$		15	
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ The data was taken at $C_L = 15$ pF, $R_L = 2$ k Ω (see Figure 1). (3) The data was taken at $C_L = 30$ pF, $R_L = 500$ Ω (see Figure 1).

SCES532D-DECEMBER 2003-REVISED AUGUST 2007



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
	$I_{OH} = -100 \mu A$	0.8 V to 2.7 V	V _{CC} - 0.1			
	$I_{OH} = -0.7 \text{ mA}$	0.8 V		0.55		
V	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8			V
V _{OH}	$I_{OH} = -5 \text{ mA}$	1.4 V	1			V
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8			
	$I_{OL} = 100 \mu A$	0.8 V to 2.7 V			0.2	
	$I_{OL} = 0.7 \text{ mA}$	0.8 V		0.25		
V	$I_{OL} = 3 \text{ mA}$	1.1 V			0.3	V
V _{OL}	I _{OL} = 5 mA	1.4 V			0.4	V
	$I_{OL} = 8 \text{ mA}$	1.65 V			0.45	
	I _{OL} = 9 mA	2.3 V			0.6	
I _I A or \overline{OE} inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μΑ
I _{off}	V_I or $V_O = 2.7 \text{ V}$	0			±10	μΑ
I _{OZ}	$V_O = V_{CC}$ or GND	2.7 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ
C _i	V _I = V _{CC} or GND	2.5 V		2.5		pF
C _o	$V_O = V_{CC}$ or GND	2.5 V		5.5		pF

⁽¹⁾ All typical values are at $T_A = 25^{\circ}C$.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

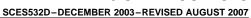
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = ± 0.	1.2 V 1 V	V _{CC} = ± 0.	1.5 V 1 V		_C = 1.8 0.15 \		V _{CC} = ± 0.		UNIT
	(INFOT)	(0011-01)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	Α	Υ	5.1	1	3.6	0.7	2.3	0.6	1	1.8	0.5	1.3	ns
t _{en}	ŌĒ	Υ	5.9	1.1	4.1	1	2.6	0.9	1.3	2	0.8	1.5	ns
t _{dis}	ŌĒ	Y	6.6	2	4.8	1.5	3.5	1.8	2.6	3.7	1.4	2.9	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C	_C = 1.8 \ : 0.15 V	/	V _{CC} = : ± 0.2	2.5 V 2 V	UNIT
	(INFOT)	(001701)	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Υ	0.8	1.6	2.6	0.7	1.8	ns
t _{en}	ŌĒ	Υ	1.1	1.7	2.9	0.9	2.2	ns
t _{dis}	ŌĒ	Υ	1.7	2.3	3.6	0.8	2	ns







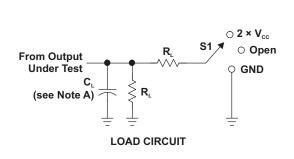
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	16	16	16	17	18	pF

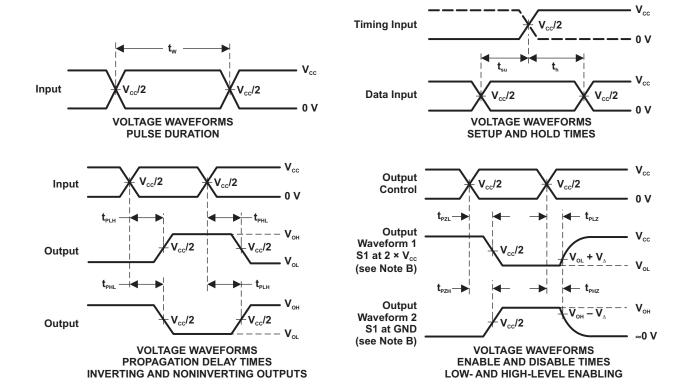


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V _{cc}
t _{PHZ} /t _{PZH}	GND

V _{cc}	C _∟	R _L	V _Δ
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V ± 0.1 V	15 pF	2 k Ω	0.1 V
$1.5 \ V \pm 0.1 \ V$	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	15 pF	2 k Ω	0.15 V
$2.5~V~\pm~0.2~V$	15 pF	2 k Ω	0.15 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	30 pF	1 k Ω	0.15 V
$2.5~\textrm{V}~\pm~0.2~\textrm{V}$	30 pF	500 Ω	0.15 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω , slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\text{\tiny PLZ}}$ and $t_{\text{\tiny PHZ}}$ are the same as $t_{\text{\tiny dis}}$.
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. $t_{Pl\,H}$ and t_{PHl} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74AUC2G125DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(2X85, U25) (R, Z)
SN74AUC2G125DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2X85, U25) (R, Z)
SN74AUC2G125DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(U25Q, U25R)
SN74AUC2G125DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U25Q, U25R)
SN74AUC2G125YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UMN
SN74AUC2G125YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UMN

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 8-Oct-2024

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G125DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74AUC2G125DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G125DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G125YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

www.ti.com 8-Oct-2024



*All dimensions are nominal

7 and an order of the final and the final an									
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)		
SN74AUC2G125DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0		
SN74AUC2G125DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0		
SN74AUC2G125DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0		
SN74AUC2G125YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0		





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





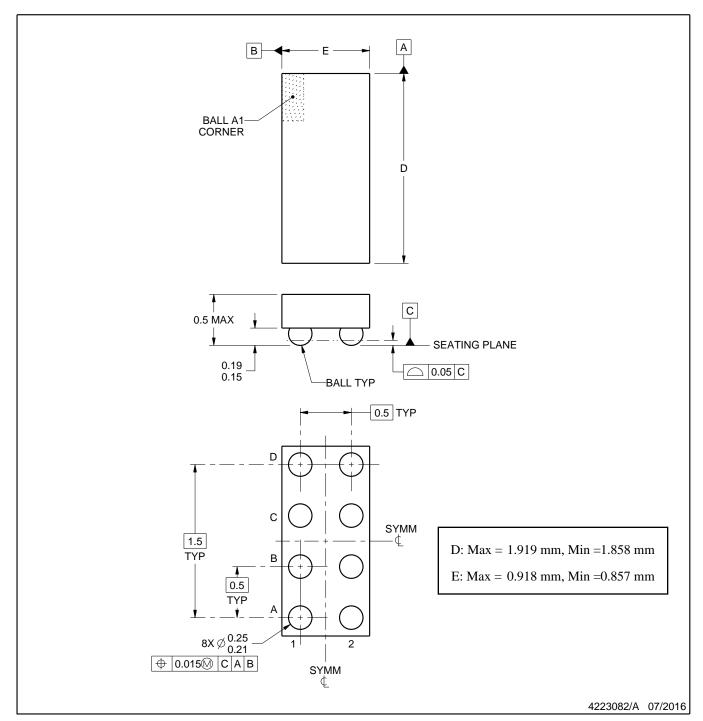
NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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