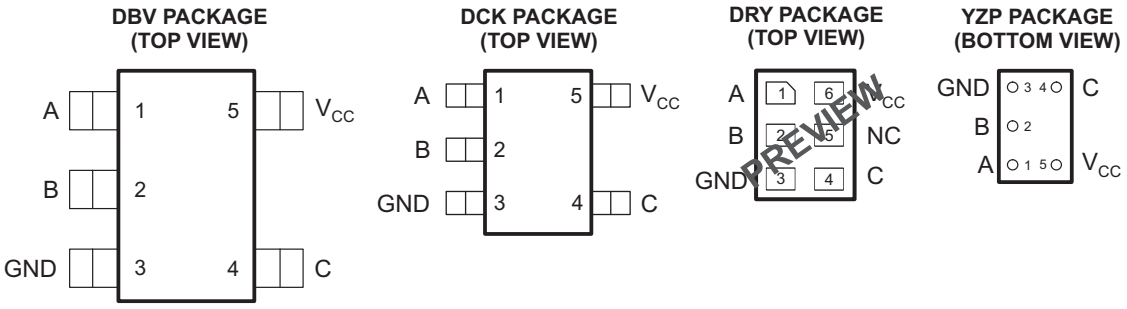
# SINGLE BILATERAL ANALOG SWITCH

## FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Wide $V_{CC}$ Range of 0.8 V to 2.7 V**
- **Sub-1-V Operable**
- **Low Power Consumption, 10-μA Max $I_{CC}$**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed – Max 0.2 ns ($V_{CC}$ = 1.8 V, $C_L$ = 15 pF)**
- **Low On-State Impedance – Typically 9 Ω ($V_{CC}$ = 2.3 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**




See mechanical drawings for dimensions.
NC– No internal connection

## DESCRIPTION/ORDERING INFORMATION

This single analog switch is operational at 0.8-V to 2.7-V $V_{CC}$, but is designed specifically for 1.65-V to 1.95-V $V_{CC}$ operation.

The SN74AUC1G66 can handle both analog and digital signals. The combined AC and DC signal has to be between $V_{CC}$ and GND for it to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

## ORDERING INFORMATION

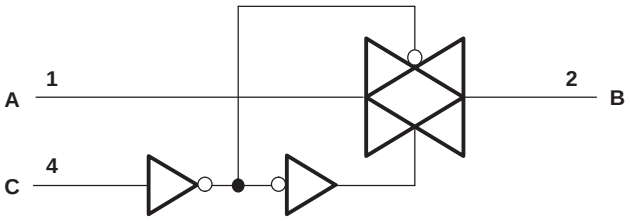
| $T_A$ | PACKAGE(1)(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING(3) |
|---|---|---|---|---|
| –40°C to 85°C | NanoFree™ WCSP (DSBGA) – YZP (Pb-free) | Reel of 3000 | SN74AUC1G66YZPR | _ _ _U6_ |
| | SON – DRY | Reel of 5000 | SN74AUC1G66DRYR | PREVIEW |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74AUC1G66DBVR | U66_ |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AUC1G66DCKR | U6_ |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DBV/DCK/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

## FUNCTION TABLE

| CONTROL INPUT (C) | SWITCH |
|---|---|
| L | OFF |
| H | ON |

## LOGIC DIAGRAM (POSITIVE LOGIC)




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 3.6 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 3.6 | V |
| $V_{I/O}$ | Switch I/O voltage range(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Control input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{IOK}$ | I/O port diode current | $V_{I/O}$ < 0 or $V_{I/O}$ > $V_{CC}$ | | ±50 | mA |
| $I_T$ | On-state switch current | $V_{I/O}$ = 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DBV package | | 206 | °C/W |
| | | DCK package | | 252 | |
| | | DRY package | | 234 | |
| | | YZP package | | 123 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 2.7 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0.65 × $V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| $V_{I/O}$ | I/O port voltage | | 0 | $V_{CC}$ | V |
| $V_I$ | Control input voltage | | 0 | 3.6 | V |
| Δt/Δv | Input transition rise or fall rate | | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $r_{on}$ | On-state switch resistance | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$ (see Figure 1) | $I_S$ = 4 mA | 1.65 V | | 10 | 20 | Ω |
| | | | $I_S$ = 8 mA | 2.3 V | | 9 | 15 | |
| $r_{on(p)}$ | Peak on resistance | $V_I$ = $V_{CC}$ to GND, $V_C$ = $V_{IH}$ (see Figure 1) | $I_S$ = 4 mA | 1.65 V | | 32 | 80 | Ω |
| | | | $I_S$ = 8 mA | 2.3 V | | 15 | 20 | |
| $I_{S(off)}$ | Off-state switch leakage current | $V_I$ = $V_{CC}$ and $V_O$ = GND, or $V_I$ = GND and $V_O$ = $V_{CC}$, $V_C$ = $V_{IL}$ (see Figure 2) | | 2.7 V | | | ±1 | μA |
| | | | | | | | ±0.1(1) | |
| $I_{S(on)}$ | On-state switch leakage current | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$, $V_O$ = Open (see Figure 3) | | 2.7 V | | | ±1 | μA |
| | | | | | | | ±0.1(1) | |
| $I_I$ | Control input current | $V_I$ = $V_{CC}$ or GND | | 0 to 2.7 V | | | ±5 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 0.8 V to 2.7 V | | | 10 | μA |
| $C_{ic}$ | Control input capacitance | | | 2.5 V | | 2 | | pF |
| $C_{io(off)}$ | Switch input/output capacitance | | | 2.5 V | | 3.5 | | pF |
| $C_{io(on)}$ | Switch input/output capacitance | | | 2.5 V | | 7 | | pF |

(1) All typical values are at $T_A$ = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$(1) | A or B | B or A | 0.9 | | 0.3 | | 0.2 | | | 0.2 | | 0.1 | ns |
| $t_{en}$ | C | A or B | 4.1 | 0.5 | 2.6 | 0.5 | 1.7 | 0.5 | 0.8 | 1.1 | 0.5 | 1 | ns |
| $t_{dis}$ | C | A or B | 5 | 0.7 | 3.6 | 0.5 | 2.6 | 0.5 | 1.7 | 2.9 | 0.5 | 2.2 | ns |

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | | $V_{CC}$ = 2.5 V ± 0.2 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ (1) | A or B | B or A | | | 0.3 | | 0.3 | ns |
| $t_{en}$ | C | A or B | 0.5 | 1.4 | 2.3 | 0.8 | 1.4 | ns |
| $t_{dis}$ | C | A or B | 0.5 | 1.7 | 2.9 | 0.5 | 1.5 | ns |

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## Analog Switch Characteristics

$T_A$ = 25°C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| Frequency response[1] (switch ON) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = sine wave (see Figure 5) | 0.8 V | 60 | MHz |
| | | | | 1.1 V | 60 | |
| | | | | 1.4 V | 80 | |
| | | | | 1.65 V | 120 | |
| | | | | 2.3 V | 170 | |
| | | | $C_L$ = 5 pF, $R_L$ = 50 Ω, $f_{in}$ = sine wave (see Figure 5) | 0.8 V | >500 | |
| | | | | 1.1 V | >500 | |
| | | | | 1.4 V | >500 | |
| | | | | 1.65 V | >500 | |
| | | | | 2.3 V | >500 | |
| Crosstalk (control input to signal output) | C | A or B | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (square wave) (see Figure 6) | 0.8 V | 9 | mV |
| | | | | 1.1 V | 14 | |
| | | | | 1.4 V | 15 | |
| | | | | 1.65 V | 16 | |
| | | | | 2.3 V | 20 | |
| Feedthrough attenuation[2] (switch OFF) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (sine wave) (see Figure 7) | 0.8 V | –60 | dB |
| | | | | 1.1 V | –60 | |
| | | | | 1.4 V | –60 | |
| | | | | 1.65 V | –60 | |
| | | | | 2.3 V | –60 | |
| | | | $C_L$ = 5 pF, $R_L$ = 50 Ω, $f_{in}$ = 1 MHz (sine wave) (see Figure 7) | 0.8 V | –55 | |
| | | | | 1.1 V | –55 | |
| | | | | 1.4 V | –55 | |
| | | | | 1.65 V | –55 | |
| | | | | 2.3 V | –55 | |
| Sine-wave distortion | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kHz (sine wave) (see Figure 8) | 0.8 V | 7.5 | % |
| | | | | 1.1 V | 0.16 | |
| | | | | 1.4 V | 0.04 | |
| | | | | 1.65 V | 0.03 | |
| | | | | 2.3 V | 0.02 | |
| | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 10 kHz (sine wave) (see Figure 8) | 0.8 V | 4.2 | |
| | | | | 1.1 V | 0.2 | |
| | | | | 1.4 V | 0.03 | |
| | | | | 1.65 V | 0.02 | |
| | | | | 2.3 V | 0.02 | |

(1) Adjust $f_{in}$ voltage to obtain 0 dBm at output. Increase $f_{in}$ frequency until dB meter reads –3 dB.
(2) Adjust $f_{in}$ voltage to obtain 0 dBm at input.

## Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V | $V_{CC}$ = 1.5 V | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 3 | 3 | 3 | 3 | 3 | pF |

## PARAMETER MEASUREMENT INFORMATION

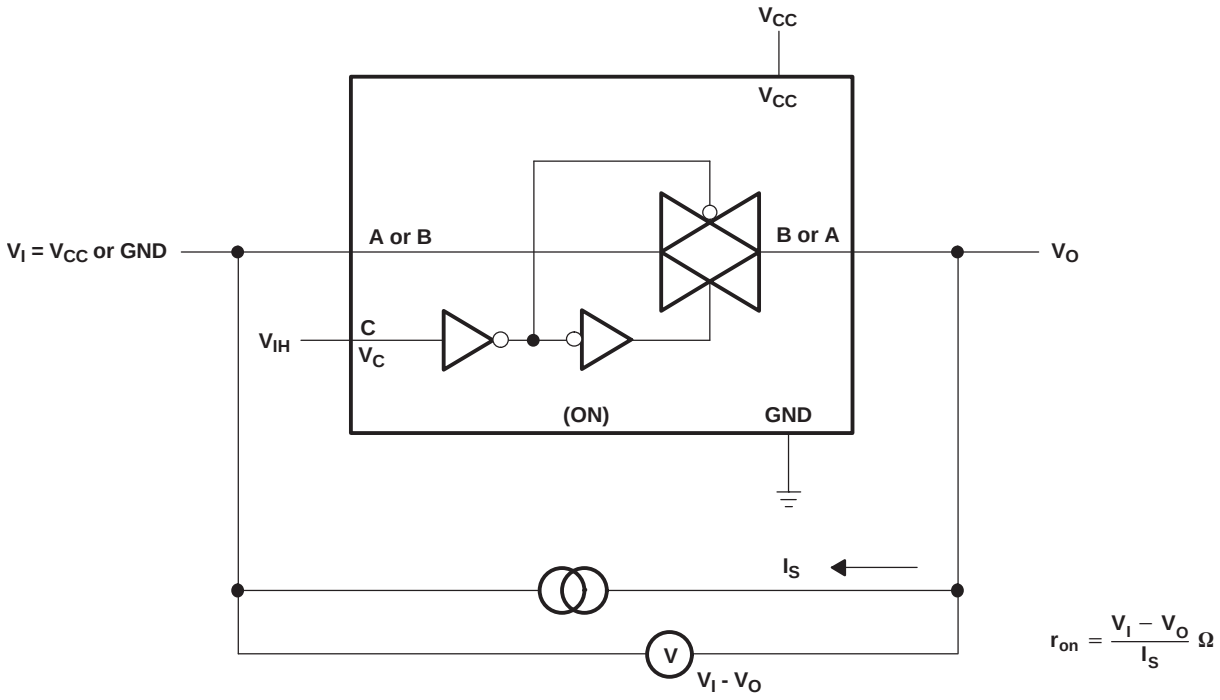



**Figure 1. On-State Resistance Test Circuit**

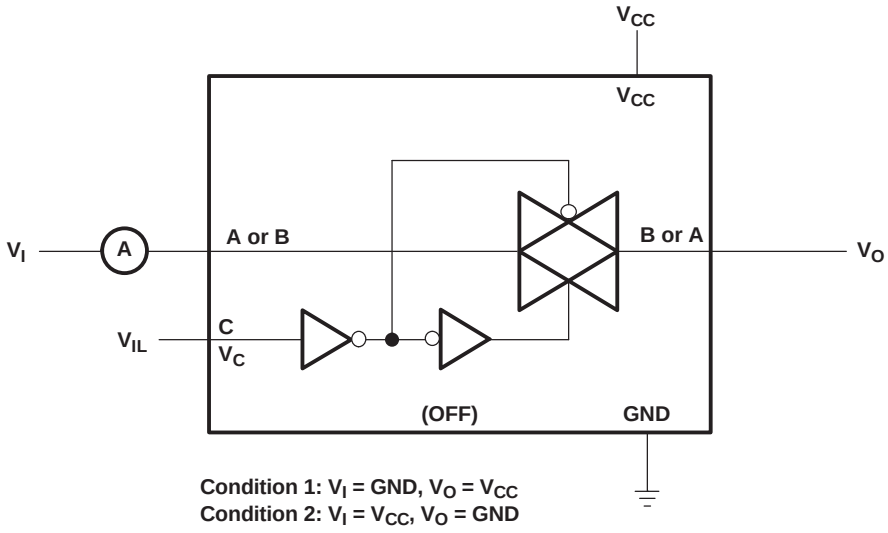



**Figure 2. Off-State Switch Leakage-Current Test Circuit**

## PARAMETER MEASUREMENT INFORMATION (Continued)

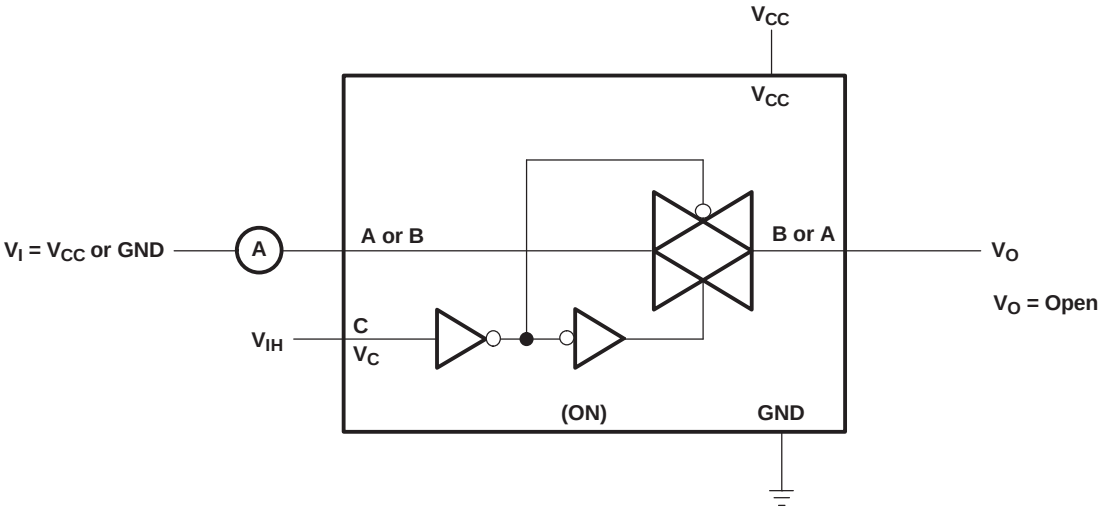
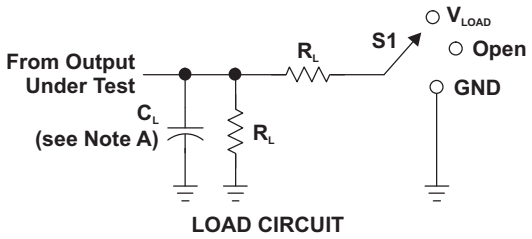



**Figure 3. On-State Leakage-Current Test Circuit**

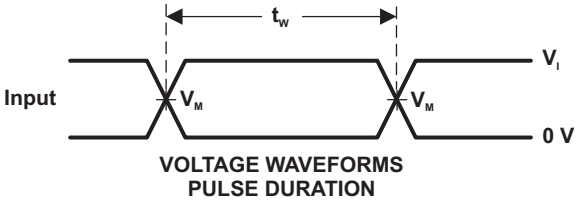
## PARAMETER MEASUREMENT INFORMATION (Continued)



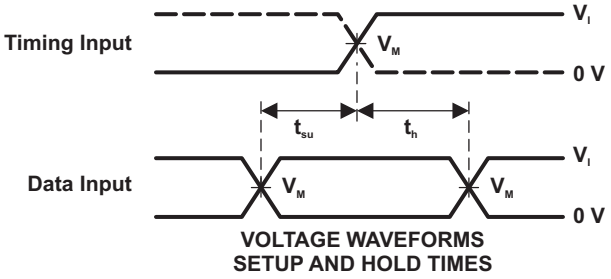

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

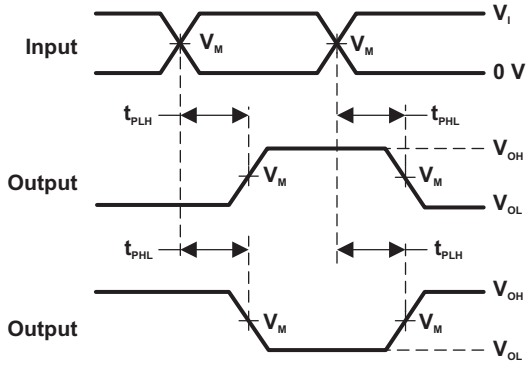
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 0.8 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 2 kΩ | 0.1 V |
| 1.2 V ± 0.1 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 2 kΩ | 0.15 V |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |



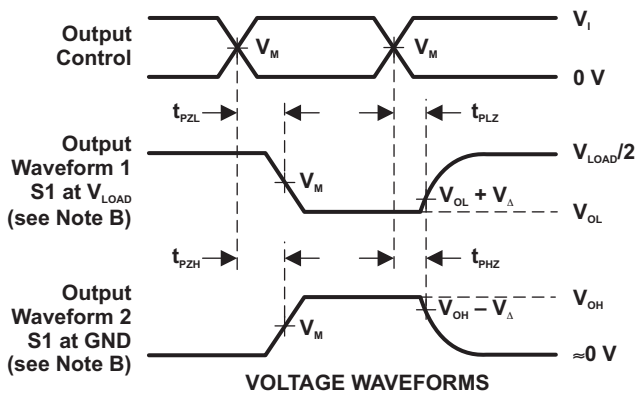

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, Slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 4. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (Continued)

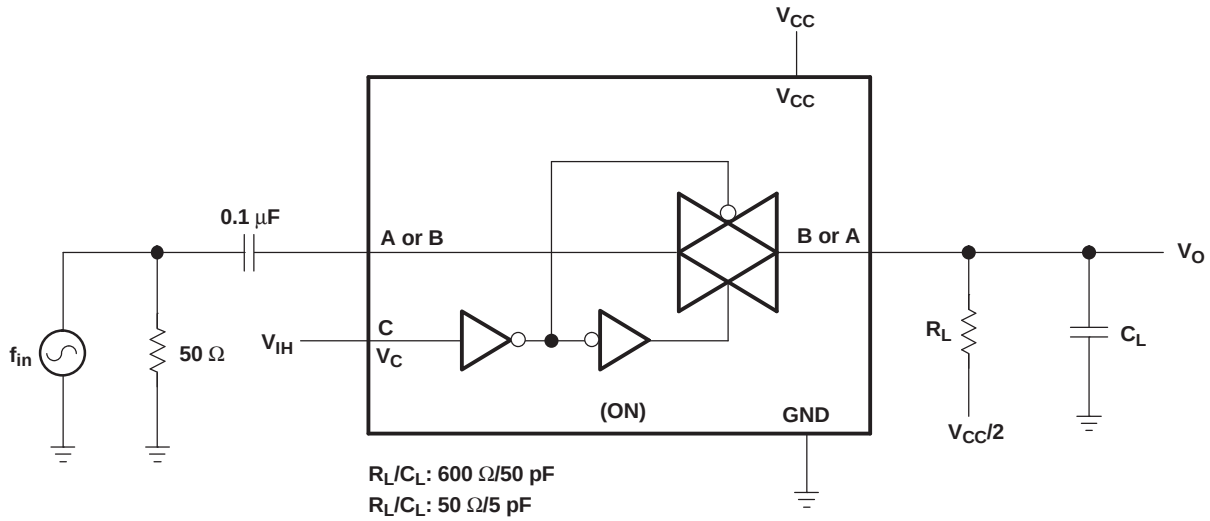



**Figure 5. Frequency Response (Switch ON)**

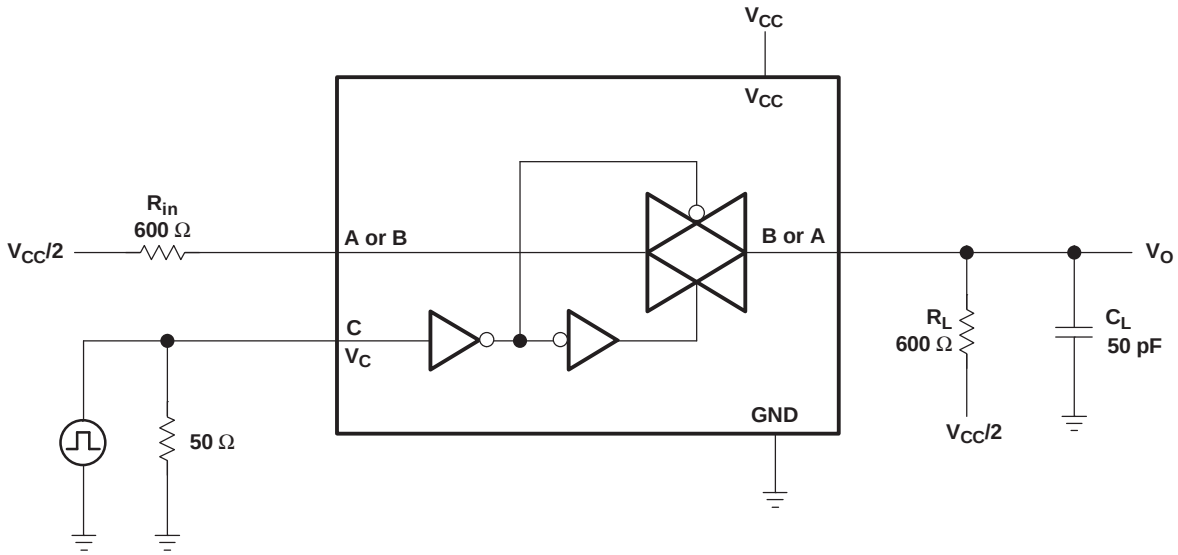



**Figure 6. Crosstalk (Control Input – Switch Output)**

## PARAMETER MEASUREMENT INFORMATION (Continued)

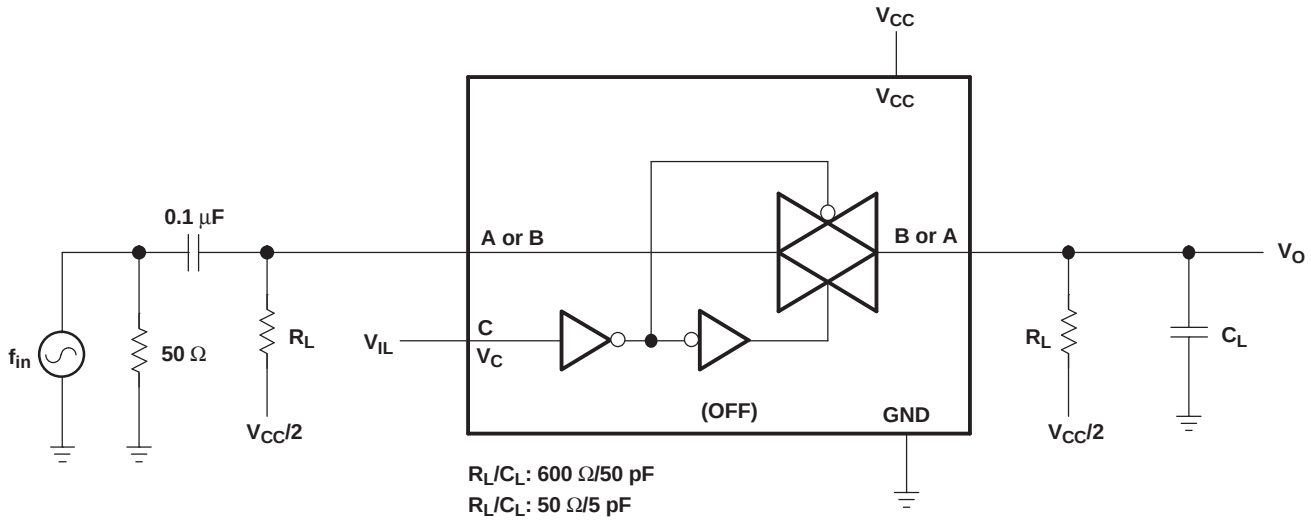



**Figure 7. Feedthrough (Switch OFF)**

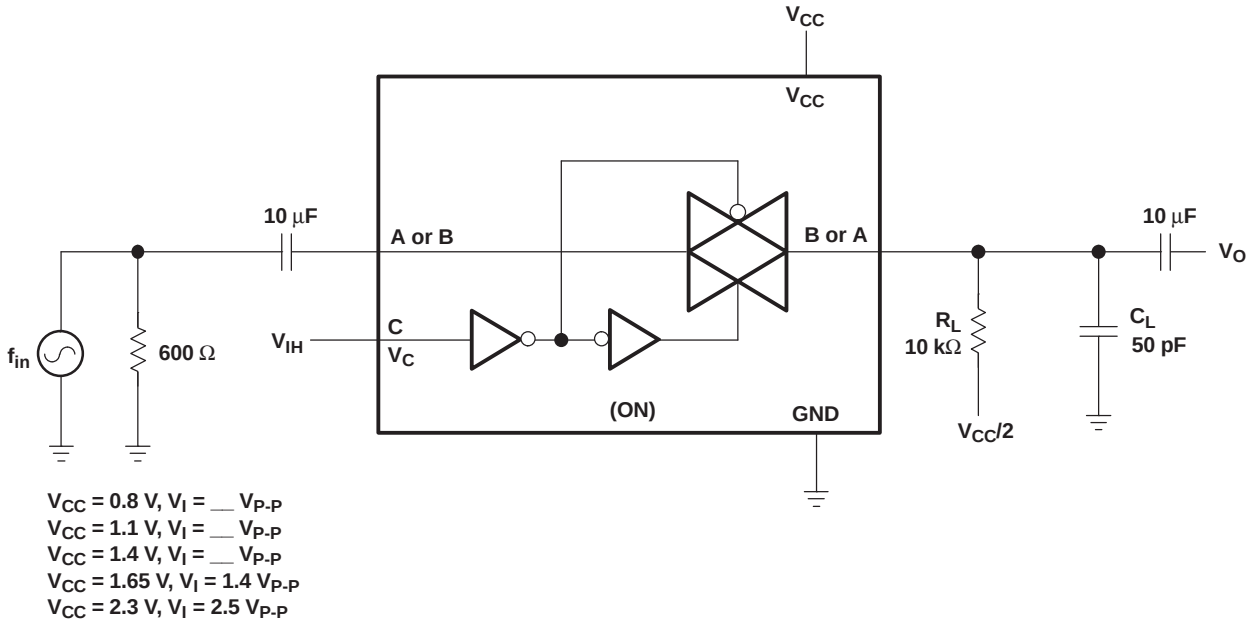



**Figure 8. Sine-Wave Distortion**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUC1G66DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (U66F, U66R) |
| SN74AUC1G66DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U66F, U66R) |
| SN74AUC1G66DBVRG4.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U66F |
| SN74AUC1G66DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U65, U6F, U6R) |
| SN74AUC1G66DCKR.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U65, U6F, U6R) |
| SN74AUC1G66YZPR | Active | Production | DSBGA (YZP) \| 5 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | U6N |
| SN74AUC1G66YZPR.B | Active | Production | DSBGA (YZP) \| 5 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | U6N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

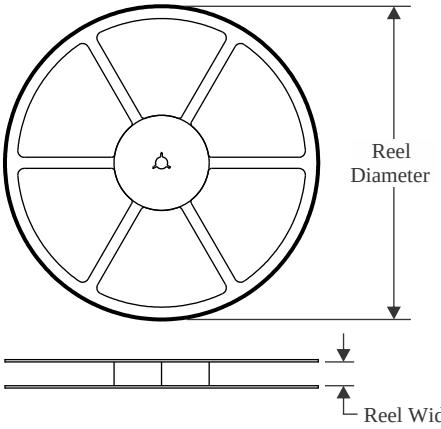
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

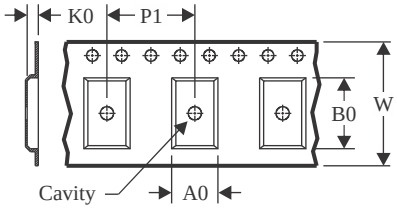
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

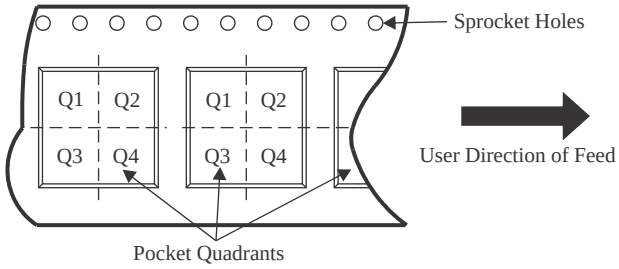



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

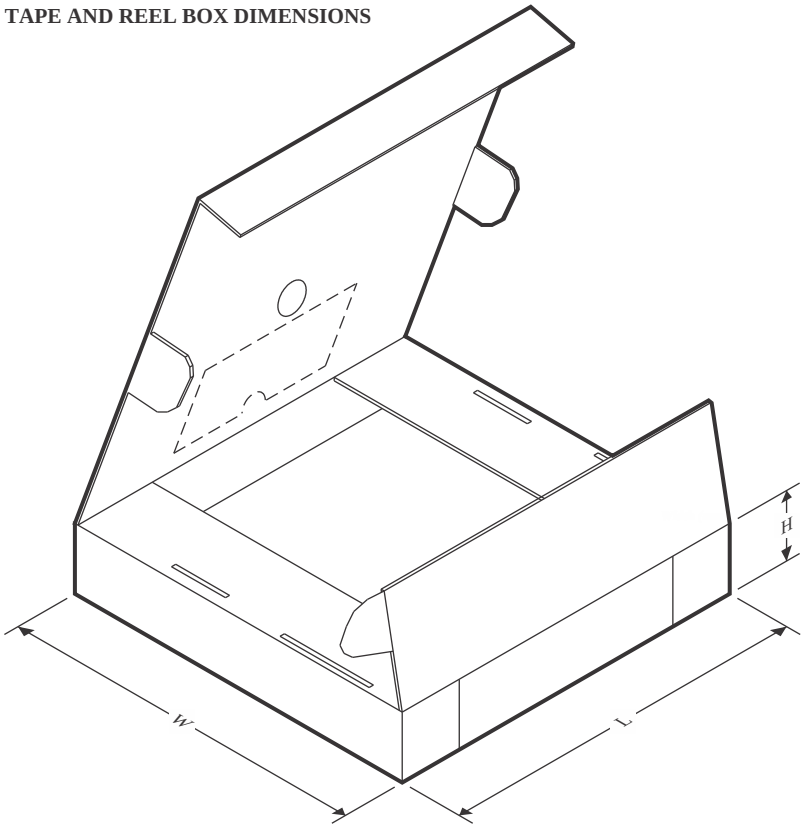
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

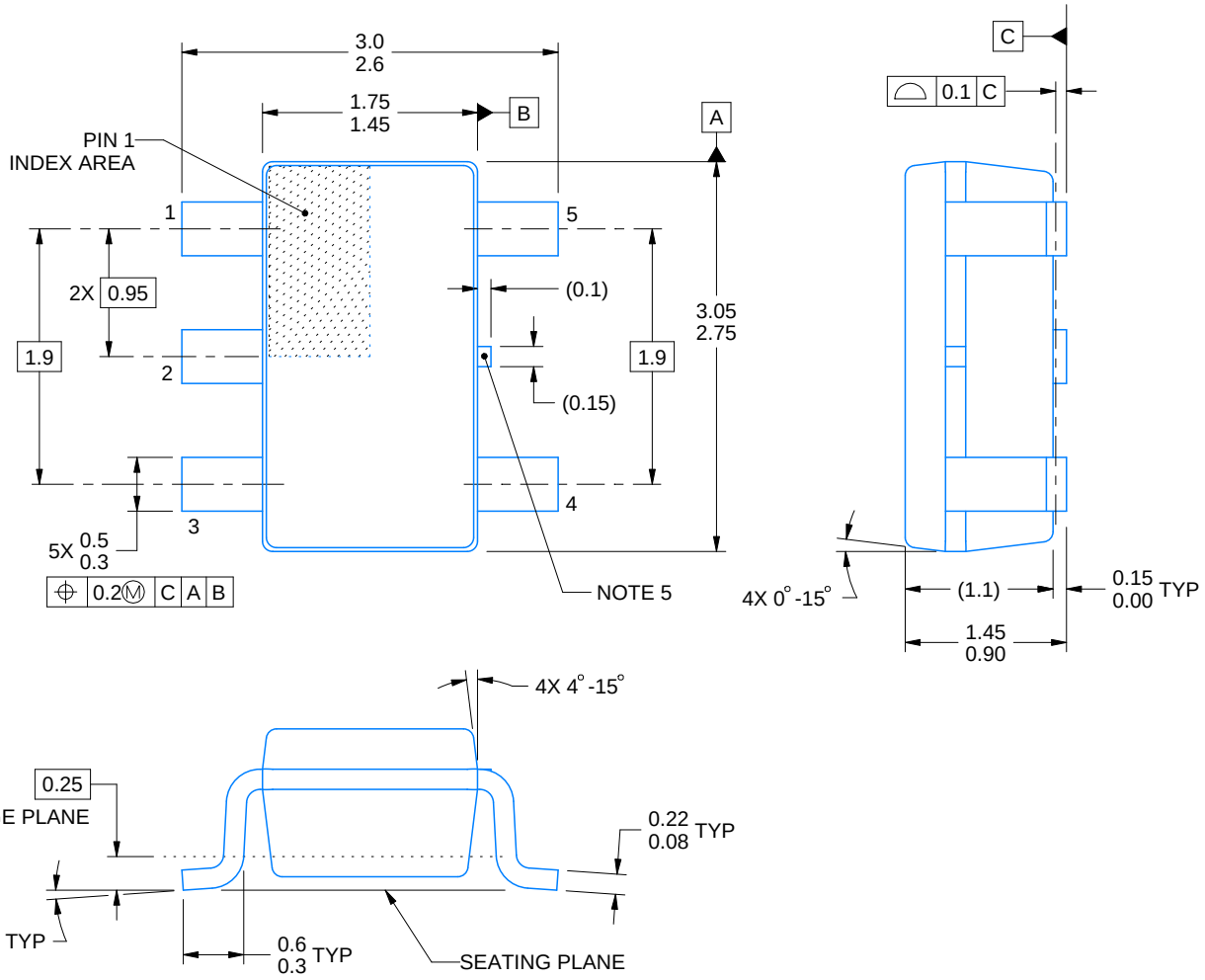
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G66YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

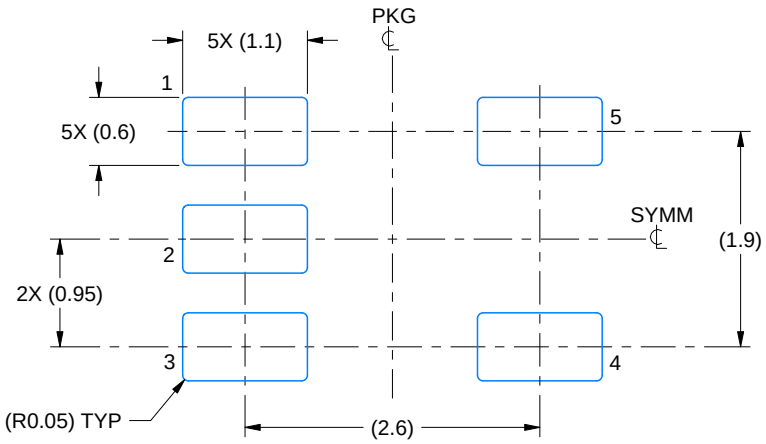
SMALL OUTLINE TRANSISTOR



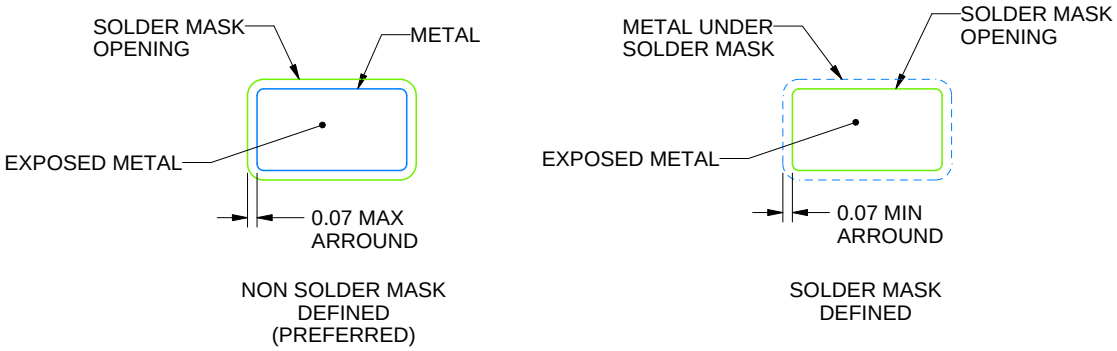

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

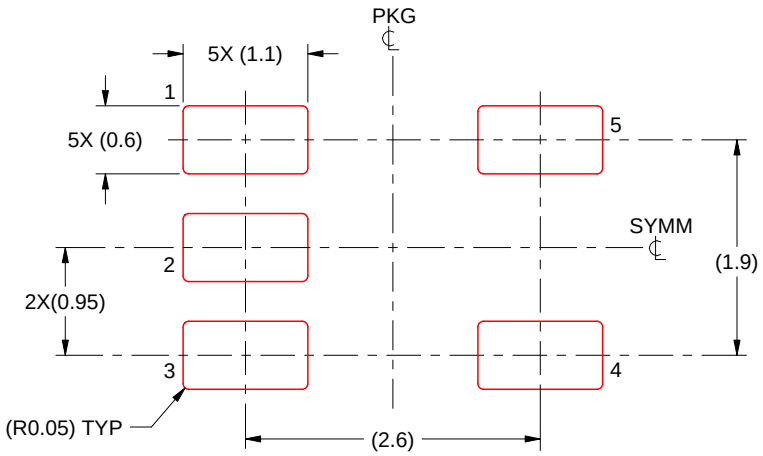



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

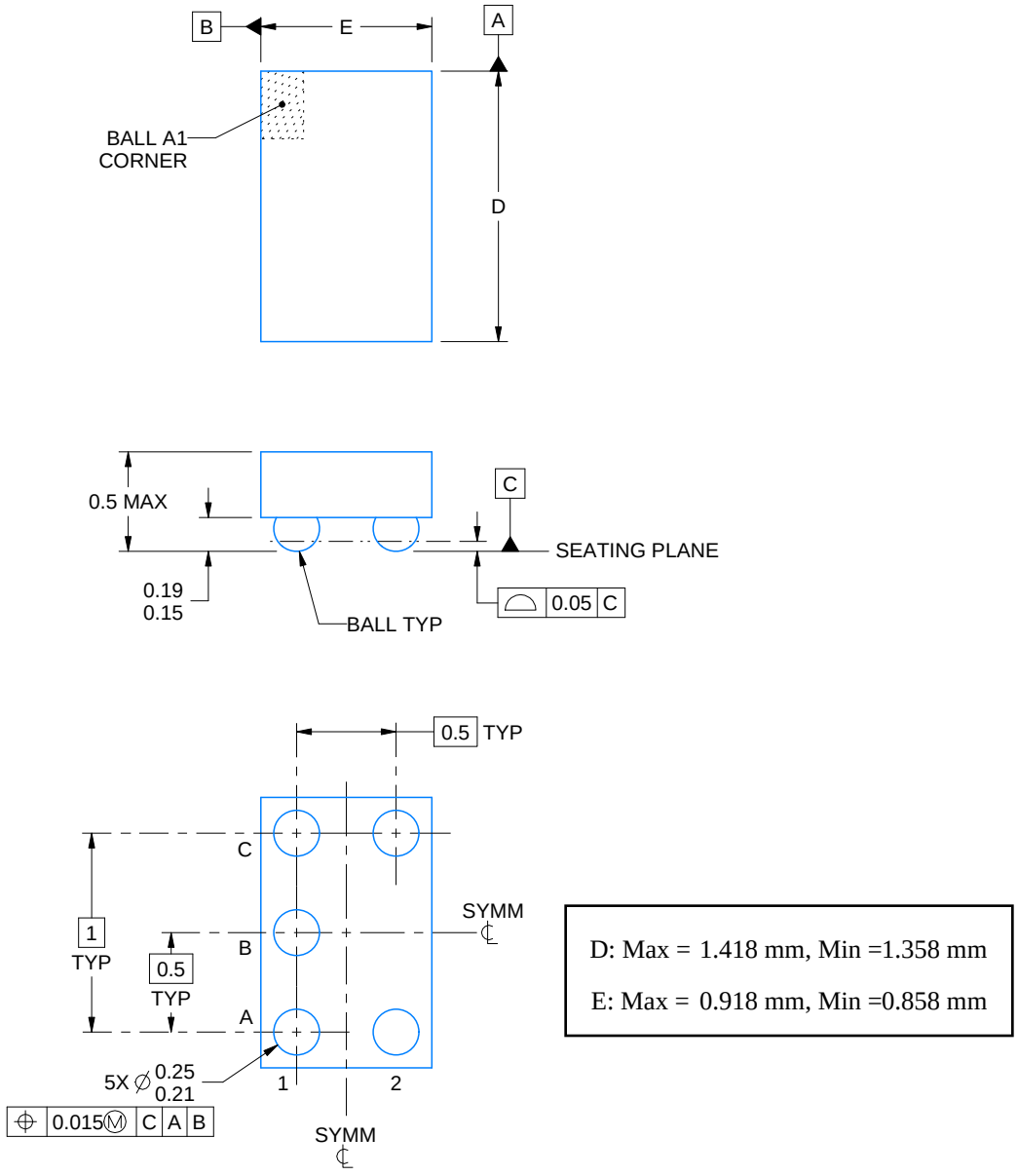
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## YZP0005

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



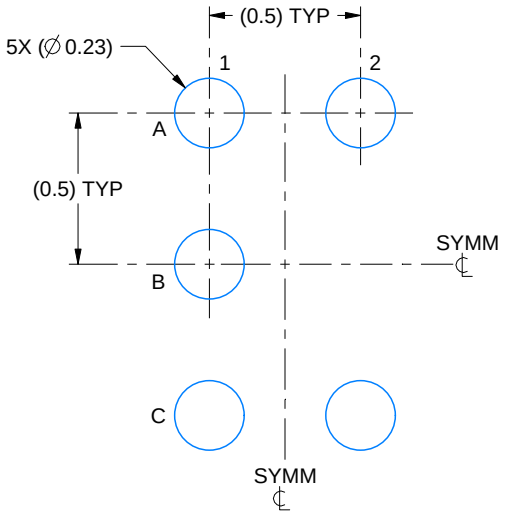

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

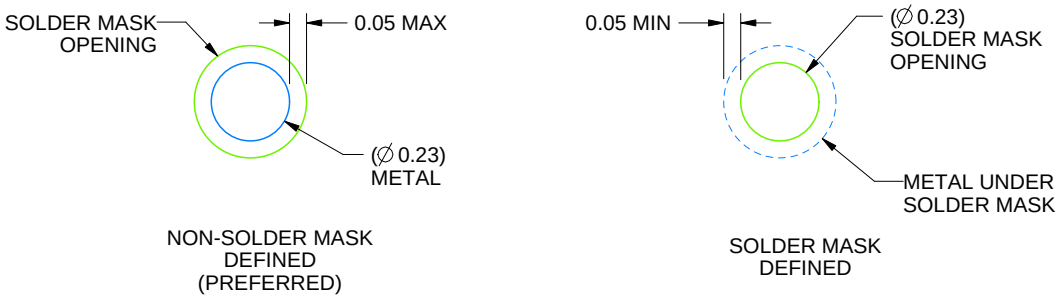
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

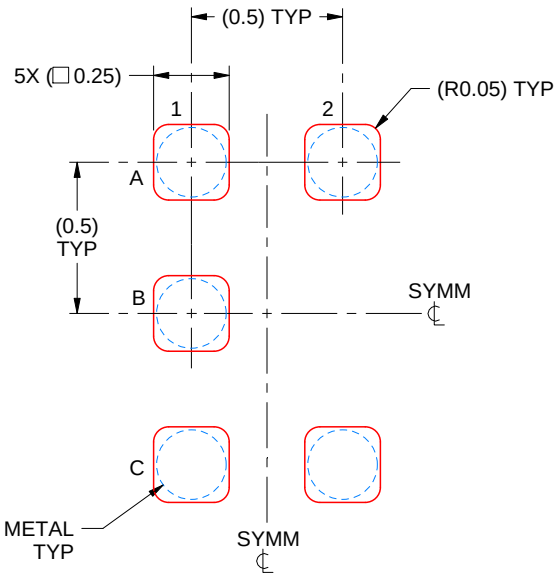



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

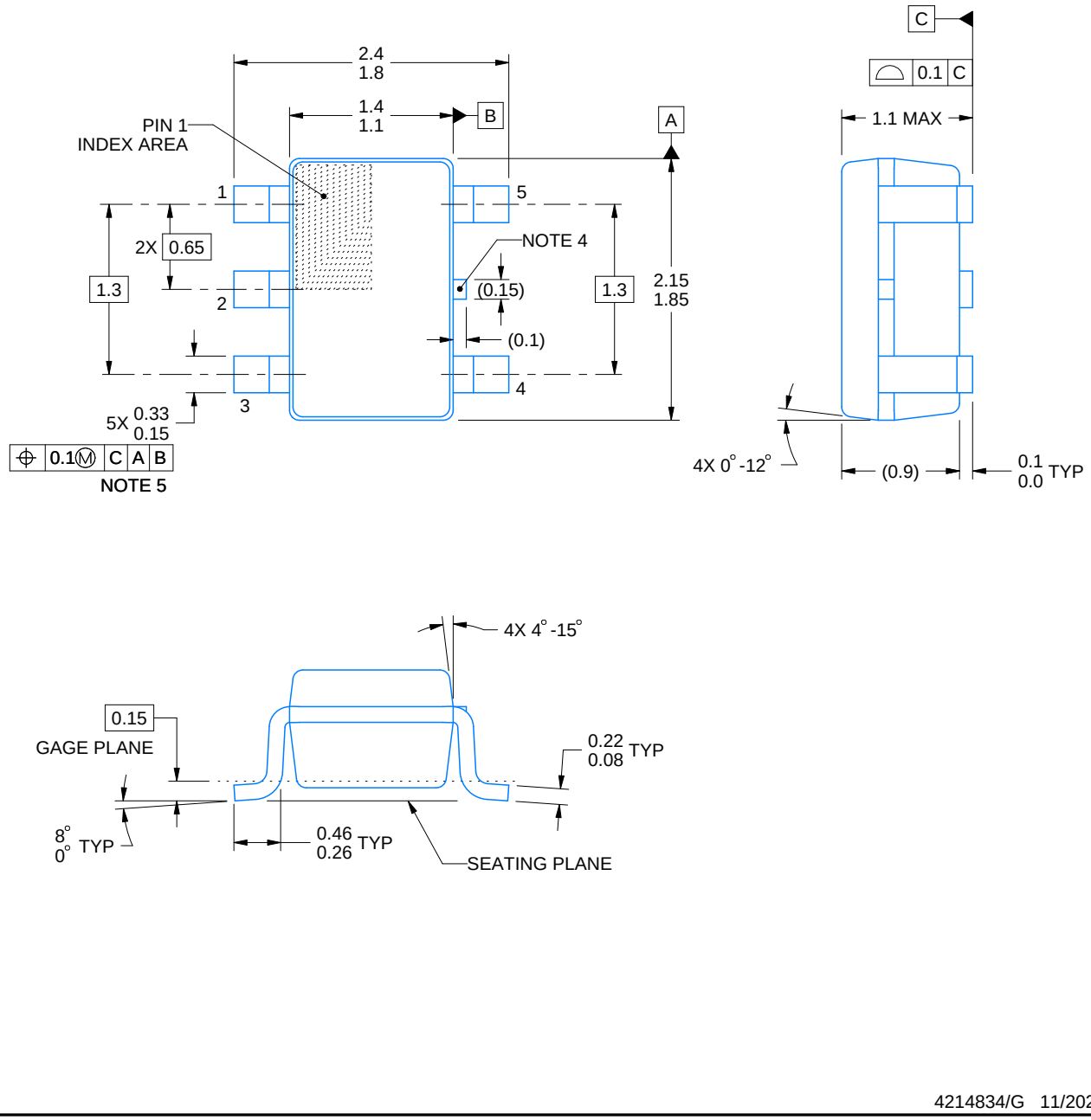
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

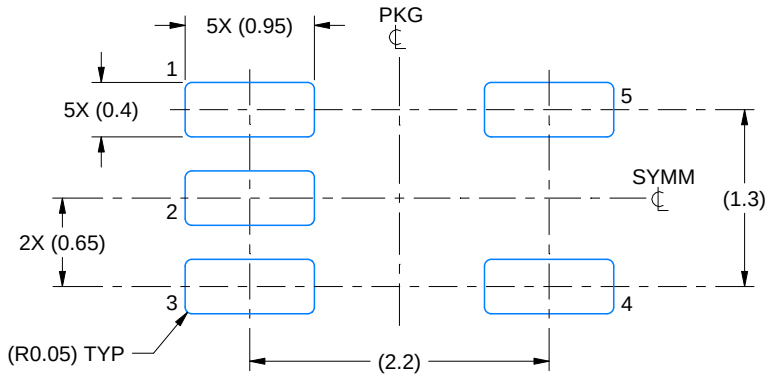
SMALL OUTLINE TRANSISTOR



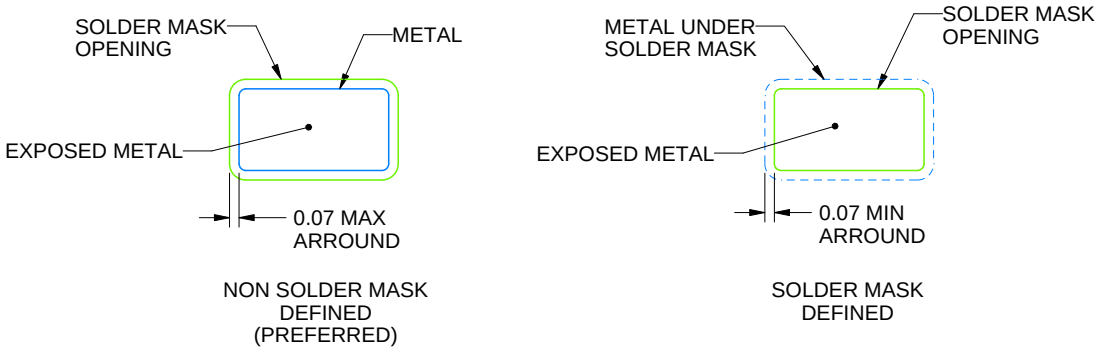

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

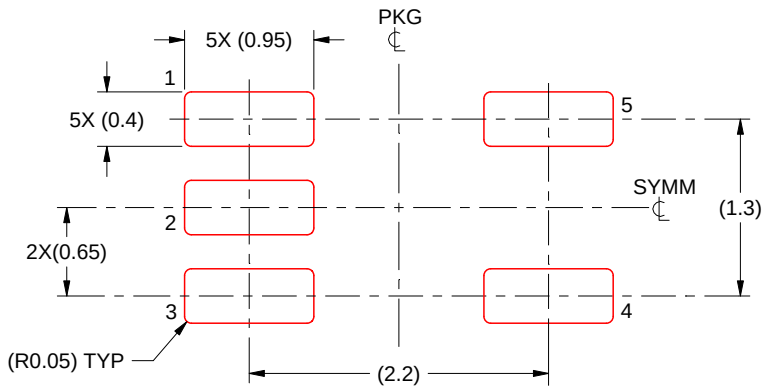



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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