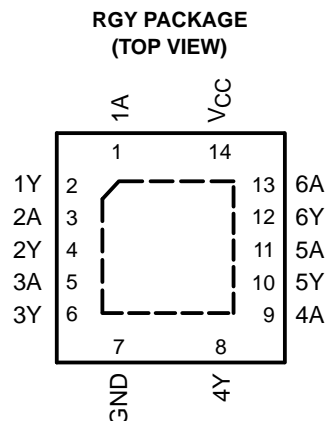


## FEATURES

- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 1.8 ns at 1.8 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



## DESCRIPTION/ORDERING INFORMATION

This hex Schmitt-trigger buffer is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC17 contains six independent buffers and performs the Boolean function  $Y = A$ . The device functions as six independent buffers, but because of Schmitt action, it may have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

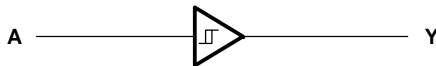
$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AUC17RGYR	MS17

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
H	H
L	L

## LOGIC DIAGRAM, EACH BUFFER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74AUC17

## HEX SCHMITT-TRIGGER BUFFER

SCES497A–OCTOBER 2003–REVISED MARCH 2005

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		–0.5	3.6	V
$V_I$	Input voltage range <sup>(2)</sup>		–0.5	3.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		–0.5	3.6	V
$V_O$	Output voltage range <sup>(2)</sup>		–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50	mA
$I_O$	Continuous output current			±20	mA
	Continuous current through $V_{CC}$ or GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>			47	°C/W
$T_{stg}$	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5.

### Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		0.8	2.7	V
$V_I$	Input voltage		0	3.6	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8$ V		–0.7	mA
		$V_{CC} = 1.1$ V		–3	
		$V_{CC} = 1.4$ V		–5	
		$V_{CC} = 1.65$ V		–8	
		$V_{CC} = 2.3$ V		–9	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8$ V		0.7	mA
		$V_{CC} = 1.1$ V		3	
		$V_{CC} = 1.4$ V		5	
		$V_{CC} = 1.65$ V		8	
		$V_{CC} = 2.3$ V		9	
$T_A$	Operating free-air temperature		–40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{T+}$ Positive-going input threshold voltage		0.8 V		0.5		V
		1.1 V	0.51		0.86	
		1.4 V	0.65		1	
		1.65 V	0.79		1.16	
		2.3 V	1.11		1.56	
$V_{T-}$ Negative-going input threshold voltage		0.8 V		0.3		V
		1.1 V	0.22		0.53	
		1.4 V	0.3		0.58	
		1.65 V	0.39		0.62	
		2.3 V	0.58		0.87	
$\Delta V_T$ Hysteresis ( $V_{T+} - V_{T-}$ )		0.8 V		0.21		V
		1.1 V	0.25		0.38	
		1.4 V	0.31		0.5	
		1.65 V	0.37		0.62	
		2.3 V	0.48		0.77	
$V_{OH}$	$I_{OH} = -100 \mu A$	0.8 V to 2.7 V	$V_{CC} - 0.1$			V
	$I_{OH} = -0.7 \text{ mA}$	0.8 V	0.55			
	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8			
	$I_{OH} = -5 \text{ mA}$	1.4 V	1			
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8			
$V_{OL}$	$I_{OL} = 100 \mu A$	0.8 V to 2.7 V	0.2			V
	$I_{OL} = 0.7 \text{ mA}$	0.8 V	0.25			
	$I_{OL} = 3 \text{ mA}$	1.1 V	0.3			
	$I_{OL} = 5 \text{ mA}$	1.4 V	0.4			
	$I_{OL} = 8 \text{ mA}$	1.65 V	0.45			
	$I_{OL} = 9 \text{ mA}$	2.3 V	0.6			
$I_I$	A inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V		$\pm 5$	$\mu A$
$I_{off}$		$V_I$ or $V_O = 2.7 \text{ V}$	0		$\pm 10$	$\mu A$
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V		10	$\mu A$
$C_i$		$V_I = V_{CC}$ or GND	2.5 V		2.5	pF

(1) All typical values are at  $T_A = 25^\circ C$ .

## Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	6.7	1.3	3.5	1	2.2	0.9	1.2	1.8	0.7	1.4	ns

## Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	1.3	1.7	2.4	1.2	1.9	ns

# SN74AUC17

## HEX SCHMITT-TRIGGER BUFFER

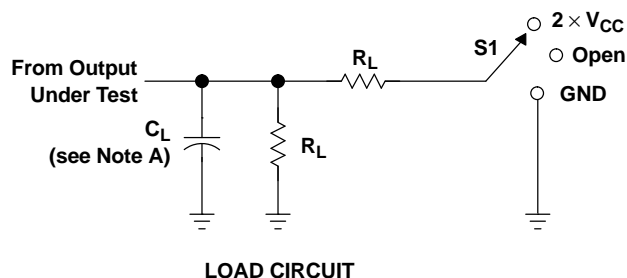
SCES497A—OCTOBER 2003—REVISED MARCH 2005

### Operating Characteristics

$T_A = 25^\circ\text{C}$

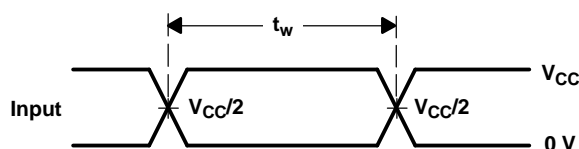
PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$f = 10\text{ MHz}$	18	19	19	20	22	pF

## PARAMETER MEASUREMENT INFORMATION

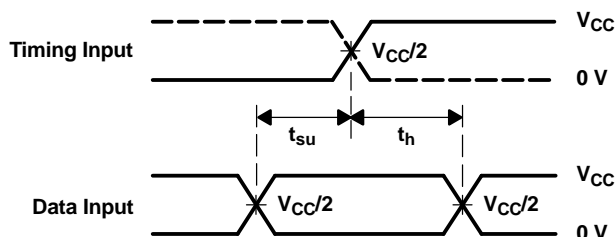


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

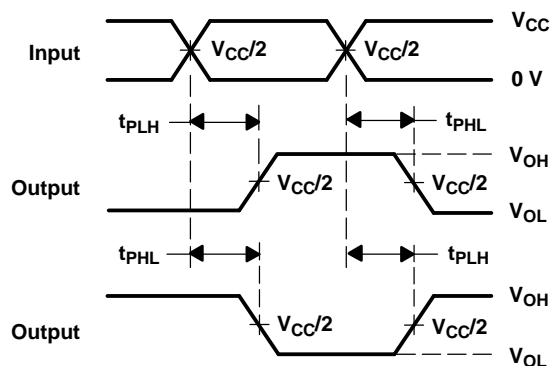
$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



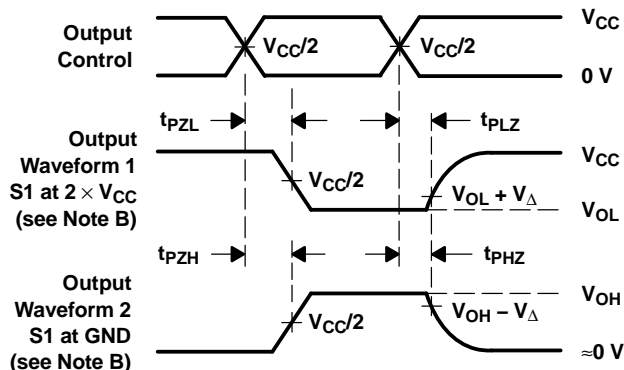
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AUC17RGYR</a>	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS17
SN74AUC17RGYR.B	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS17
SN74AUC17RGYRG4	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS17

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC17RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC17RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0



## GENERIC PACKAGE VIEW

**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

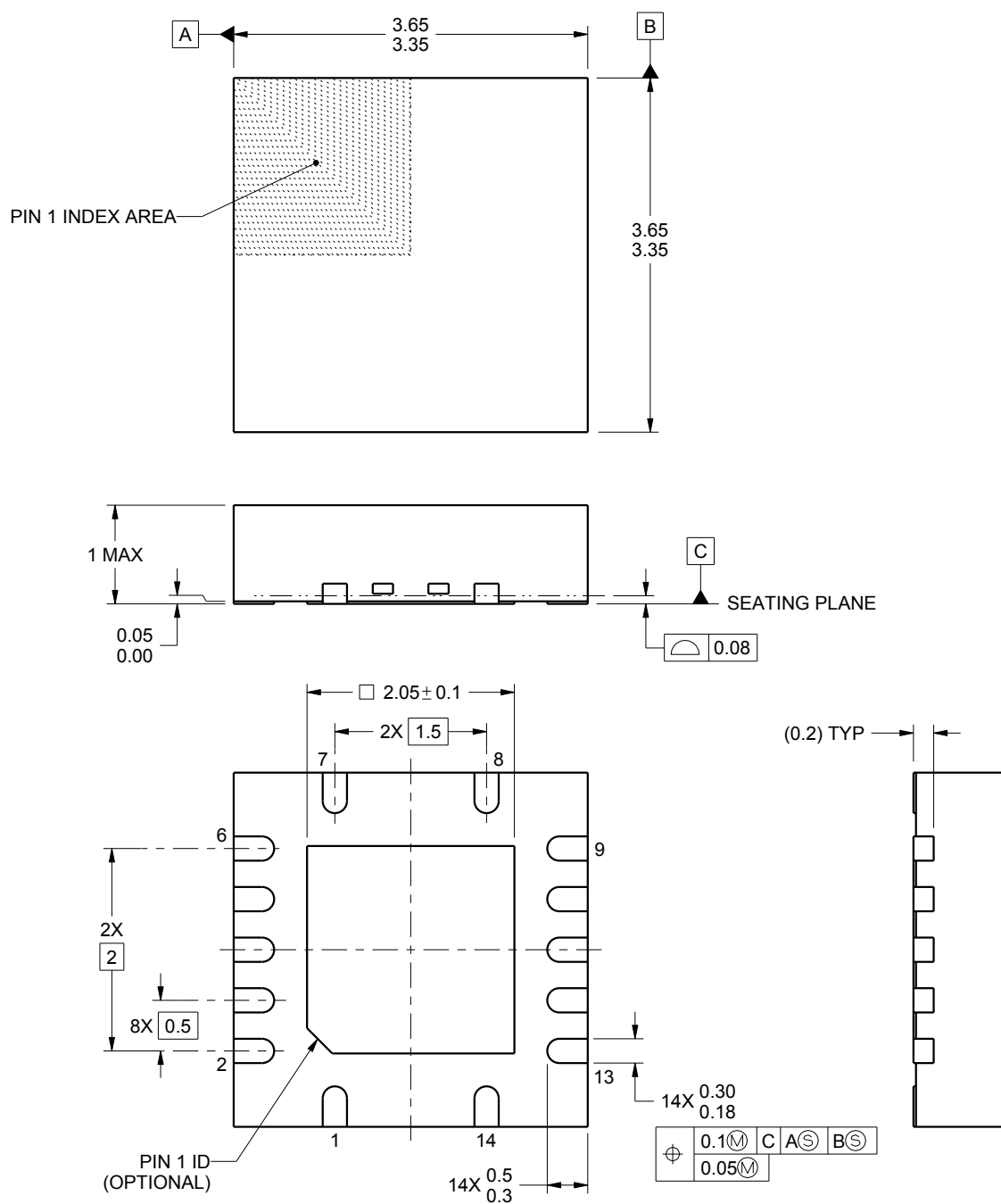


4231541/A



### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 EXPOSED PAD  
 80% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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