

SN54AS867, SN54AS869 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

- Fully Programmable With Synchronous Counting and Loading
- SN74ALS867A and 'AS867 Have Asynchronous Clear; SN74ALS869 and 'AS869 Have Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Ripple-Carry Output for n-Bit Cascading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

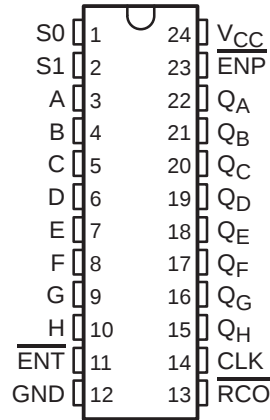
These synchronous, presettable, 8-bit up/down counters feature internal-carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable ($\overline{\text{ENP}}$, $\overline{\text{ENT}}$) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; they may be preset to any number between 0 and 255. The load-input circuitry allows parallel loading of the cascaded counters. Because loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

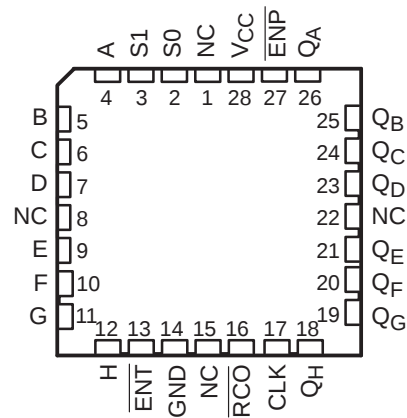
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Two count-enable ($\overline{\text{ENP}}$ and $\overline{\text{ENT}}$) inputs and a ripple-carry ($\overline{\text{RCO}}$) output are instrumental in accomplishing this function. Both $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ must be low to count. The direction of the count is determined by the levels of the select (S0, S1) inputs as shown in the function table. $\overline{\text{ENT}}$ is fed forward to enable $\overline{\text{RCO}}$. $\overline{\text{RCO}}$ thus enabled produces a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ are allowed regardless of the level of CLK. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the SN74ALS867A and 'AS867, changes at S0 and S1 that modify the operating mode have no effect on the Q outputs until clocking occurs. For the 'AS867 and 'AS869, any time $\overline{\text{ENP}}$ and/or $\overline{\text{ENT}}$ is taken high, $\overline{\text{RCO}}$ either goes or remains high. For the SN74ALS867A and SN74ALS869, any time $\overline{\text{ENT}}$ is taken high, $\overline{\text{RCO}}$ either goes or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

SN54AS867, SN54AS869 . . . JT PACKAGE
SN74ALS867A, SN74ALS869, SN74AS867,
SN74AS869 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS867, SN54AS869 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

description (continued)

The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS867A, SN74ALS869, SN74AS867, and SN74AS869 are characterized for operation from 0°C to 70°C .

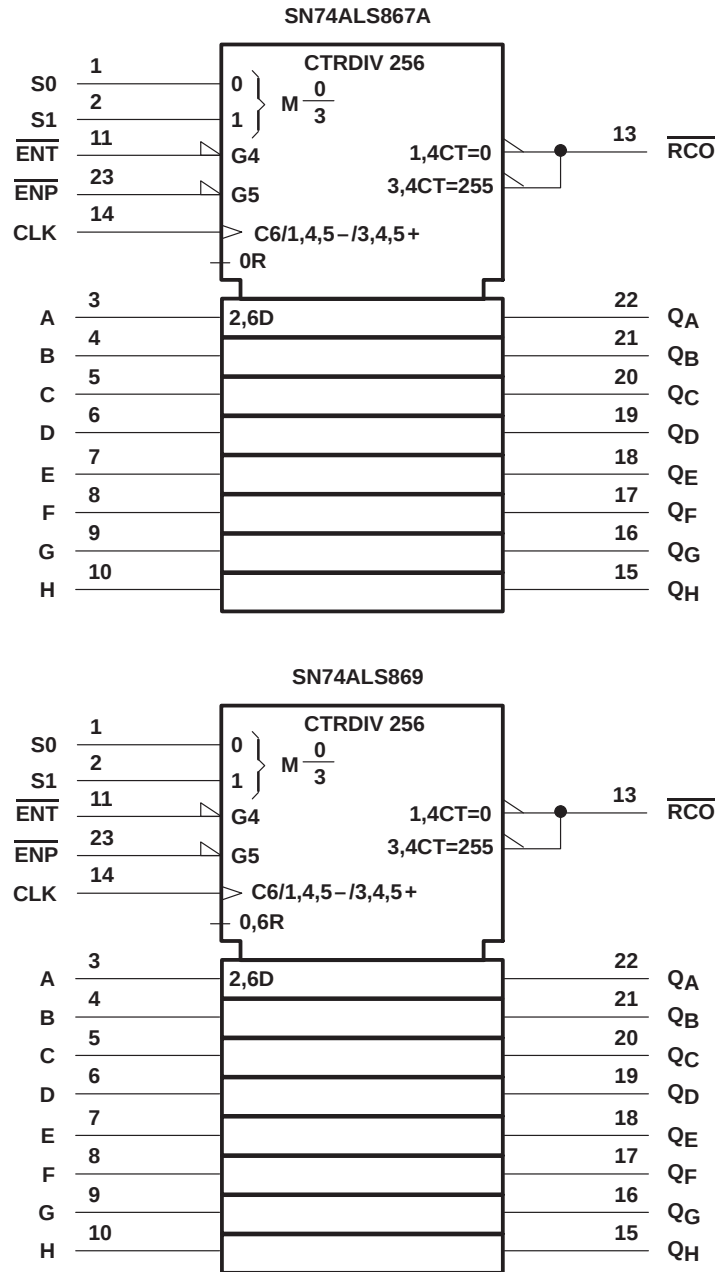
FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic symbols[†]

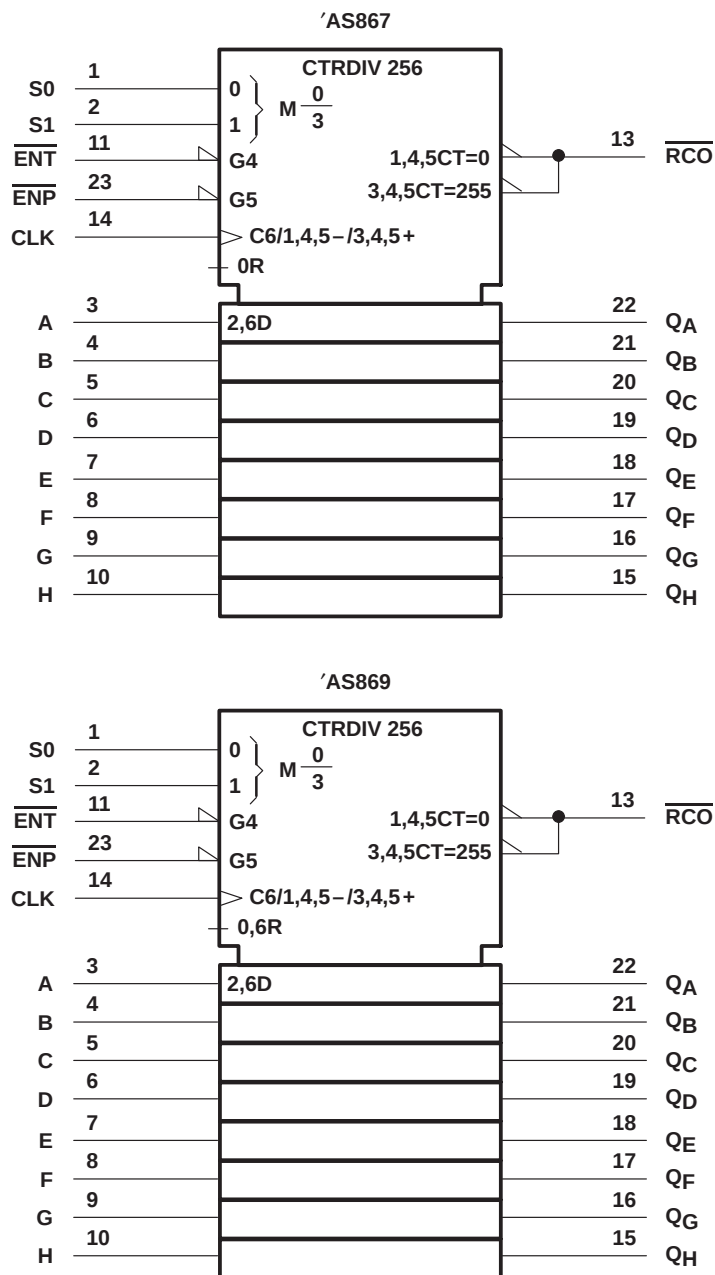


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic symbols (continued)[†]

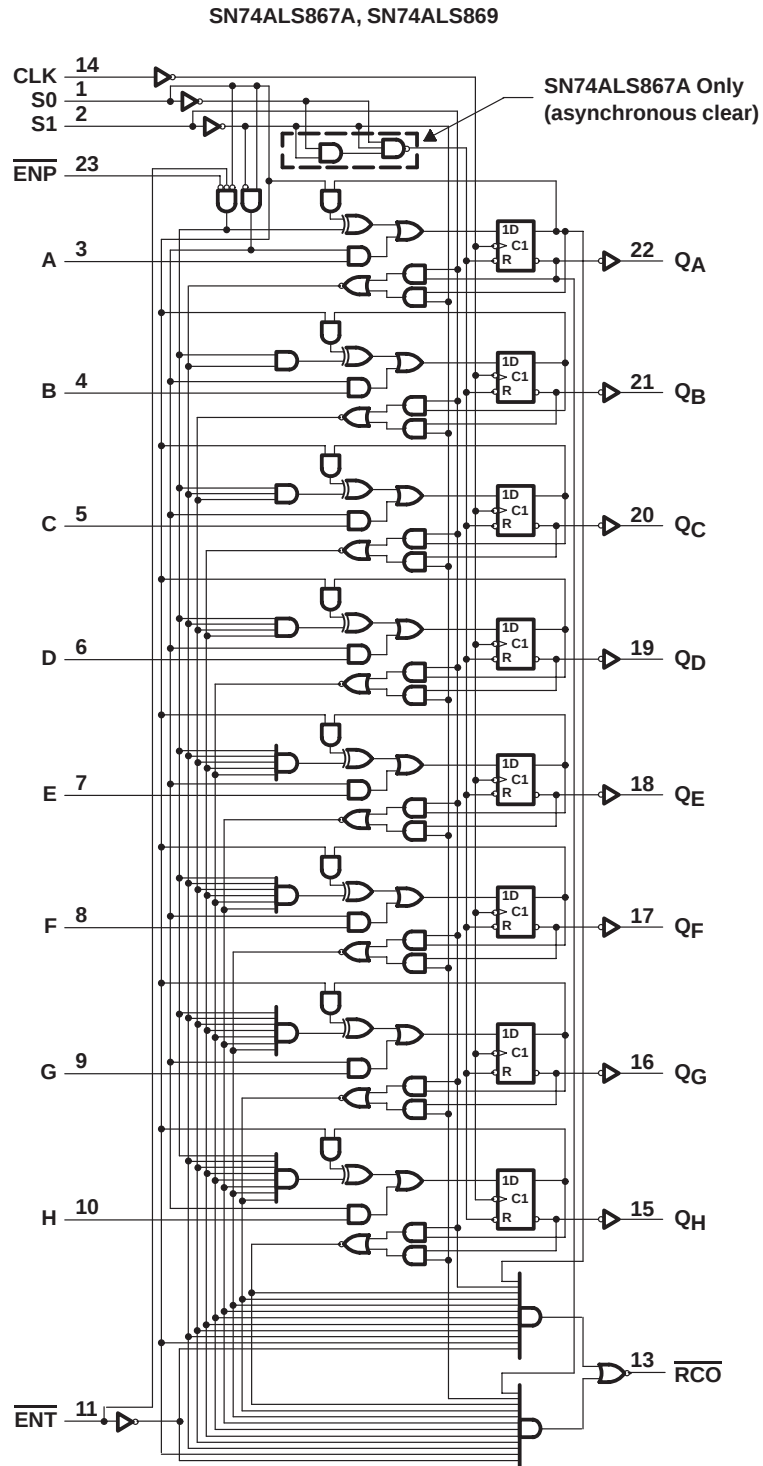


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic diagram (positive logic)

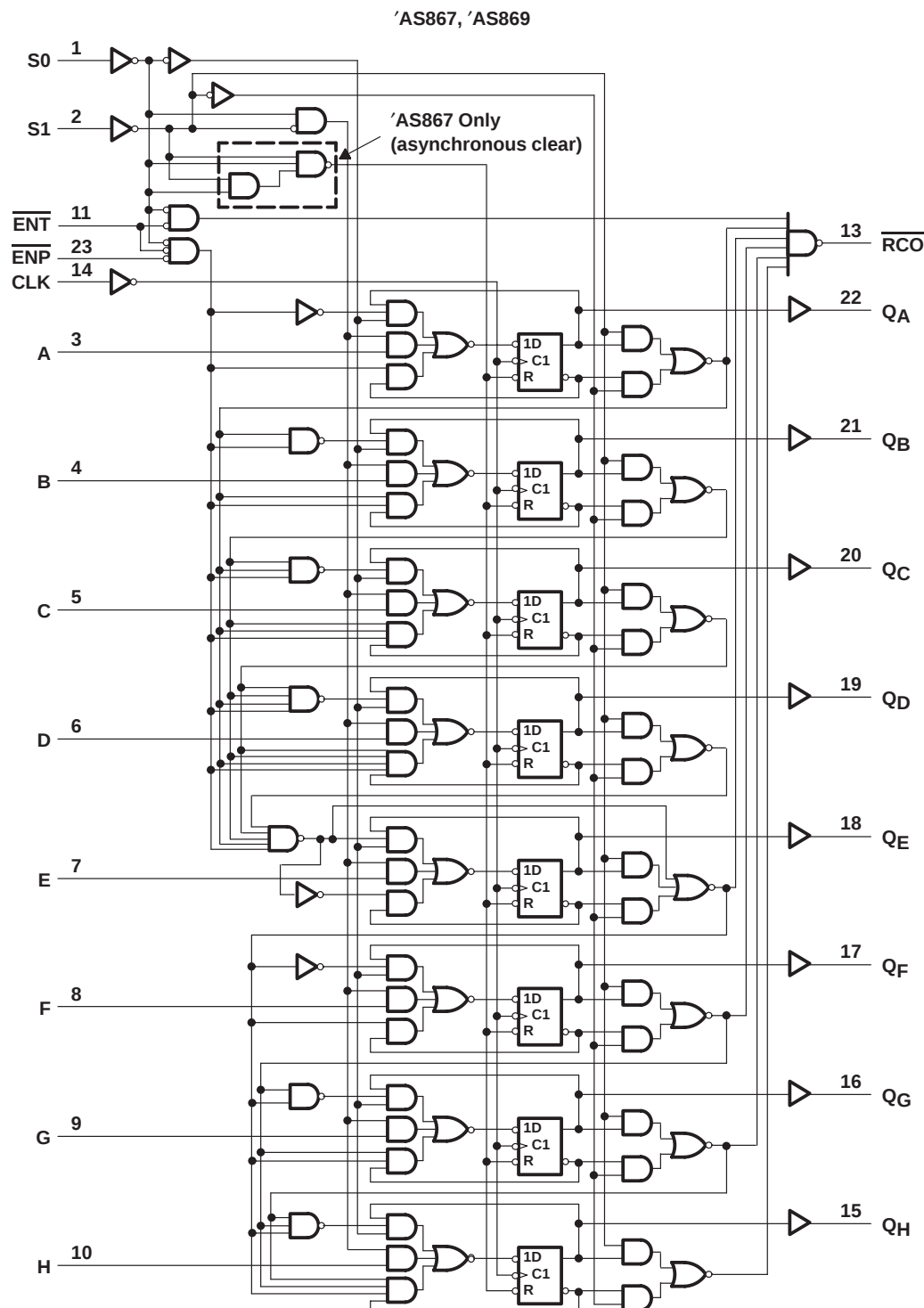


Pin numbers shown are for the DW, JT, and NT packages.

**SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS**

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic diagram (positive logic)

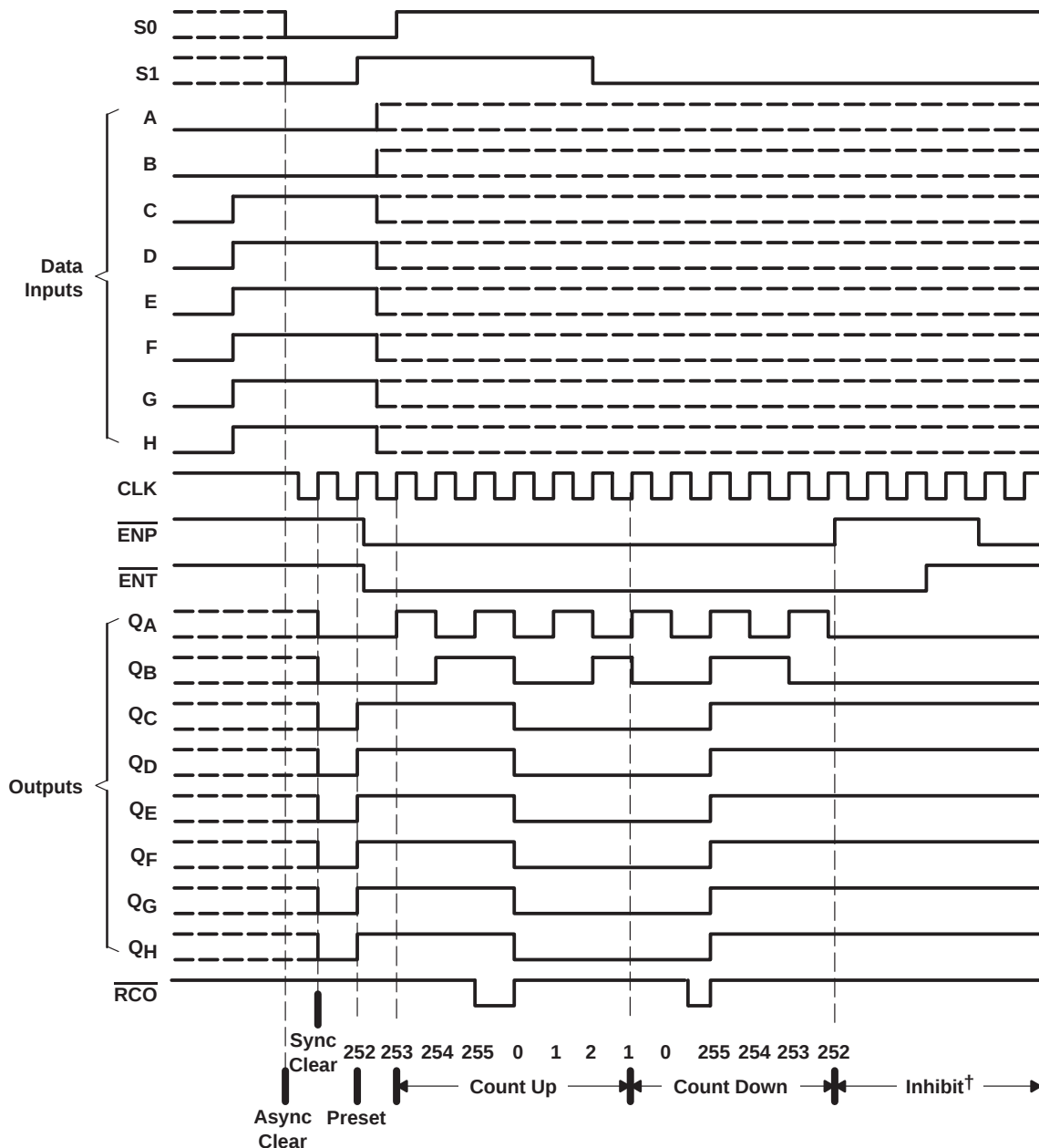


Pin numbers shown are for the DW, JT, and NT packages.

typical clear, preset, count, and inhibit sequences

The following sequence is illustrated below:

1. Clear outputs to zero (SN74ALS867A and 'AS867 are asynchronous; SN74ALS869 and 'AS869 are synchronous.)
2. Preset to binary 252
3. Count up to 253, 254, 255, 0, 1, and 2
4. Count down to 1, 0, 255, 254, 253, and 252
5. Inhibit



† ENT and ENP both must be low for counting to occur.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN74ALS867A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS867A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
f_{clock}	Clock frequency	0		35	MHz
$t_{w(clock)}$	Pulse duration, CLK high or low	14			ns
$t_{w(clear)}$	Pulse duration of clear pulse, S0 and S1 low	10			ns
t_{su}	Setup time before CLK $\uparrow$	Data inputs A–H	10		ns
		$\overline{ENP}$ or $\overline{ENT}$	15		
		S0 low and S1 high (load)	12		
		S0 high and S1 low (count down)	12		
		S0 and S1 high (count up)	12		
t_h	Hold time after CLK $\uparrow$	S0 high after S1 $\uparrow$ or S1 high after S0 $\uparrow$	3		ns
		Data inputs A–H	0		
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS867A			UNIT
		MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V
		$I_{OL} = 8\text{ mA}$	0.35	0.5	
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$		0.1		mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$		20		μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$		–0.2		mA
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	–30		–112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$		28	45	mA

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS867A		
			MIN	MAX	
f _{max}			35		MHz
t _{PLH}	CLK	$\overline{\text{RCO}}$	4	14	ns
t _{PHL}			4	14	
t _{PLH}	CLK	Any Q	3	16	ns
t _{PHL}			3	16	
t _{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	14	ns
t _{PHL}			2	9	
t _{PHL}	S0 or S1 (clear mode)	Any Q	8	26	ns
t _{PLH}	S0 or S1 (count up/down)	$\overline{\text{RCO}}$	4	16	ns
t _{PHL}			4	16	
t _{PLH}	S0 or S1 (clear mode)	$\overline{\text{RCO}}$	4	16	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN74ALS869	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS869			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
f_{clock}	Clock frequency	0		35	MHz
$t_{w(clock)}$	Pulse duration, CLK high or low	14			ns
t_{su}	Setup time before CLK $\uparrow$	Data inputs A–H	10		ns
		$\overline{ENP}$ or $\overline{ENT}$	15		
		S0 and S1 low (clear)	13		
		S0 low and S1 high (load)	13		
		S0 high and S1 low (count down)	13		
		S0 and S1 high (count up)	13		
t_h	Hold time after CLK $\uparrow$	S0 high after S1 $\uparrow$ or S1 high after S0 $\uparrow$	3		ns
		Data inputs A–H	0		
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS869			UNIT
		MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 4$ mA		0.25	0.4	V
			0.35	0.5	
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1		mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V		20		μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V		–0.2		mA
$I_O^{\S}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V		28	45	mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS869		
			MIN	MAX	
f _{max}			35		MHz
t _{PLH}	CLK	$\overline{\text{RCO}}$	4	14	ns
t _{PHL}			4	14	
t _{PLH}	CLK	Any Q	3	16	ns
t _{PHL}			3	16	
t _{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	14	ns
t _{PHL}			2	9	
t _{PLH}	S1 (count up/down)	$\overline{\text{RCO}}$	4	15	ns
t _{PHL}			4	15	
t _{PLH}	S0 (clear/load)	$\overline{\text{RCO}}$	4	16	ns
t _{PHL}			4	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS867	–55°C to 125°C
SN74AS867	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

		SN54AS867			SN74AS867			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			−2			−2	mA
I _{OL}	Low-level output current			20			20	mA
f _{clock} *	Clock frequency	0		40	0		50	MHz
t _{w(clock)} *	Pulse duration, CLK high or low	12.5			10			ns
t _{w(clear)} *	Pulse duration of clear pulse, S0 and S1 low	12.5			10			ns
t _{su} *	Setup time before CLK↑	Data inputs A–H	5		4			ns
		$\overline{\text{ENP}}$ or $\overline{\text{ENT}}$	9		8			
		S0 low and S1 high (load)	11		10			
		S0 and S1 low (clear)	11		10			
		S0 high and S1 low (count down)	42		40			
		S0 and S1 high (count up)	42		40			
t _h *	Hold time after CLK↑	Data inputs A–H	0		0			ns
t _{skew} *	Skew time between S0 and S1 (maximum to avoid inadvertent clear)			8			7	ns
T _A	Operating free-air temperature	−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS867			SN74AS867			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} − 2			V _{CC} − 2			V
V _{OL}	$\overline{\text{RCO}}$	V _{CC} = 4.5 V	I _{OL} = 20 mA, V _{IL} on ENT = 0.7 V	0.34 0.5					V	
	Other outputs				0.34 0.5					
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	$\overline{\text{ENT}}$	V _{CC} = 5.5 V, V _I = 2.7 V		40			40			μA
	Other inputs			20			20			
I _{IL}	$\overline{\text{ENT}}$	V _{CC} = 5.5 V, V _I = 0.4 V		−4			−4			mA
	Other inputs			−2			−2			
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		−30 −112		−30 −112		mA		
I _{CC}		V _{CC} = 5.5 V		134 195		134 195		mA		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS867		SN74AS867		
			MIN	MAX	MIN	MAX	
f _{max} *			40		50		MHz
t _{PLH}	CLK	$\overline{\text{RCO}}$	5	31	5	22	ns
t _{PHL}			6	19	6	16	
t _{PLH}	CLK	Any Q	3	12	3	11	ns
t _{PHL}			4	16	4	15	
t _{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	19	3	10	ns
t _{PHL}			5	21	5	17	
t _{PLH}	$\overline{\text{ENP}}$	$\overline{\text{RCO}}$	5	16	5	14	ns
t _{PHL}			5	21	5	17	
t _{PHL}	Clear (S0 or S1 low)	Any Q	7	23	7	21	ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} 7 V
Input voltage, V_I 7 V
Operating free-air temperature range, T_A : SN54AS869 –55°C to 125°C
SN74AS869 0°C to 70°C
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS869			SN74AS869			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			−2			−2	mA
I _{OL}	Low-level output current			20			20	mA
f _{clock} *	Clock frequency			40			45	MHz
t _{w(clock)} *	Pulse duration, CLK high or low	12.5			11			ns
t _{su} *	Setup time before CLK↑	Data inputs A–H	6		5			ns
		ENP or ENT	10		9			
		S0 low and S1 high (load)	13		11			
		S0 and S1 low (clear)	13		11			
		S0 high and S1 low (count down)	52		50			
		S0 and S1 high (count up)	52		50			
t _h *	Hold time after CLK↑	Data inputs A–H	0		0			ns
T _A	Operating free-air temperature	−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS869		SN74AS869		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA				V _{CC} − 2		V
		V _{CC} = 4.5 V, I _{OH} = −2 mA		V _{CC} − 2*				
V _{OL}	$\overline{\text{RCO}}$	V _{CC} = 4.5 V	I _{OL} = 20 mA, V _{IL} on $\overline{\text{ENT}}$ = 0.7 V	0.34 0.5				V
	Other outputs		I _{OL} = 20 mA			0.34 0.5		
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
I _{IH}	$\overline{\text{ENT}}$	V _{CC} = 5.5 V, V _I = 2.7 V		40		40		μA
	Other inputs			20		20		
I _{IL}	$\overline{\text{ENT}}$	V _{CC} = 5.5 V, V _I = 0.4 V		−4		−4		mA
	Other inputs			−2		−2		
I _O †		V _{CC} = 5.5 V, V _O = 2.25 V		−30 −112		−30 −112		mA
I _{CC}		V _{CC} = 5.5 V		134 195		134 195		mA

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS869		SN74AS869		
			MIN	MAX	MIN	MAX	
f _{max} *			40		45		MHz
t _{PLH}	CLK	$\overline{\text{RCO}}$	6	35	6	35	ns
t _{PHL}			6	20	6	18	
t _{PLH}	CLK	Any Q	3	12	3	11	ns
t _{PHL}			4	16	4	15	
t _{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3	25	3	15	ns
t _{PHL}			6	21	6	17	
t _{PLH}	$\overline{\text{ENP}}$	$\overline{\text{RCO}}$	5	27	5	19	ns
t _{PHL}			6	21	6	18	

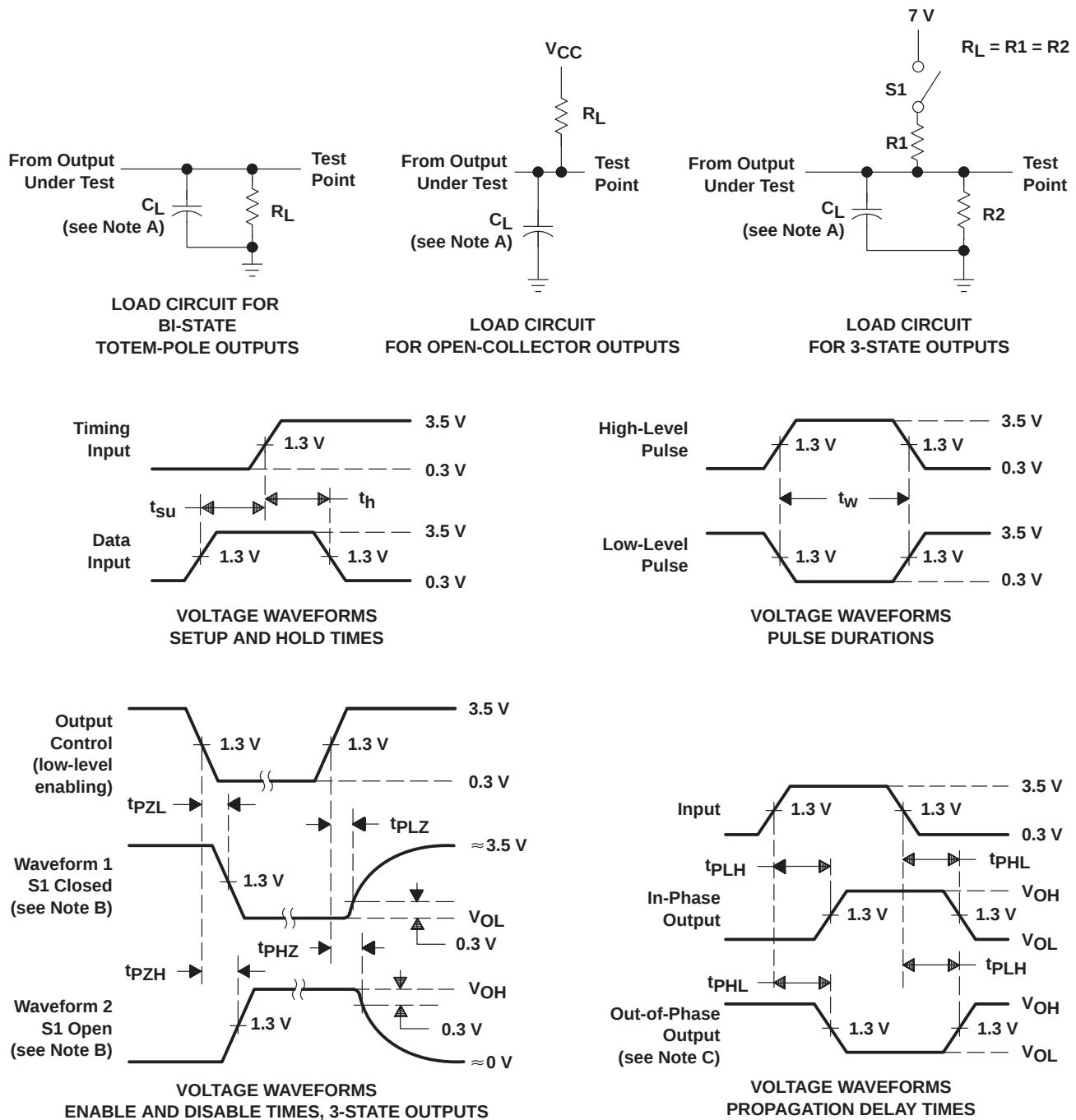
* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8966801LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT
SN54AS867JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS867JT
SN54AS867JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS867JT
SN54AS869JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS869JT
SN54AS869JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS869JT
SN74ALS867ADW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS867A
SN74ALS867ADW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS867A
SN74ALS869DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869
SN74ALS869DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869
SN74ALS869DWE4	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869
SN74AS869DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS869
SN74AS869DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS869
SNJ54AS867JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT
SNJ54AS867JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT
SNJ54AS869JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8952601LA SNJ54AS869JT
SNJ54AS869JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8952601LA SNJ54AS869JT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AS869, SN74AS869 :

- Catalog : [SN74AS869](#)
- Military : [SN54AS869](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE

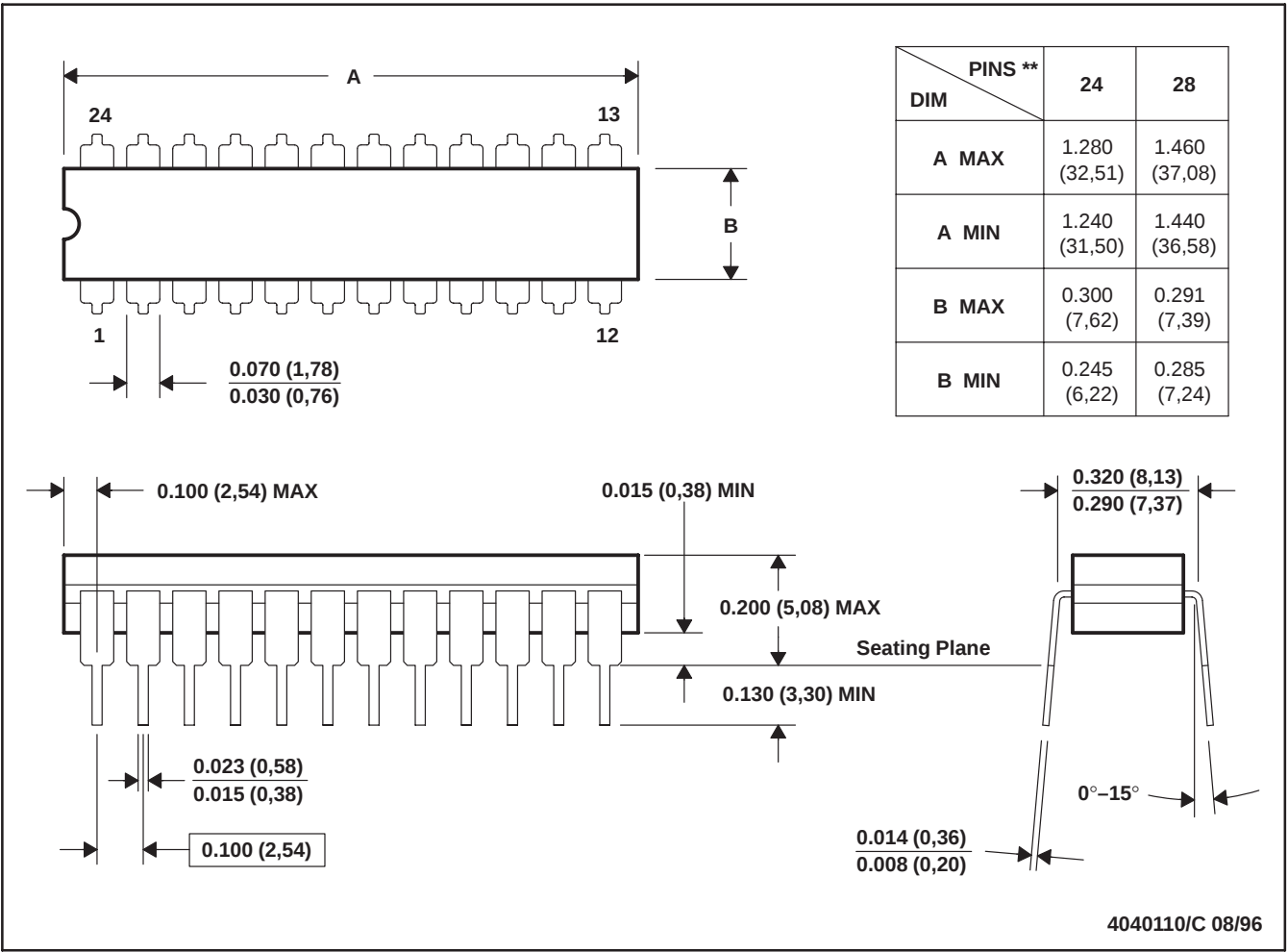


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS867ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS867ADW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS869DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS869DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS869DWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74AS869DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74AS869DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

JT (R-GDIP-T**) 24 LEADS SHOWN

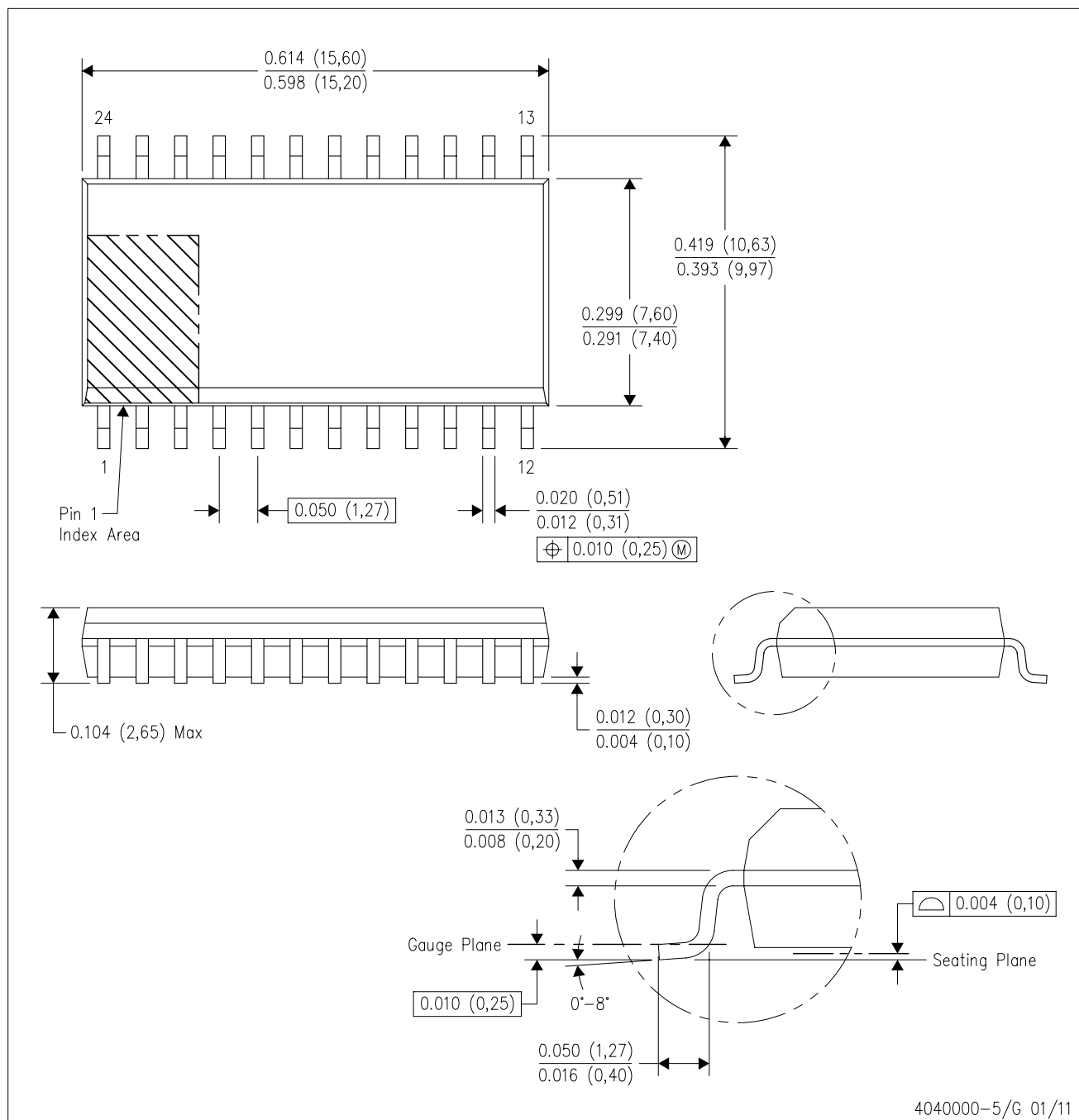
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated