

# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- True Logic
- 3-State Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

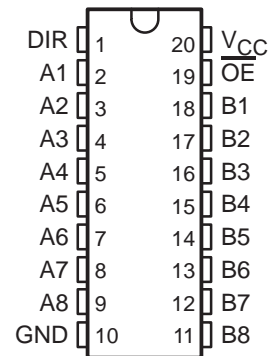
## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

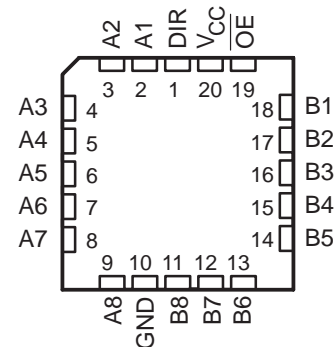
The -1 version of the SN74ALS645A is identical to the standard version, except that the recommended maximum  $I_{OL}$  is increased to 48 mA. There is no -1 version of the SN54ALS645A.

The SN54ALS645A and SN54AS645 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS645A and SN74AS645 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS645A, SN54AS645 . . . J PACKAGE  
SN74ALS645A, SN74AS645 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS645A, SN54AS645 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

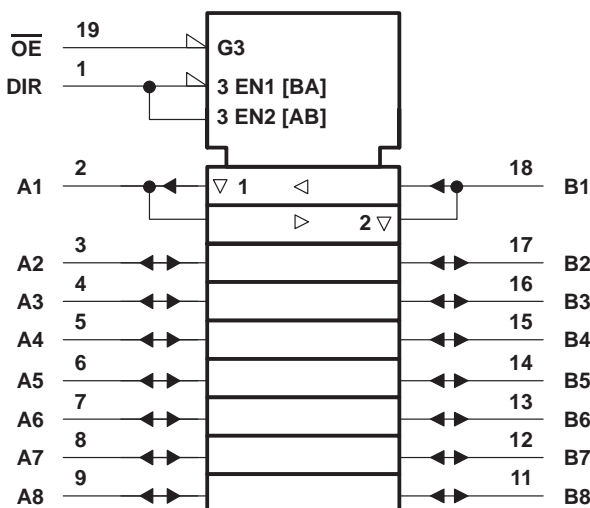
# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645

## OCTAL BUS TRANSCEIVERS

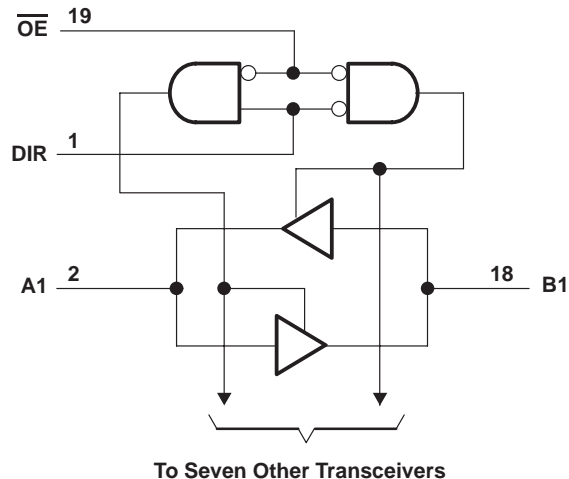
### WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS645A	–55°C to 125°C
SN74ALS645A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN54ALS645A			SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			12			24	mA
							48§	
$T_A$	Operating free-air temperature	–55		125	0		70	°C

§ Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS645A		SN74ALS645A		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA	−1.5		−1.5		V		
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −0.4 mA	V <sub>CC</sub> − 2		V <sub>CC</sub> − 2		V		
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −3 mA	2.4	3.2	2.4		3.2	
			I <sub>OH</sub> = −12 mA	2					
			I <sub>OH</sub> = −15 mA			2			
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V	
			I <sub>OL</sub> = 24 mA			0.35	0.5		
			I <sub>OL</sub> = 48 mA‡			0.35	0.5		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V		0.1		0.1	mA	
	A or B ports		V <sub>I</sub> = 5.5 V		0.1		0.1		
I <sub>IH</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20		20		μA		
	A or B ports§		20		20				
I <sub>IL</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	−0.1		−0.1		mA		
	A or B ports§		−0.1		−0.1				
I <sub>O</sub> ¶		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	−20	−112	−30	−112	mA		
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V	Outputs high		30	48	30	45	mA
			Outputs low		36	60	36	55	
			Outputs disabled		38	63	38	58	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

§ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX#				UNIT
			SN54ALS645A		SN74ALS645A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	19	3	10	ns
t <sub>PHL</sub>			1	14	3	10	
t <sub>PZH</sub>	$\overline{OE}$	A or B	2	30	5	20	ns
t <sub>PZL</sub>			2	29	5	20	
t <sub>PHZ</sub>	$\overline{OE}$	A or B	2	14	2	10	ns
t <sub>PLZ</sub>			2	30	4	15	

# For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54AS645	–55°C to 125°C
SN74AS645	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN54AS645			SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS645			SN74AS645			UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				–1.2			–1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$		2.4	3.2		2.4	3.2		
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -12\text{ mA}$		2.4						
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$					2.4			
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$		0.3	0.55					V
		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 64\text{ mA}$					0.35	0.55		
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$				0.1			0.1	mA
	A or B ports	$V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V}$				0.1			0.1	
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$				20			20	$\mu\text{A}$
	A or B ports <sup>§</sup>	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$				70			70	
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$				–0.5			–0.5	mA
	A or B ports <sup>§</sup>	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$				–0.75			–0.75	
$I_{O}^{\parallel}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$		–50		–150	–50		–150	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , Outputs high		62	97		62	97		mA
		$V_{CC} = 5.5\text{ V}$ , Outputs low		95	149		95	149		
		$V_{CC} = 5.5\text{ V}$ , Outputs disabled		79	123		79	123		

<sup>‡</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

<sup>||</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS645		SN74AS645		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	2	11	2	9.5	ns
t <sub>PHL</sub>			2	10.5	2	9	
t <sub>PZH</sub>	$\overline{OE}$	A or B	2	12	2	11	ns
t <sub>PZL</sub>			2	12	2	10	
t <sub>PHZ</sub>	$\overline{OE}$	A or B	2	8	2	7	ns
t <sub>PLZ</sub>			2	13	2	12	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645

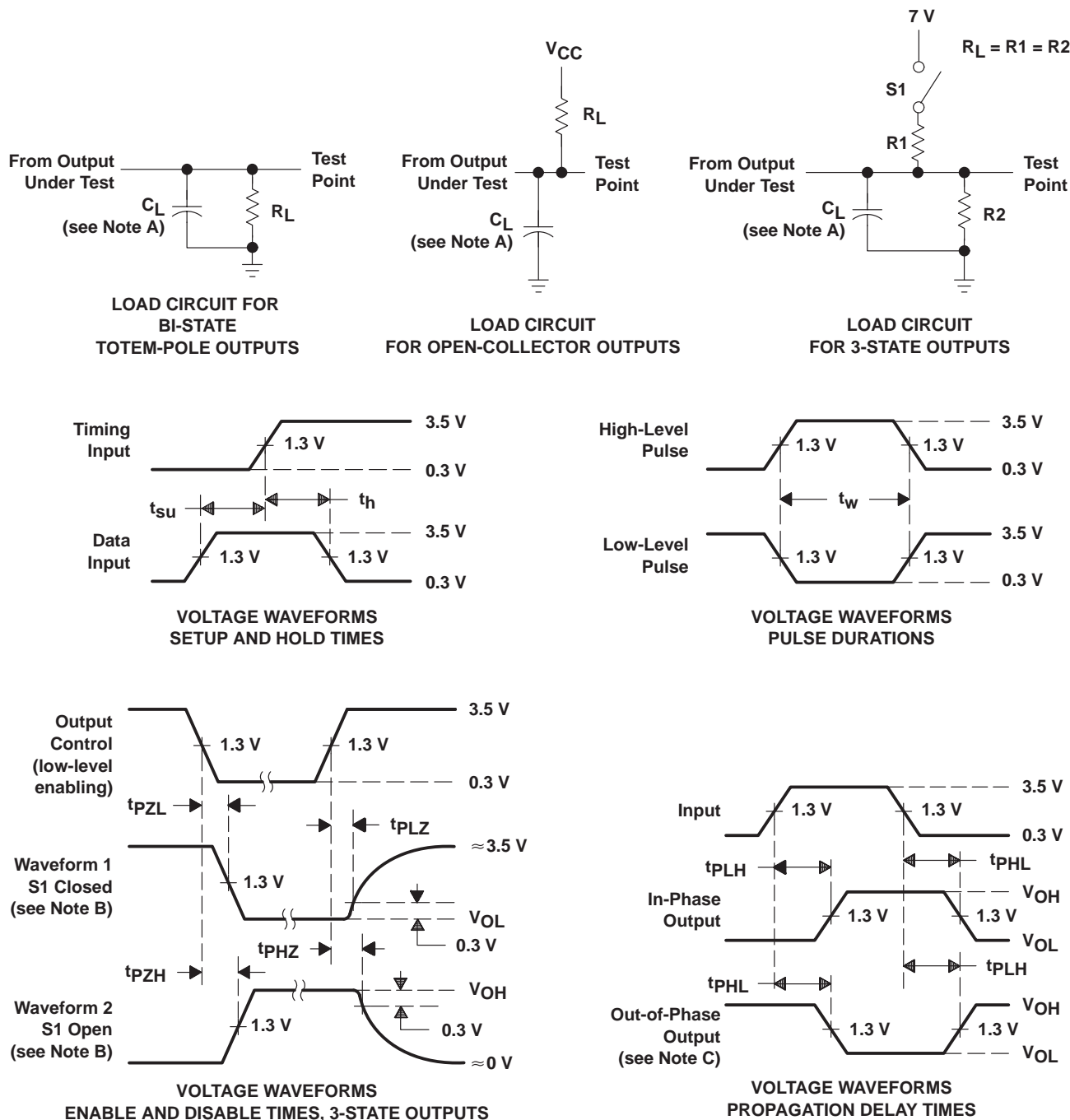
## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

#### PARAMETER MEASUREMENT INFORMATION

#### SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">8403301RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403301RA SNJ54ALS645AJ
<a href="#">8403301SA</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403301SA SNJ54ALS645AW
<a href="#">SN54ALS645AJ</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS645AJ
SN54ALS645AJ.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS645AJ
<a href="#">SN54AS645J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS645J
SN54AS645J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS645J
<a href="#">SN74ALS645A-1DW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	ALS645A-1
<a href="#">SN74ALS645A-1DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1
SN74ALS645A-1DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1
<a href="#">SN74ALS645A-1N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS645A-1N
SN74ALS645A-1N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS645A-1N
<a href="#">SN74ALS645A-1NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1
SN74ALS645A-1NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1
<a href="#">SN74ALS645ADW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	ALS645A
SN74ALS645ADW.B	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	ALS645A
<a href="#">SN74ALS645ADWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A
SN74ALS645ADWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A
<a href="#">SN74ALS645AN</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS645AN
SN74ALS645AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS645AN
<a href="#">SN74ALS645ANSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A
SN74ALS645ANSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A
<a href="#">SN74AS645N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS645N
SN74AS645N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS645N
<a href="#">SNJ54ALS645AJ</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403301RA SNJ54ALS645AJ
SNJ54ALS645AJ.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403301RA SNJ54ALS645AJ

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SNJ54ALS645AW</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403301SA SNJ54ALS645AW
SNJ54ALS645AW.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8403301SA SNJ54ALS645AW
<a href="#">SNJ54AS645J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS645J
SNJ54AS645J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS645J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 :**



- Catalog : [SN74ALS645A](#), [SN74AS645](#)
- Military : [SN54ALS645A](#), [SN54AS645](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

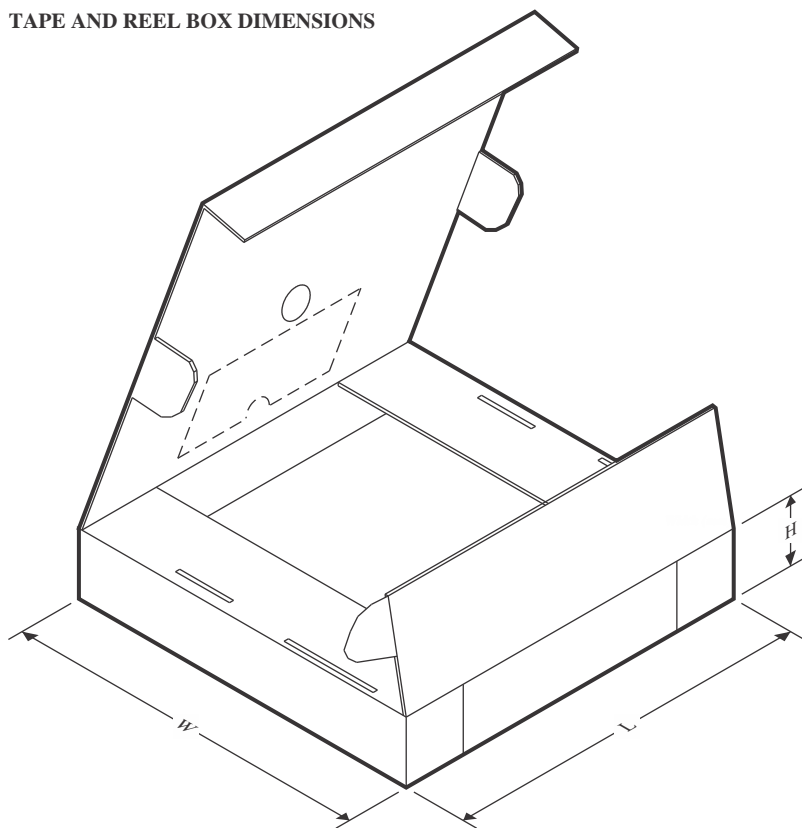
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS645A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS645A-1NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS645ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS645ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS645A-1DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS645A-1NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ALS645ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS645ANSR	SOP	NS	20	2000	356.0	356.0	45.0

## TUBE

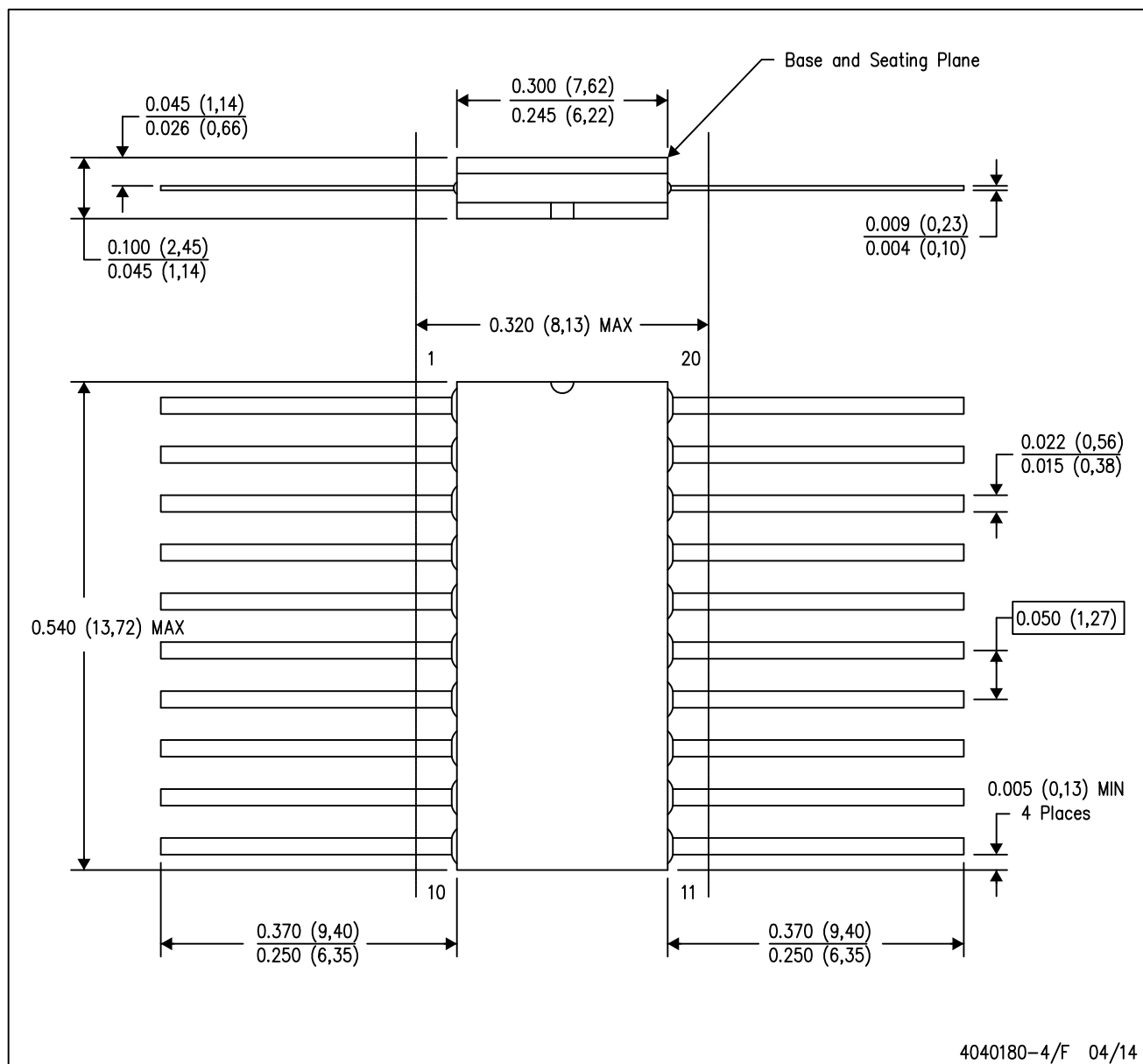


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
8403301SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ALS645A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS645A-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS645AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS645AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS645N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS645N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS645AW	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS645AW.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



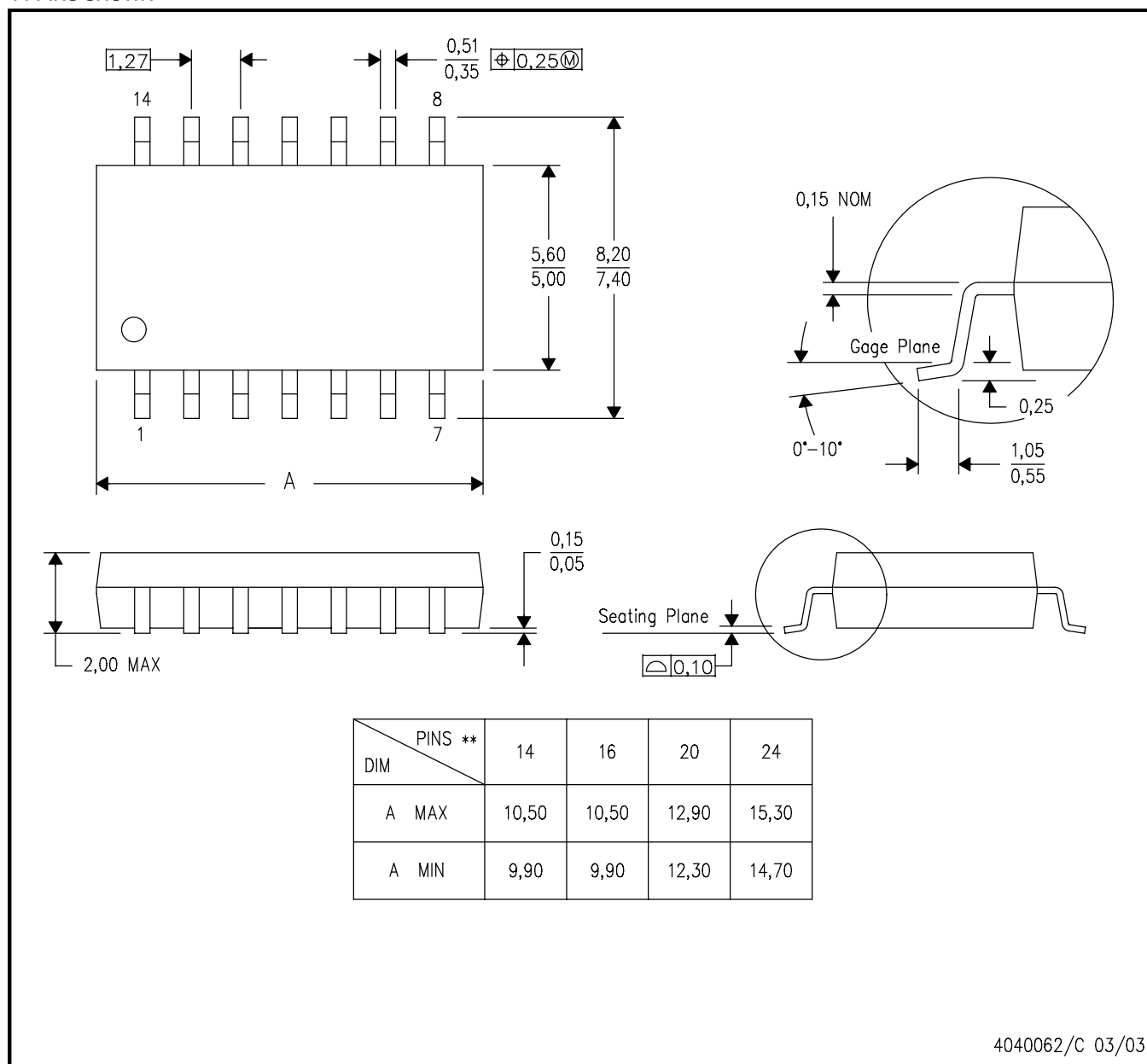
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

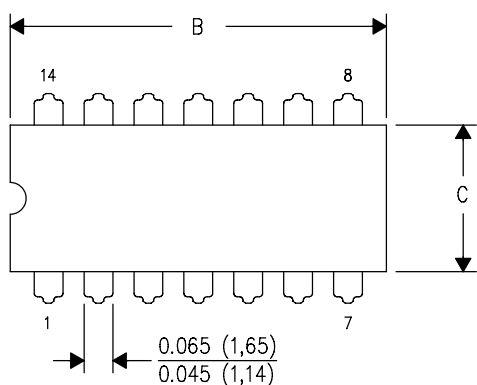
14-PINS SHOWN



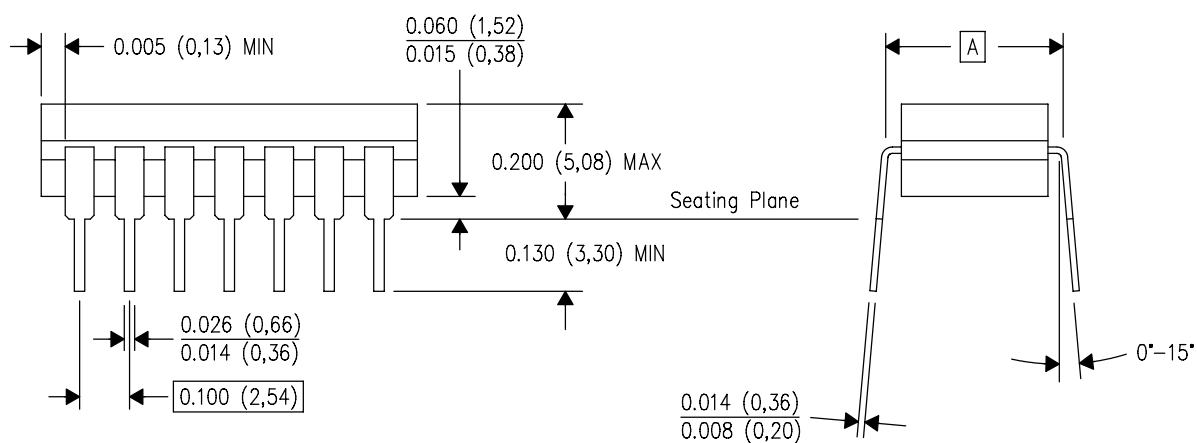
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

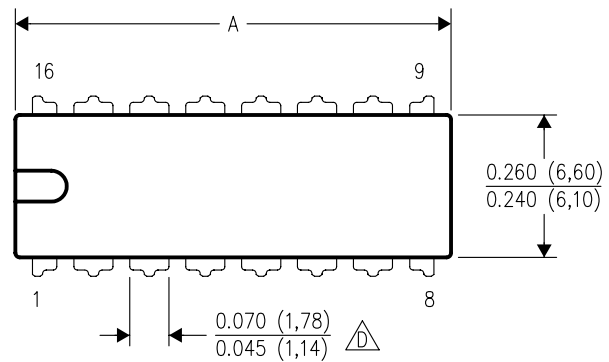
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cop for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

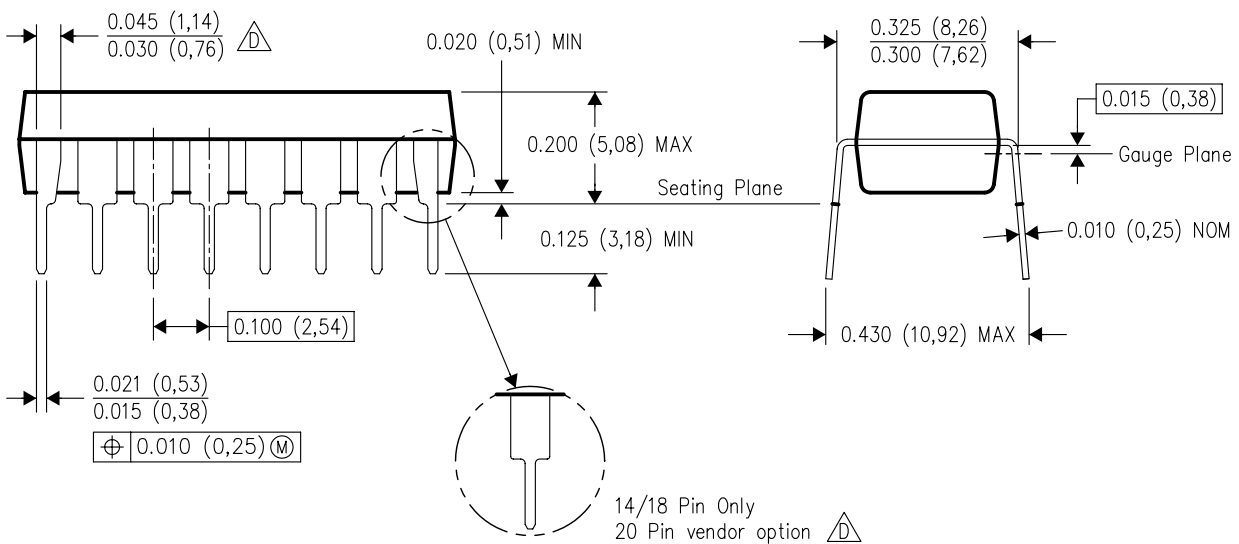
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

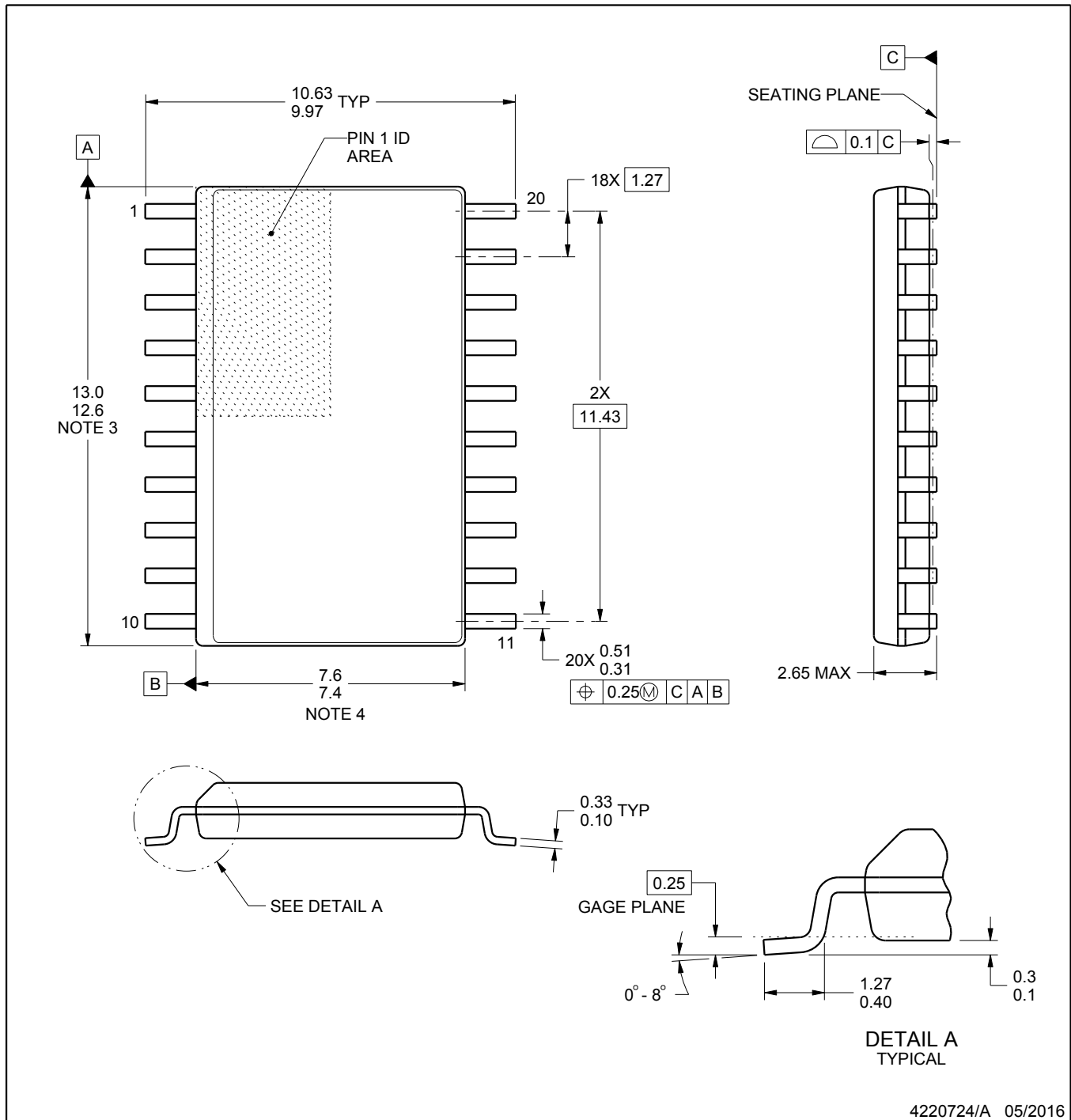
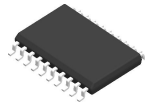


14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.





4220724/A 05/2016

## NOTES:

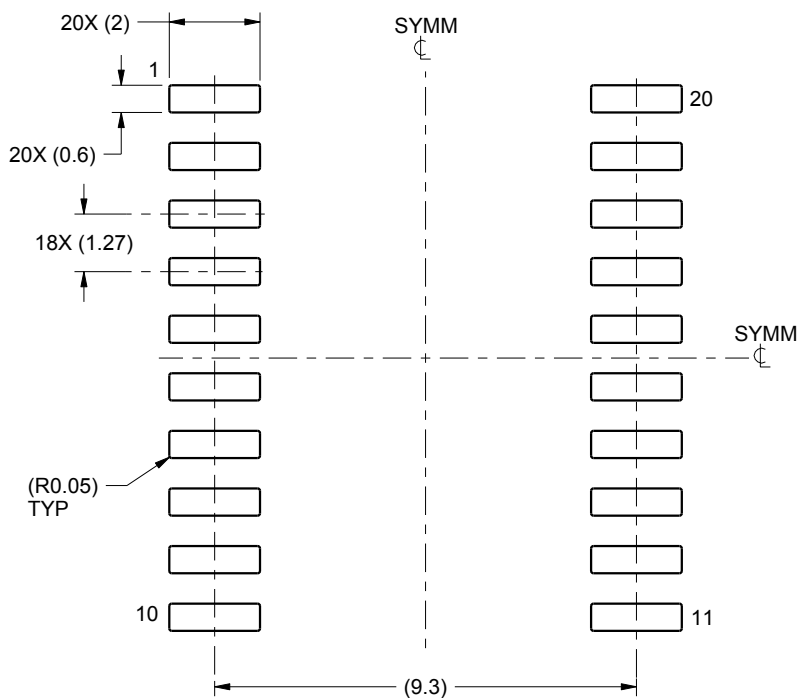
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

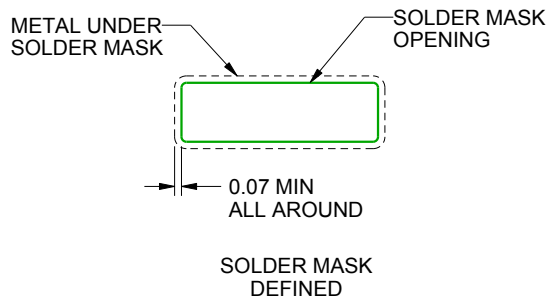
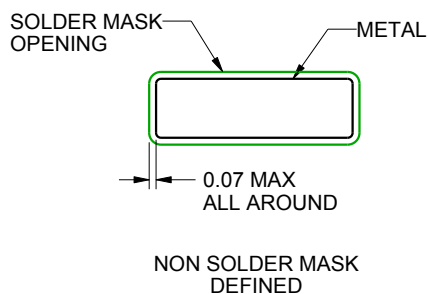
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

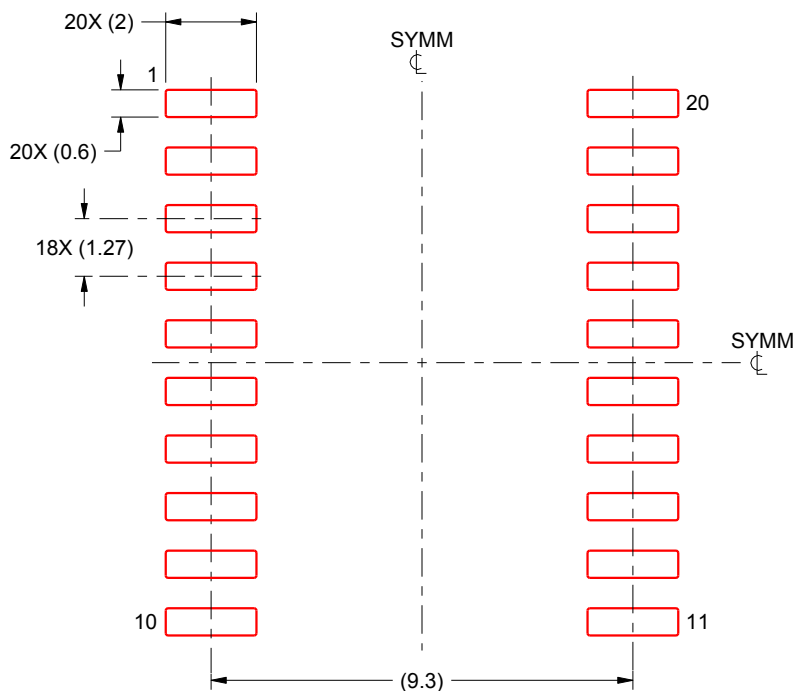
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated