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- Local Bus-Latch Capability
- Choice of True or Inverting Logic
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DEVICE	OUTPUT	LOGIC
SN74ALS620A	3 state	Inverting
SN74ALS621A	Open collector	True
SN74ALS623A, SN74AS623	3 state	True

#### (TOP VIEW) OEAB [ 20 🛭 V<sub>CC</sub> 19 OEBA А1 [ 2 A2 [ 18 B1 3 A3 [ B2 17 A4 🛮 5 16**∏** B3 A5 [ 6 15 □ B4 **∏** B5 A6 ∏ 7 14 A7 **∏** 8 13**∏** B6 A8 [ 9 12 ∏ B7 GND [] 10 11 **∏** B8

DW OR N PACKAGE

#### description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

The output-enable inputs disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and OEBA. Each output reinforces its input in this transceiver configuration. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical for the SN74ALS621A, SN74ALS623A, and SN74AS623 or complementary for the SN74ALS620A.

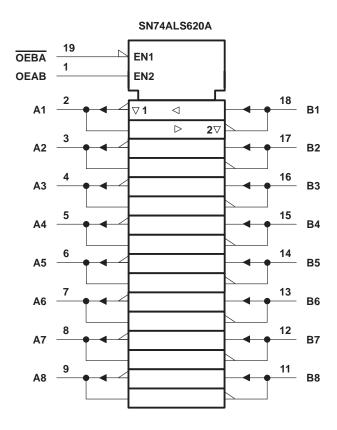
The -1 versions of the SN74ALS620A and SN74ALS621A are identical to the standard versions, except that the recommended maximum I<sub>OI</sub> is increased to 48 mA in the -1 versions.

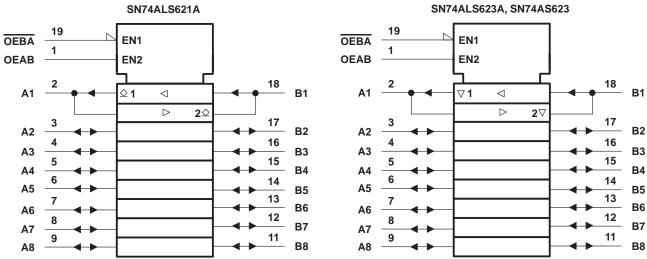
The SN74ALS620A, SN74ALS621A, SN74ALS623A, and SN74AS623 are characterized for operation from 0°C to 70°C.

#### **FUNCTION TABLE**

INPUTS		OPERATION		
OEBA OEAB		SN74ALS620A	SN74ALS621A SN74ALS623A SN74AS623	
L	L	B data to A bus	B data to A bus	
Н	Н	A data to B bus	A data to B bus	
Н	L	Isolation	Isolation	
L	Н	B data to A bus, A data to B bus	B data to A bus, A data to B bus	

## logic symbols†

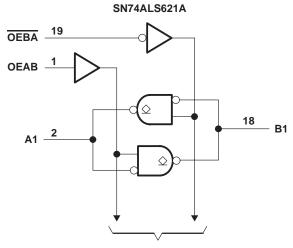




<sup>&</sup>lt;sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagrams (positive logic)

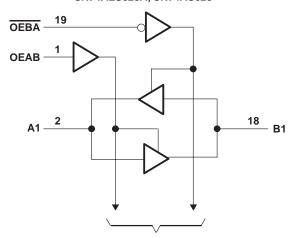
# SN74ALS620A OEBA 19 OEAB 1 18 B1



To Seven Other Transceivers

To Seven Other Transceivers

#### SN74ALS623A, SN74AS623



To Seven Other Transceivers

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub> : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN74ALS620A, SN74ALS623A	0°C to 70°C
Storage temperature range6	5°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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#### recommended operating conditions

		SN74ALS620A SN74ALS623A			UNIT
		MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
IOH	High-level output current			-15	mA
loL	Low-level output current			24	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS620A SN74ALS623A		-	UNIT
				MIN	TYP <sup>†</sup>	MAX	
VIK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2	<u>)</u>		
Vон	VOH	V <sub>CC</sub> = 4.5 V	$I_{OH} = -3 \text{ mA}$	2.4	3.2		V
		∨CC = 4.5 ∨	$I_{OH} = -15 \text{ mA}$	2			
\/a:		V22 - 45 V	I <sub>OL</sub> = 12 mA		0.25	0.4	V
VOL		$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 24 \text{ mA}^{\ddagger}$		0.35	0.5	\ \ \
ı.	Control inputs	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V			0.1	mA
t <sub>1</sub>	A or B ports	vCC = 9.9 v	V <sub>I</sub> = 5.5 V			0.1	mA
I	Control inputs		\/. 0.7.\/			20	
lН	A or B ports§	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 2.7 V			20	μΑ
l	Control inputs	V 55V	\/. 0.4\/			-0.1	mA
IIL	A or B ports§	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.4 V			-0.1	mA
Io¶		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	mA
			Outputs high		24	34	
	SN74ALS620A	$V_{CC} = 5.5 V$	Outputs low		31	44	
			Outputs disabled		33	47	mA
Icc			Outputs high		32	43	IIIA
	SN74ALS623A	$V_{CC} = 5.5 V$	Outputs low		39	50	
			Outputs disabled		42	55	1

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

 $<sup>\</sup>ddagger$  Applies only to the -1 version and only if VCC is between 4.75 V and 5.25 V

 $<sup>\</sup>S$  For I/O ports, the parameters  $I_{\hbox{\scriptsize IH}}$  and  $I_{\hbox{\scriptsize IL}}$  include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	112 = 000;		,	UNIT	
			SN74AL	S620A	SN74AL	S623A	
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	А		2	10	2	13	ns
<sup>t</sup> PHL	A	В	2	10	3	11	115
t <sub>PLH</sub>	В	A	2	10	2	13	ns
<sup>t</sup> PHL		А	2	10	3	11	115
<sup>t</sup> PZH	OEBA	^	3	17	5	22	ns
t <sub>PZL</sub>	OEBA	А	5	25	5	22	115
<sup>t</sup> PHZ	<del>OEBA</del>	٨	2	12	2	16	ns
<sup>t</sup> PLZ	OEBA	А	3	18	2	19	115
<sup>t</sup> PZH	OFAR	В	3	18	5	22	ns
<sup>t</sup> PZL	OEAB	В	5	25	5	22	115
<sup>t</sup> PHZ	OEAB	В	2	12	2	16	ns
<sup>t</sup> PLZ	OLAB	ט	3	18	2	19	115

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>		 7 V
Input voltage, V <sub>I</sub> : All inputs and I/O ports		 7 V
Operating free-air temperature range, TA:	SN74ALS621A .	 0°C to 70°C
Storage temperature range		 -65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN74ALS621A		UNIT	
		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
Vон	High-level output voltage			5.5	V
la.	Low lovel output ourrant			24	mA
lOL	Low-level output current			48§	mA
TA	Operating free-air temperature	0		70	°C

 $<sup>\</sup>S$  Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CO	NUDITIONS	SN	74ALS62	1A	UNIT
	PARAMETER	TEST CONDITIONS		MIN TYPT		MAX	UNII
٧ıĸ		$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$			-1.5	V
IOH		$V_{CC} = 4.5 V,$	V <sub>OH</sub> = 5.5 V			0.1	mA
\/		V45V	I <sub>OL</sub> = 24 mA		0.35	0.5	V
VOL		VCC = 4.5 V	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 48 \text{ mA}^{\ddagger}$		0.35	0.5	V
ī	Control inputs	V-2 - 5 5 V	V <sub>I</sub> = 7 V			0.1	mA
'1	A or B ports	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V			0.1	mA
	Control inputs	V 55V	\/. 27\/			20	
ΊΗ	A or B ports§	$V_{CC} = 5.5 V$ ,	$V_{I} = 2.7 \text{ V}$			20	μΑ
Ίμ	Control inputs	V 55V				-0.1	A
	A or B ports§	$V_{CC} = 5.5 V$	$V_I = 0.4 V$			-0.1	mA
1		V	Outputs high		29	40	mA
Icc		V <sub>CC</sub> = 5.5 V	Outputs low		35	48	IIIA

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega,$ $T_A = \text{MIN to MAX}$ $\text{SN74ALS621A}$		UNIT
			MIN	MAX	
t <sub>PLH</sub>	А	В	10	33	ns
t <sub>PHL</sub>		В	5	20	113
t <sub>PLH</sub>	В		10	33	ns
<sup>t</sup> PHL	В	A	5	20	115
<sup>t</sup> PLH	<u> </u>		10	39	
<sup>t</sup> PHL	OEBA	A	12	35	ns
t <sub>PLH</sub>	OEAB	В	10	39	
<sup>t</sup> PHL	OEAB	В	12	35	ns

<sup>¶</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V

<sup>§</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub> : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, TA: SN74AS623	0°C to 70°C
Storage temperature range	-65°C to 150°C

#### recommended operating conditions

		SN74AS623		3	UNIT
		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
IOH	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEGT 00ND	SN				
		TEST COND	IIIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
۷ıK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I <sub>OH</sub> = −2 mA	V <sub>CC</sub> -2			
Vон		V 45V	$I_{OH} = -3 \text{ mA}$	2.4	3.2		V
		$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -15 \text{ mA}$	2			
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 64 \text{ mA}$		0.35	0.55	V
1.	Control inputs	V F5V	V <sub>I</sub> = 7 V			0.1	mA
'1	A or B ports	$V_{CC} = 5.5 V$	V <sub>I</sub> = 5.5 V	(			IIIA
1	Control inputs	V	\/. 07\/			20	^
lН	A or B ports§	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 2.7 V			70	μΑ
l	Control inputs	V	\/. 0.4\/			-0.5	A
IIL	A or B ports§	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.4 V			-0.75	mA
IoI		$V_{CC} = 5.5 V,$	V <sub>O</sub> = 2.25 V	-30		-150	mA
			Outputs high		57	93	
ICC		$V_{CC} = 5.5 V$	Outputs low		16	189	mA
			Outputs disabled		71	116	

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>§</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

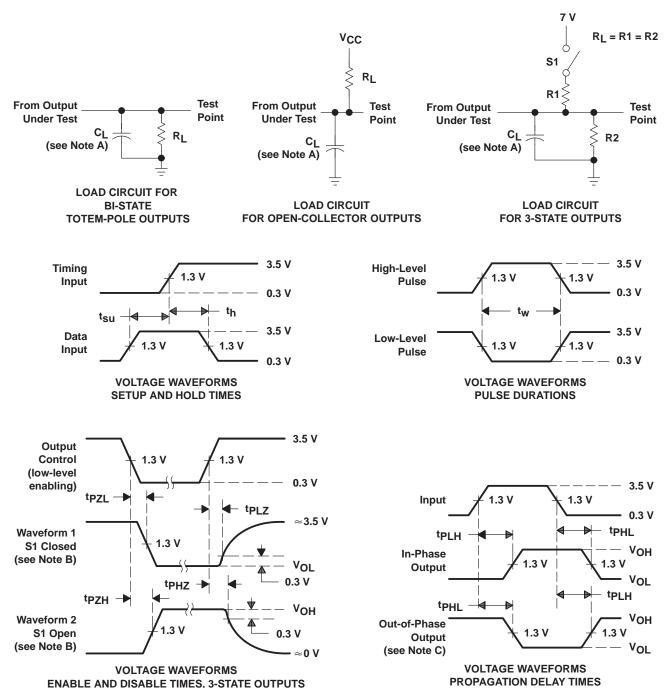
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# switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5^{\circ}$ $C_{L} = 50 \text{ pF}$ $R1 = 500 \Omega$ $R2 = 500 \Omega$ $T_{A} = \text{MIN to}$ $SN74A$	, , , o MAX†	UNIT	
			MIN	MAX	1	
t <sub>PLH</sub>	A		1	9	no	
<sup>t</sup> PHL	A	В	1	8	ns	
t <sub>PLH</sub>	В	•	1	9	ns	
<sup>t</sup> PHL	ם	А	1	8.5	115	
<sup>t</sup> PZH	<del>OEBA</del>	•	2	11		
<sup>t</sup> PZL	OEBA	А	2	10	ns	
<sup>t</sup> PHZ	<del></del> OEBA		1	7.5	ns	
<sup>t</sup> PLZ	OEBA	А	1	11.5	115	
<sup>t</sup> PZH	OFAR		2	11.5	ns	
tPZL	OEAB	В	2	11	115	
<sup>t</sup> PHZ	OEAB	В	1	7	ne	
<sup>t</sup> PLZ	OLAD	ט	1	9	ns	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_f = t_f = 2$  ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms







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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74ALS620ADW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS620A
SN74ALS620ADW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS620A
SN74ALS620AN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS620AN
SN74ALS620AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS620AN
SN74ALS621A-1N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621A-1N
SN74ALS621A-1N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621A-1N
SN74ALS621ADW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS621A
SN74ALS621ADW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS621A
SN74ALS621AN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621AN
SN74ALS621AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS621AN
SN74ALS623ADW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A
SN74ALS623ADW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A
SN74ALS623AN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS623AN
SN74ALS623AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS623AN
SN74ALS623ANSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A
SN74ALS623ANSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS623A

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



# **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS623ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS623ANSR	SOP	NS	20	2000	356.0	356.0	45.0





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#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS620ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS620ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS620AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS620AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621A-1N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS621ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS621AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS621AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS623ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS623ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS623AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS623AN.A	N	PDIP	20	20	506	13.97	11230	4.32

#### **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





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#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



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NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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