# SNx4AHCT540 Octal Buffers/Drivers With 3-State Outputs

## 1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)
  - 200V machine model (A115-A)
  - 1000V charged-device model (C101)

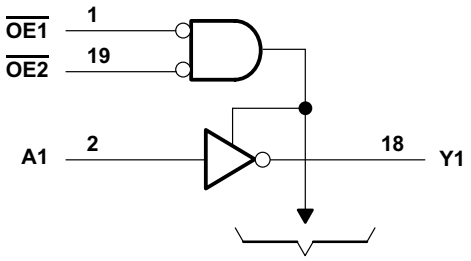
## 2 Description

The ’AHCT540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SNx4AHCT540 | N (PDIP, 20) | 24.33mm × 9.4mm | 24.33mm × 6.35mm |
| | DB (SSOP, 20) | 7.2mm × 7.8mm | 7.2mm × 5.3mm |
| | PW (TSSOP, 20) | 6.50mm × 6.4mm | 6.50mm × 4.40mm |
| | DGV (TVSOP, 20) | 5.00mm × 6.4mm | 5.00mm × 4.40mm |
| | DW (SOIC, 20) | 12.80mm × 10.3mm | 12.80mm × 7.50mm |
| | J (CDIP, 20) | 24.2mm x 7.62mm | 24.2 mm x 6.92mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram (Positive Logic)**

# Table of Contents

# 3 Pin Configuration and Functions

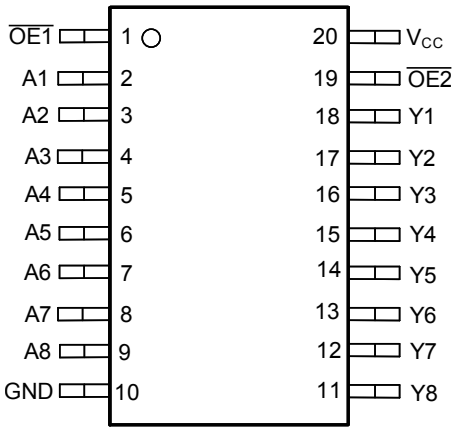



**Figure 3-1. SN54AHCT540: J Package, 20-Pin CDIP; SN74AHCT540: DB, DGV, DW, N, NS, or PW Package; 20-Pin SSOP, TVSOP, SOIC, PDIP, PDIP, or TSSOP(Top View)**

**Table 3-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{OE1}$ | I | Output Enable 1 |
| 2 | A1 | I | A1 Input |
| 3 | A2 | I | A2 Input |
| 4 | A3 | I | A3 Input |
| 5 | A4 | I | A4 Input |
| 6 | A5 | I | A5 Input |
| 7 | A6 | I | A6 Input |
| 8 | A7 | I | A7 Input |
| 9 | A8 | I | A8 Input |
| 10 | GND | — | Ground |
| 11 | Y8 | O | Y8 Output |
| 12 | Y7 | O | Y7 Output |
| 13 | Y6 | O | Y6 Output |
| 14 | Y5 | O | Y5 Output |
| 15 | Y4 | O | Y4 Output |
| 16 | Y3 | O | Y3 Output |
| 17 | Y2 | O | Y2 Output |
| 18 | Y1 | O | Y1 Output |
| 19 | $\overline{OE2}$ | I | Output Enable 2 |
| 20 | $V_{CC}$ | — | Power Pin |

# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ (2) | Input voltage | | –0.5 | 7 | V |
| $V_O$ (2) | Output voltage | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | ($V_I$ < 0) | | –20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 4.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | SN54AHCT540 | | SN74AHCT540 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| Δt/Δv | Input Transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHCT540 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DB (SSOP) | DGV (TVSOP) | DW (SOIC) | N (PDIP) | NS (PDIP) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 70 | 92 | 58 | 69 | 60 | 116.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | SN54AHCT540 | | SN74AHCT540 | | Recommended SN74AHCT540 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OH}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1[1] | | ±1 | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | | ±2.5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 20 | | 40 | µA |
| $\Delta I_{CC}$ [2] | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | | | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 5V | | 4 | | | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or VCC.

## 4.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | SN54AHCT540 | | SN54AHCT540 | | Recommended SN54AHCT540 | | |
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | 4.0[1] | 6.0[1] | 1[1] | 7.5[1] | 1 | 7.5 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | 4.0[1] | 6.0[1] | 1[1] | 7.5[1] | 1 | 7.5 | 1 | 7.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | 5.5[1] | 8.0[1] | 1[1] | 9[1] | 1 | 9.0 | 1 | 9.0 | ns |
| $t_{PZL}$ | | | | 5.5[1] | 8.0[1] | 1[1] | 9[1] | 1 | 9.0 | 1 | 9.0 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | 5.0[1] | 8.0[1] | 1[1] | 9[1] | 1 | 9 | 1 | 9 | ns |
| $t_{PLZ}$ | | | | 5.0[1] | 8.0[1] | 1[1] | 9[1] | 1 | 9 | 1 | 9 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | 6.0 | 8.5 | 1 | 10 | 1 | 10 | 1 | 10 | ns |
| $t_{PHL}$ | | | | 6.0 | 8.5 | 1 | 10 | 1 | 10 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | 7.5 | 11.0 | 1 | 12 | 1 | 12 | 1 | 12 | ns |
| $t_{PZL}$ | | | | 7.5 | 11.0 | 1 | 12 | 1 | 12 | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | 8.0 | 11.0 | 1 | 12 | 1 | 12 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | 8.0 | 11.0 | 1 | 12 | 1 | 12 | 1 | 12 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | 1[2] | | | | 1 | | | |

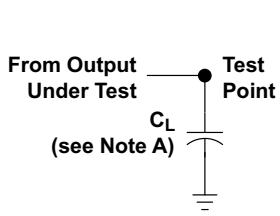
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply

## 4.7 Operating Characteristics

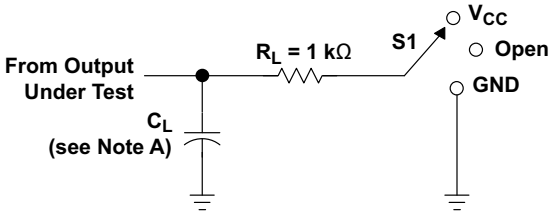
$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 12 | pF |

## 5 Parameter Measurement Information

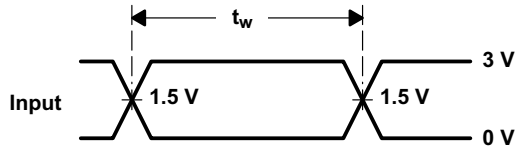



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

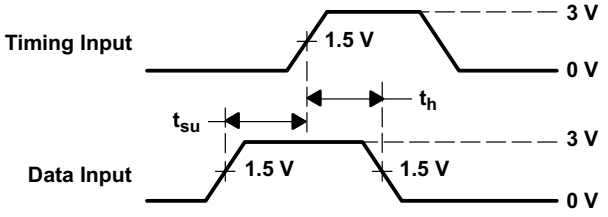



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

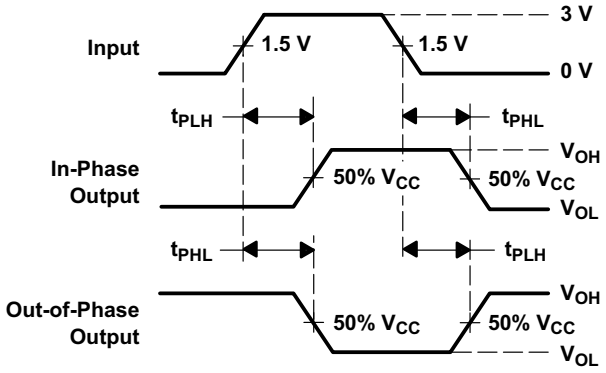
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



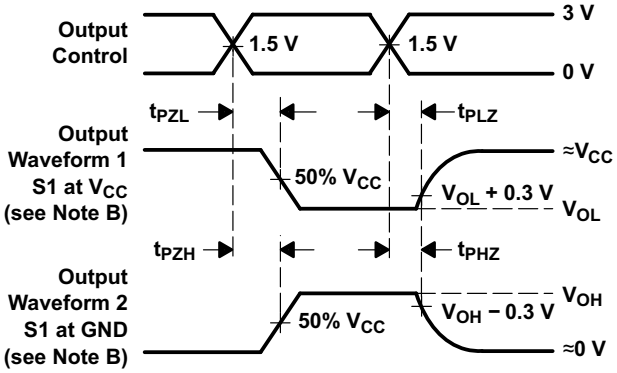

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 5-1. Load Circuit and Voltage Waveforms**

# 6 Detailed Description

## 6.1 Overview

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 6.2 Functional Block Diagram

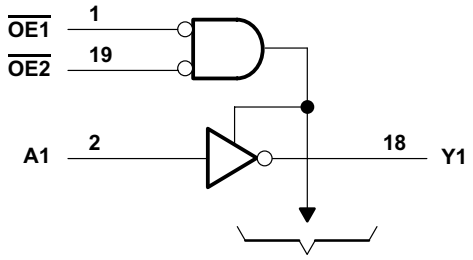



**Figure 6-1. Logic Diagram (Positive Logic)**

## 6.3 Device Functional Modes

Function Table
(Each Buffer/Driver) shows the device functions for each buffer and driver.

**Function Table**
**(Each Buffer/Driver)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ terminals then 0.01 µF or 0.022 µF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.2 Layout

### 7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the Figure 7-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 7.2.2 Layout Example

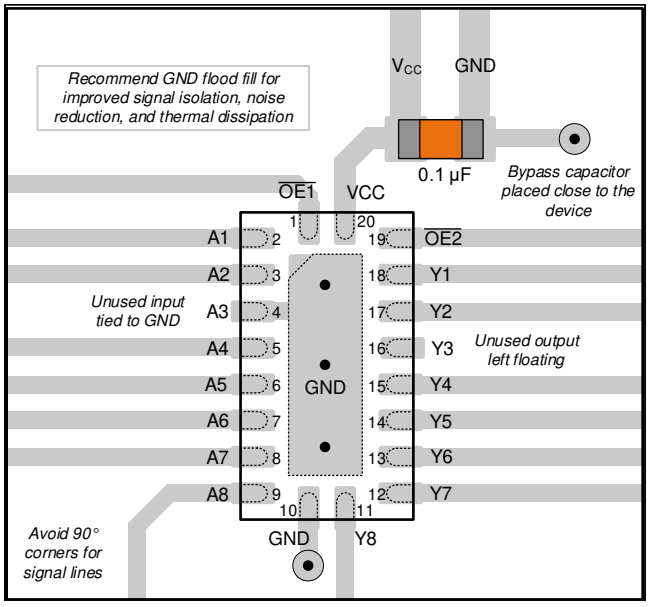



**Figure 7-1. Example Layout for the SN74AHCT540**

# 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

### *8.1.1 Related Links*

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54AHCT540 | Click here | Click here | Click here | Click here | Click here |
| SN74AHCT540 | Click here | Click here | Click here | Click here | Click here |

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision M (June 2013) to Revision N (August 2024) | Page |
|---|---|
| • Added J package to *Device Information* table, *Pin Configuration and Functions* section, and *Thermal Information* section | 1 |
| • Deleted machine model and FK and W packages from data sheet | 1 |
| • Updated RθJA values: PW = 83 to 116.8, all values in °C/W | 4 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9685101QRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685101QR A SNJ54AHCT540J |
| SN74AHCT540DBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB540 |
| SN74AHCT540DBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB540 |
| SN74AHCT540DGVR | Active | Production | TVSOP (DGV) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB540 |
| SN74AHCT540DGVR.A | Active | Production | TVSOP (DGV) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB540 |
| SN74AHCT540DW | Obsolete | Production | SOIC (DW) \| 20 | - | - | Call TI | Call TI | -40 to 125 | AHCT540 |
| SN74AHCT540DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT540 |
| SN74AHCT540DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT540 |
| SN74AHCT540DWRE4 | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT540 |
| SN74AHCT540N | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHCT540N |
| SN74AHCT540N.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHCT540N |
| SN74AHCT540NSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT540 |
| SN74AHCT540NSR.A | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT540 |
| SN74AHCT540PW | Obsolete | Production | TSSOP (PW) \| 20 | - | - | Call TI | Call TI | -40 to 125 | HB540 |
| SN74AHCT540PWR | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB540 |
| SN74AHCT540PWR.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB540 |
| SNJ54AHCT540J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685101QR A SNJ54AHCT540J |
| SNJ54AHCT540J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685101QR A SNJ54AHCT540J |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF SN54AHCT540, SN74AHCT540 :**

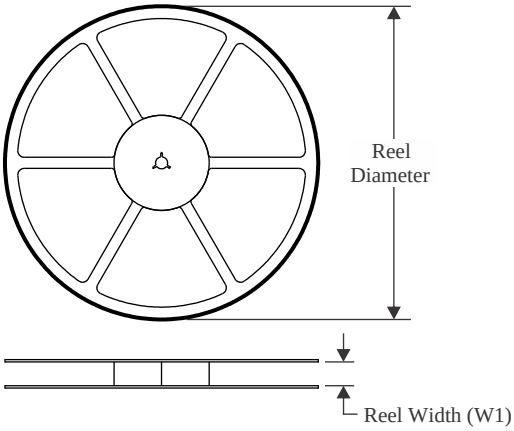
- Catalog : SN74AHCT540
- Military : SN54AHCT540

NOTE: Qualified Version Definitions:

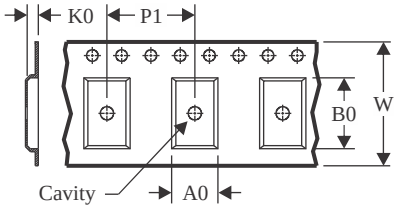
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

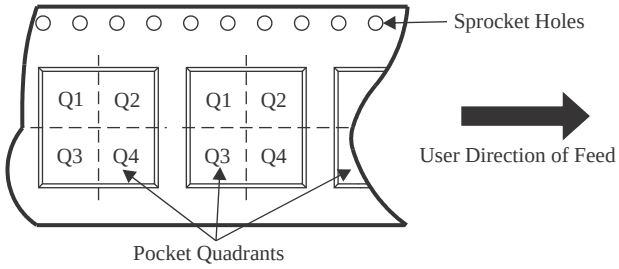



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

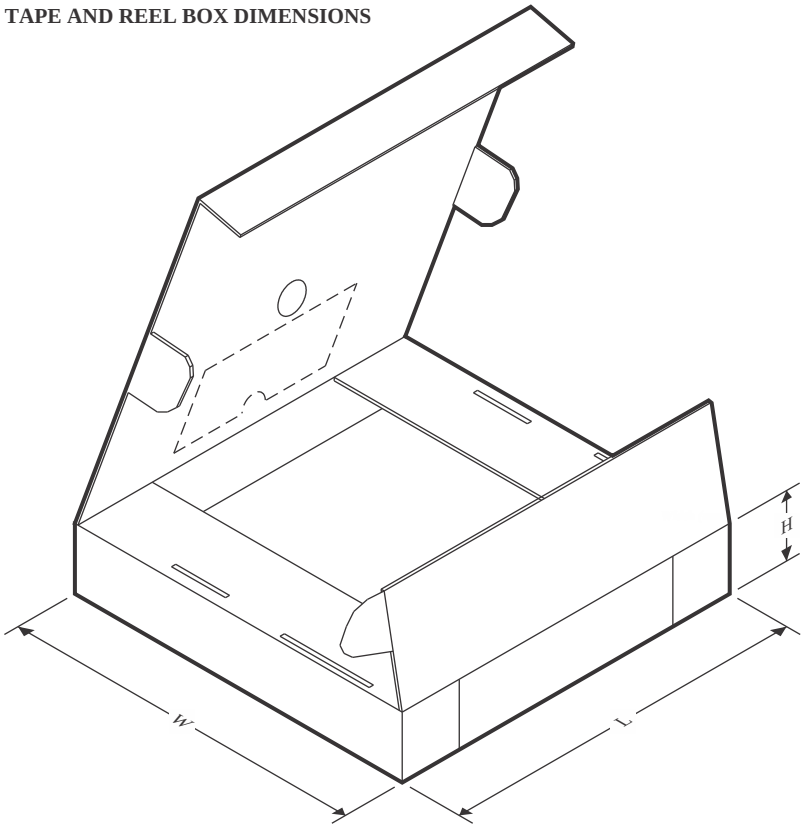
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHCT540DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT540DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT540DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHCT540NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHCT540PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

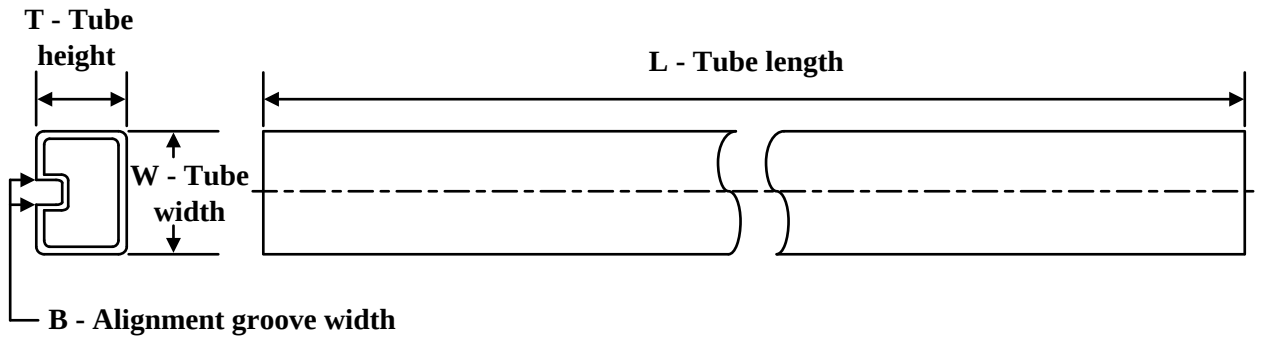
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHCT540DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT540DGVR | TVSOP | DGV | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT540DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHCT540NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHCT540PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

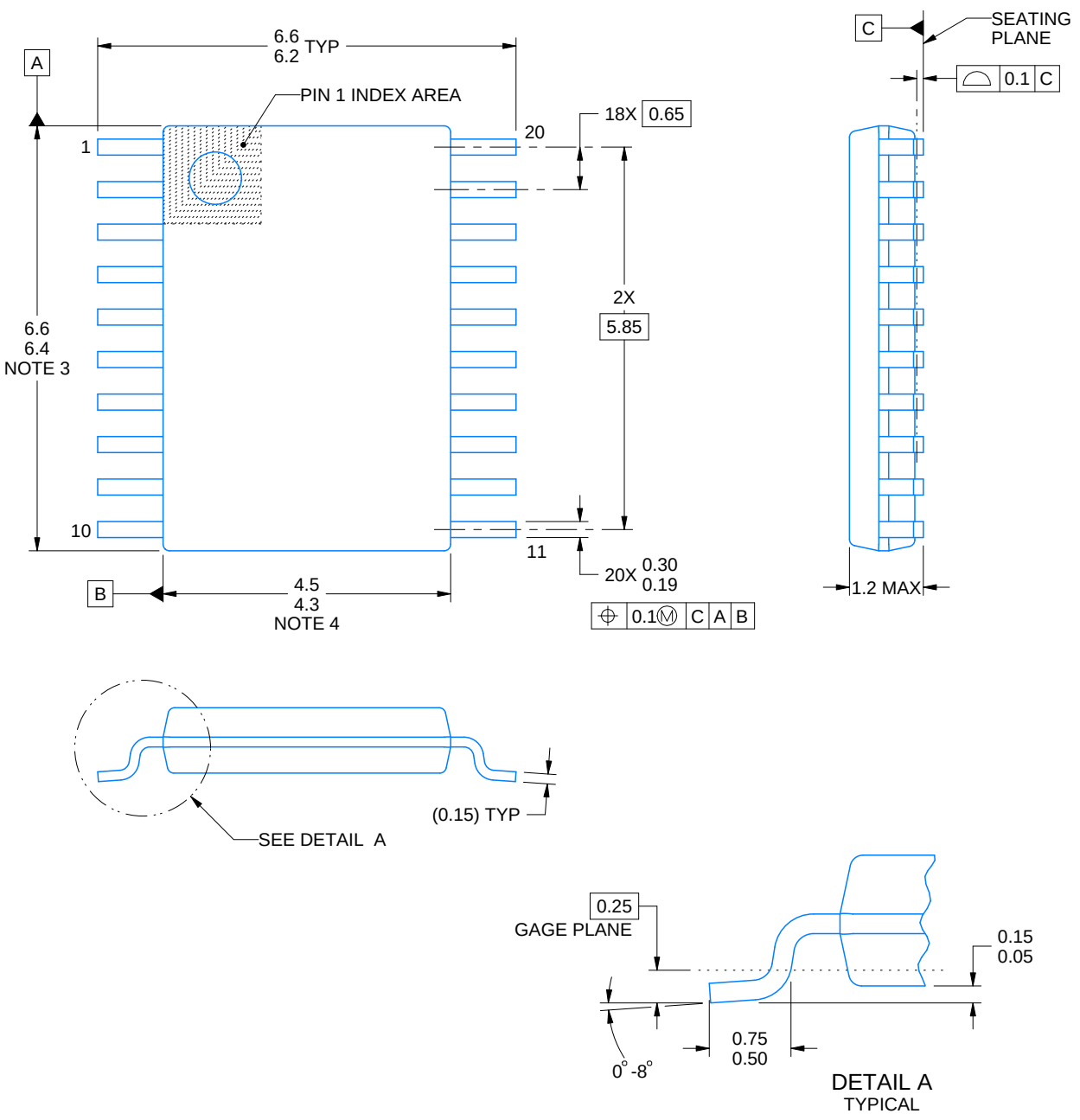
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74AHCT540N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHCT540N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

# PACKAGE OUTLINE

## PW0020A

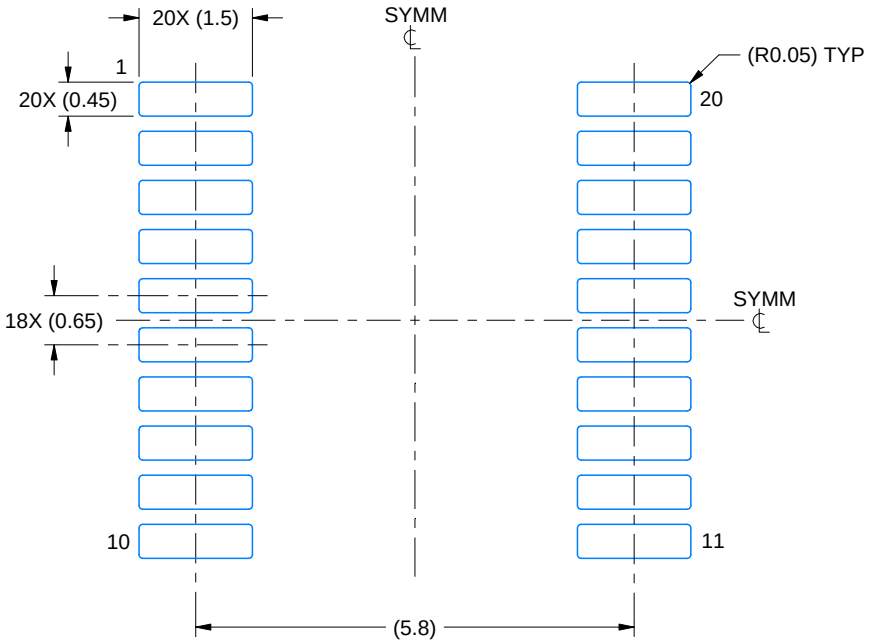
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



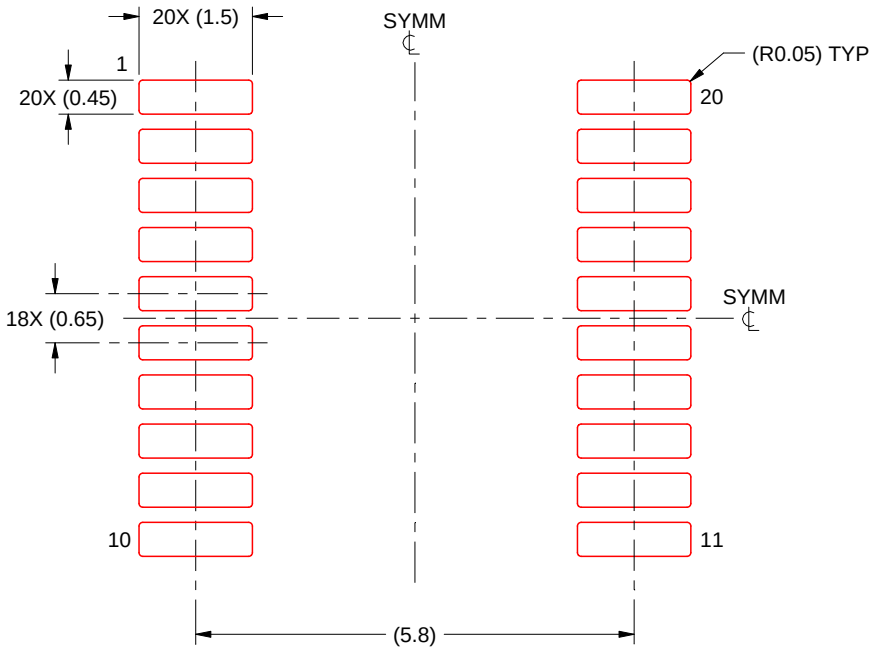

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

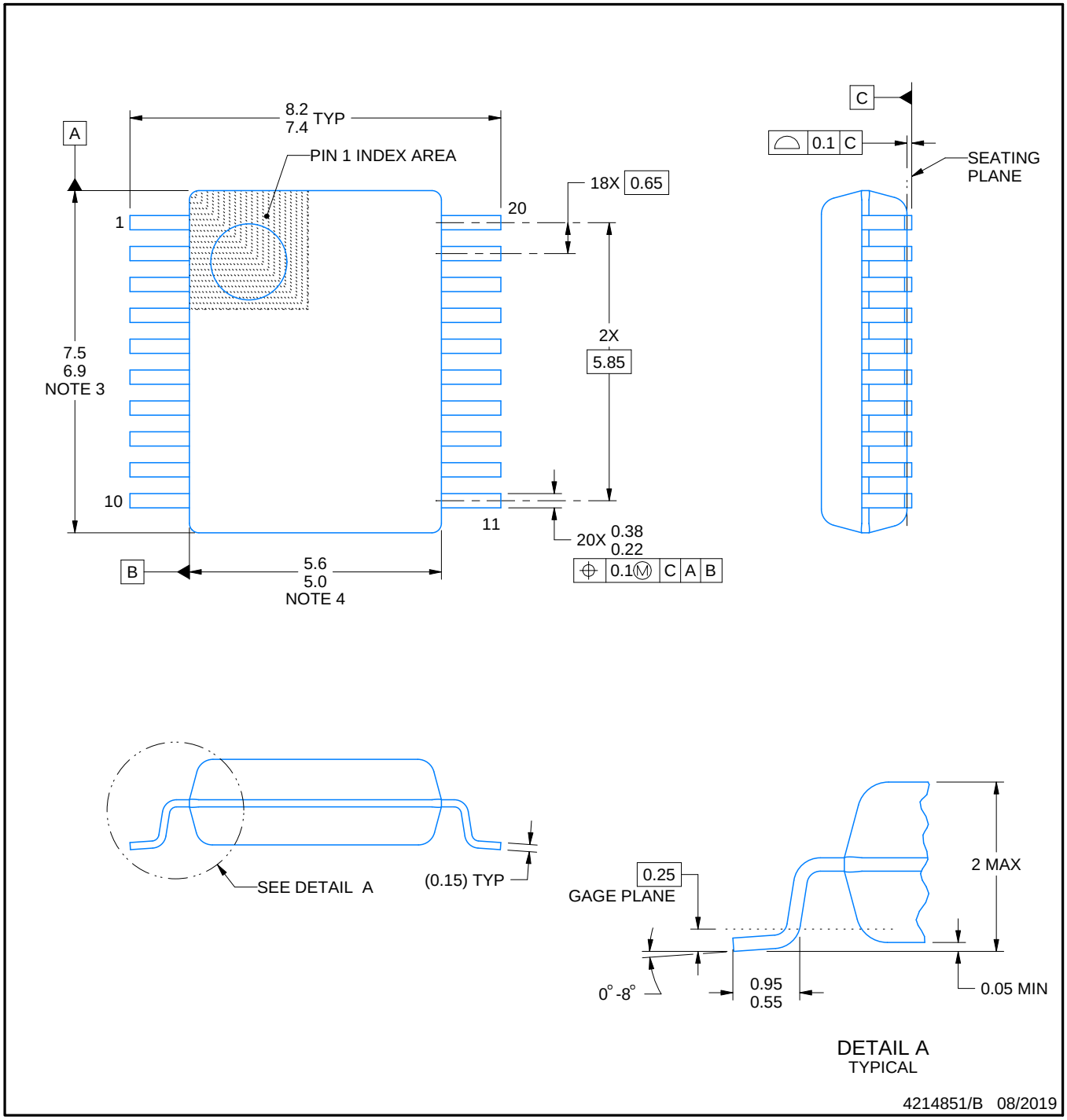
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DB0020A

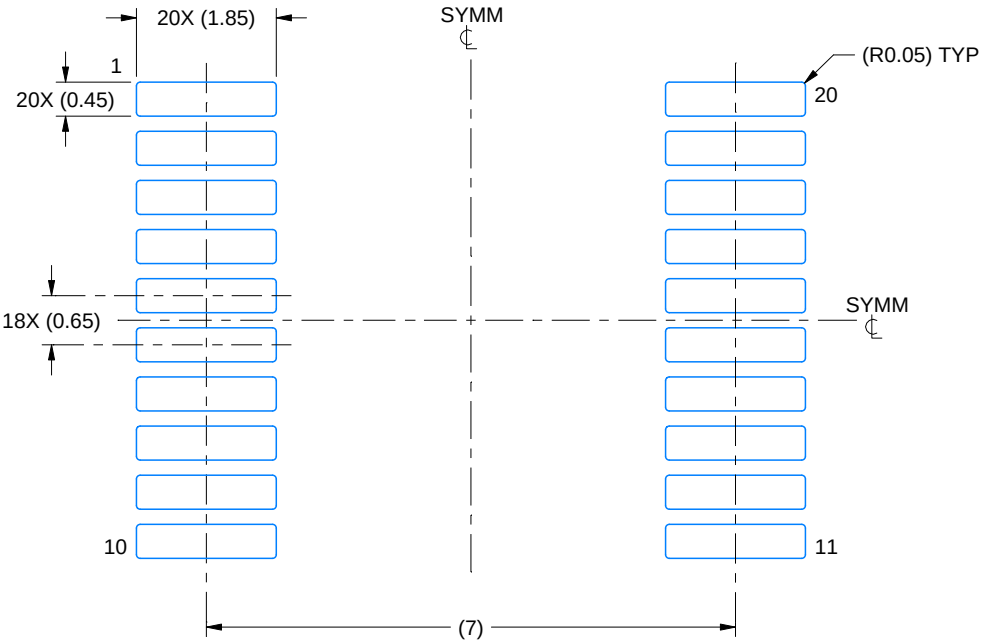
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

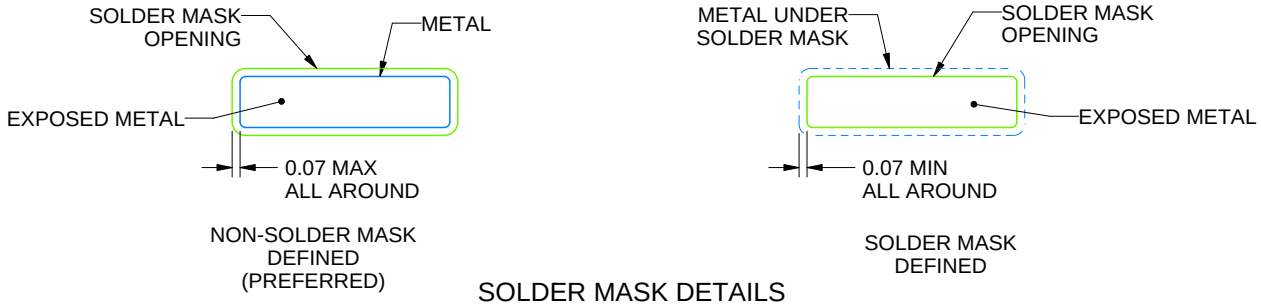



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

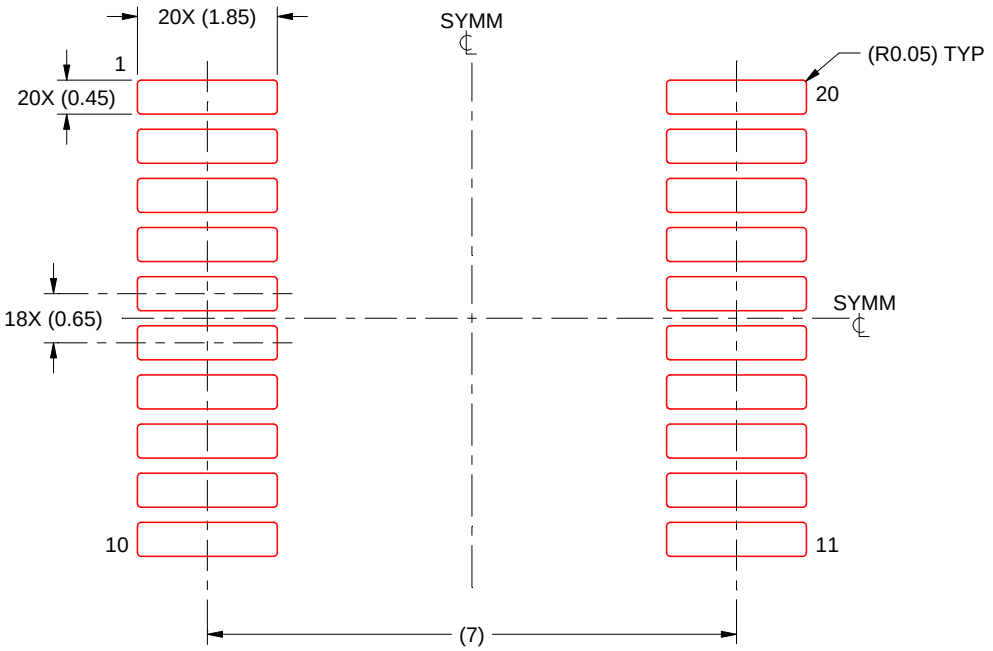
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

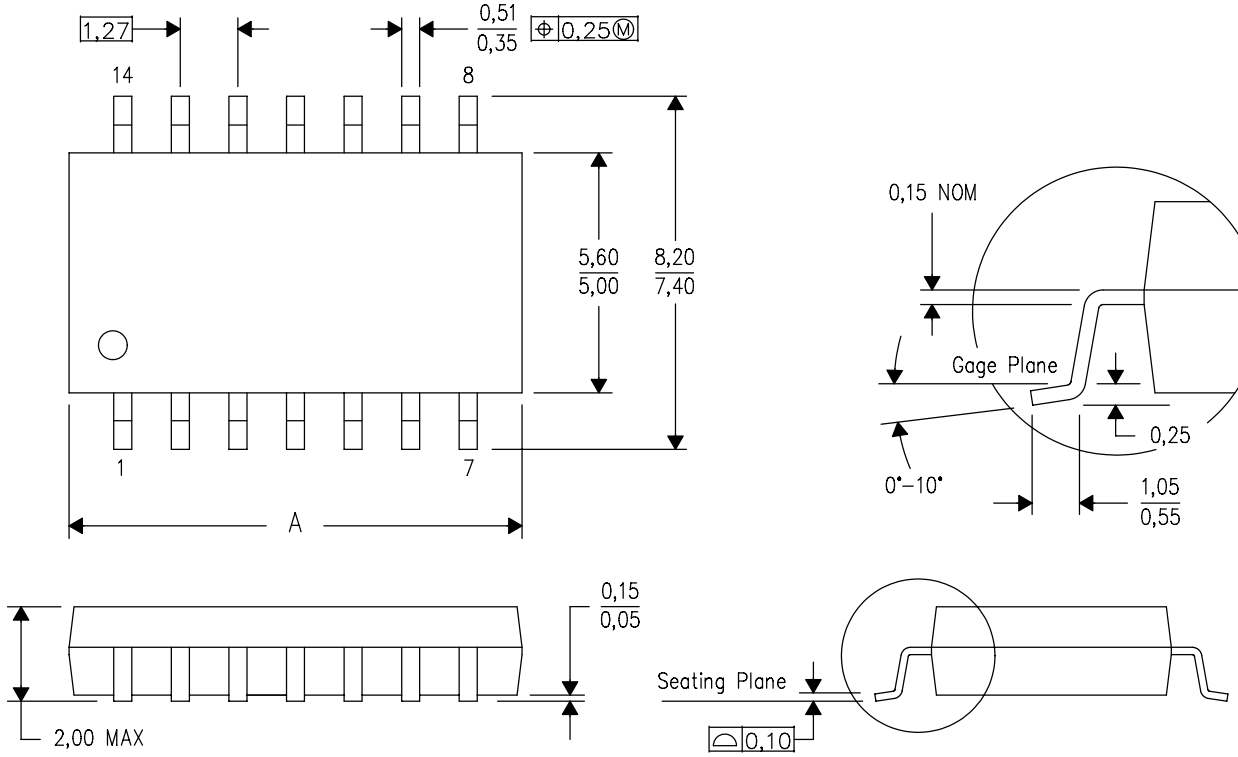
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

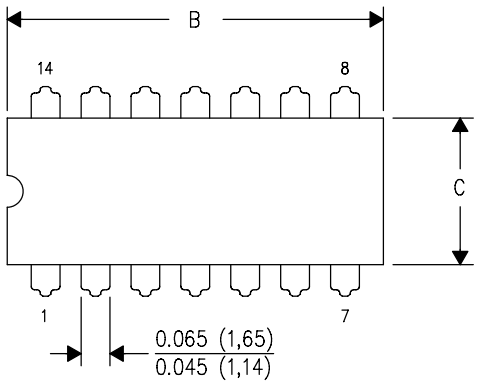
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

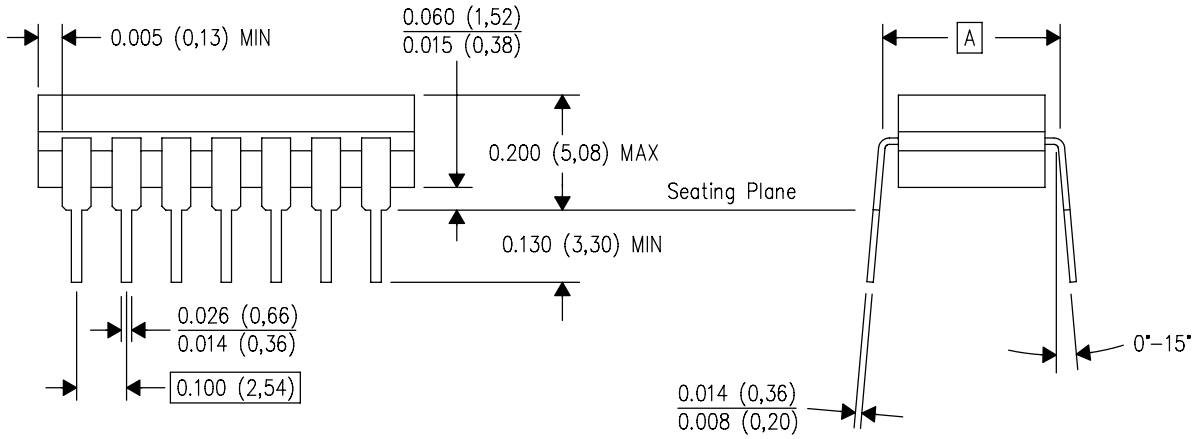
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

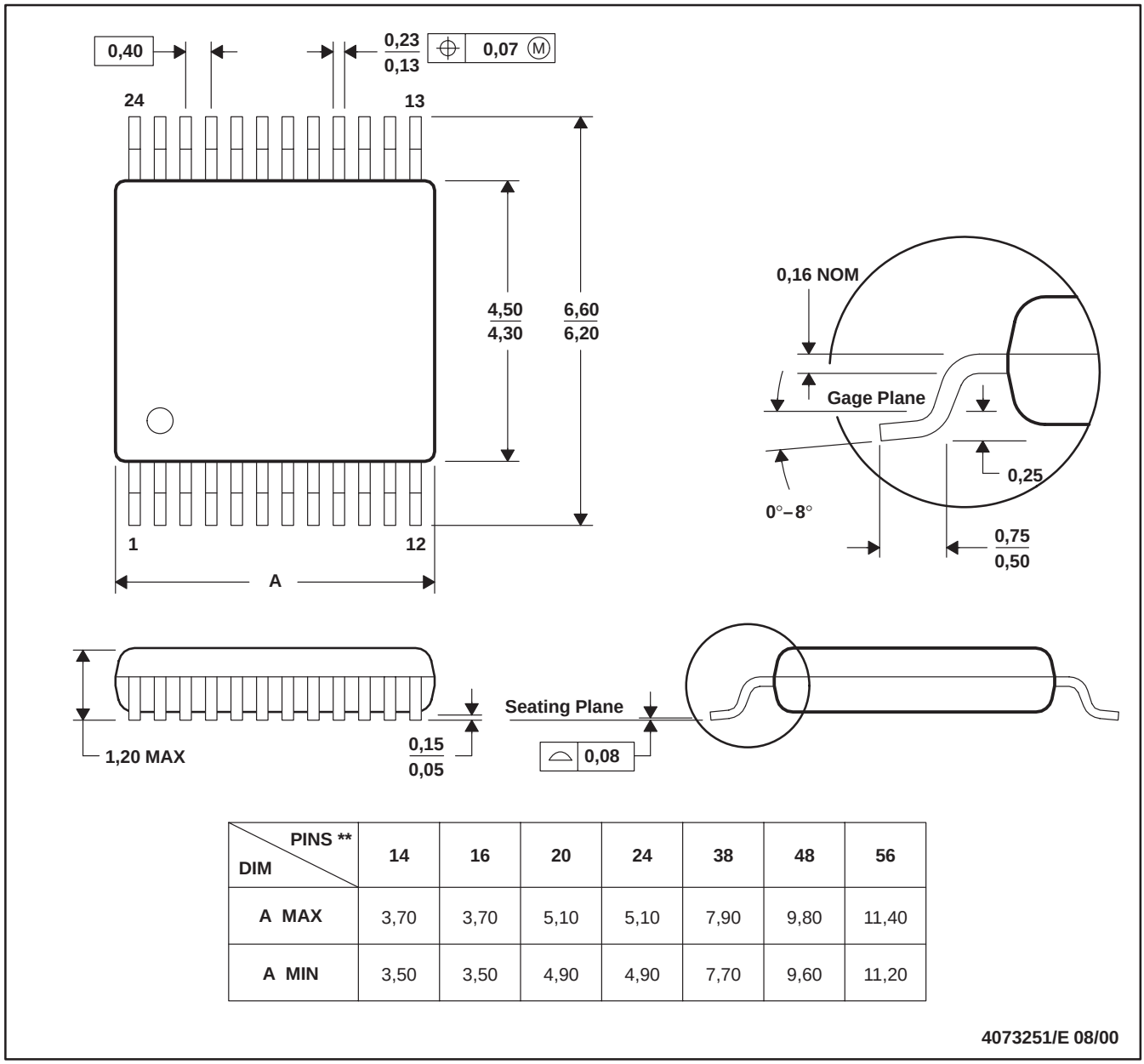



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

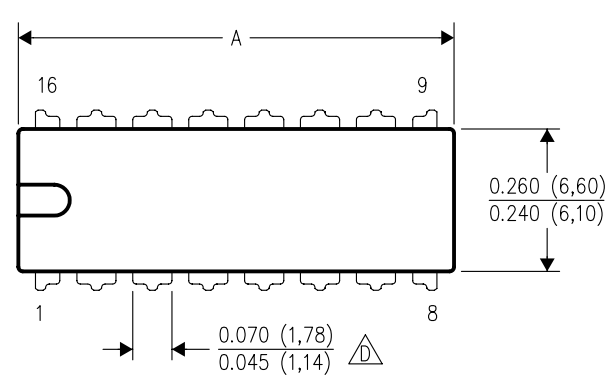
**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

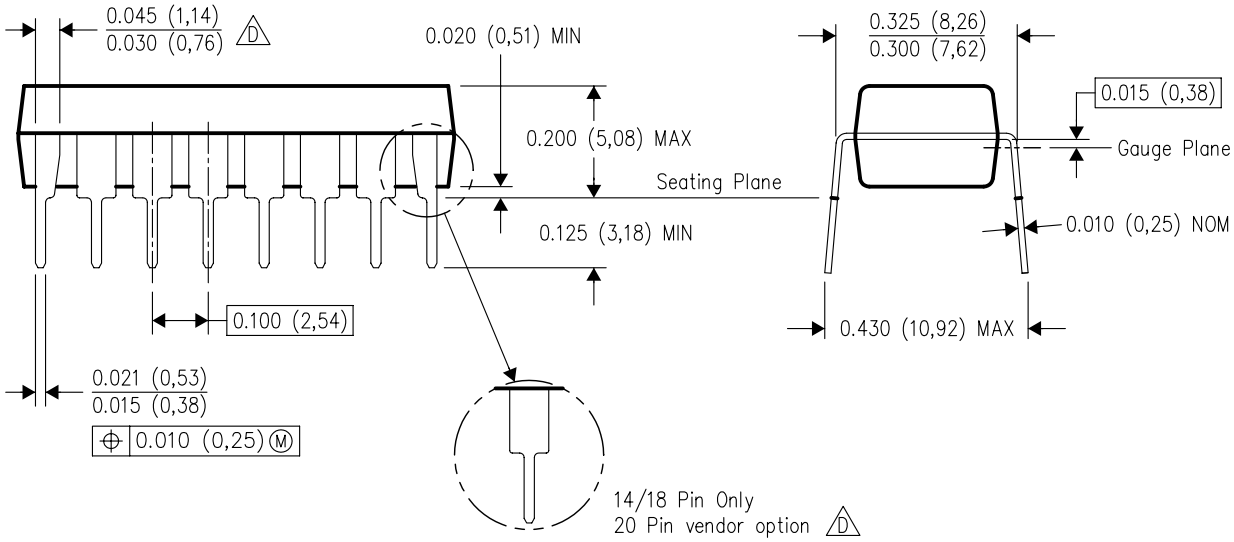
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

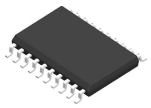



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

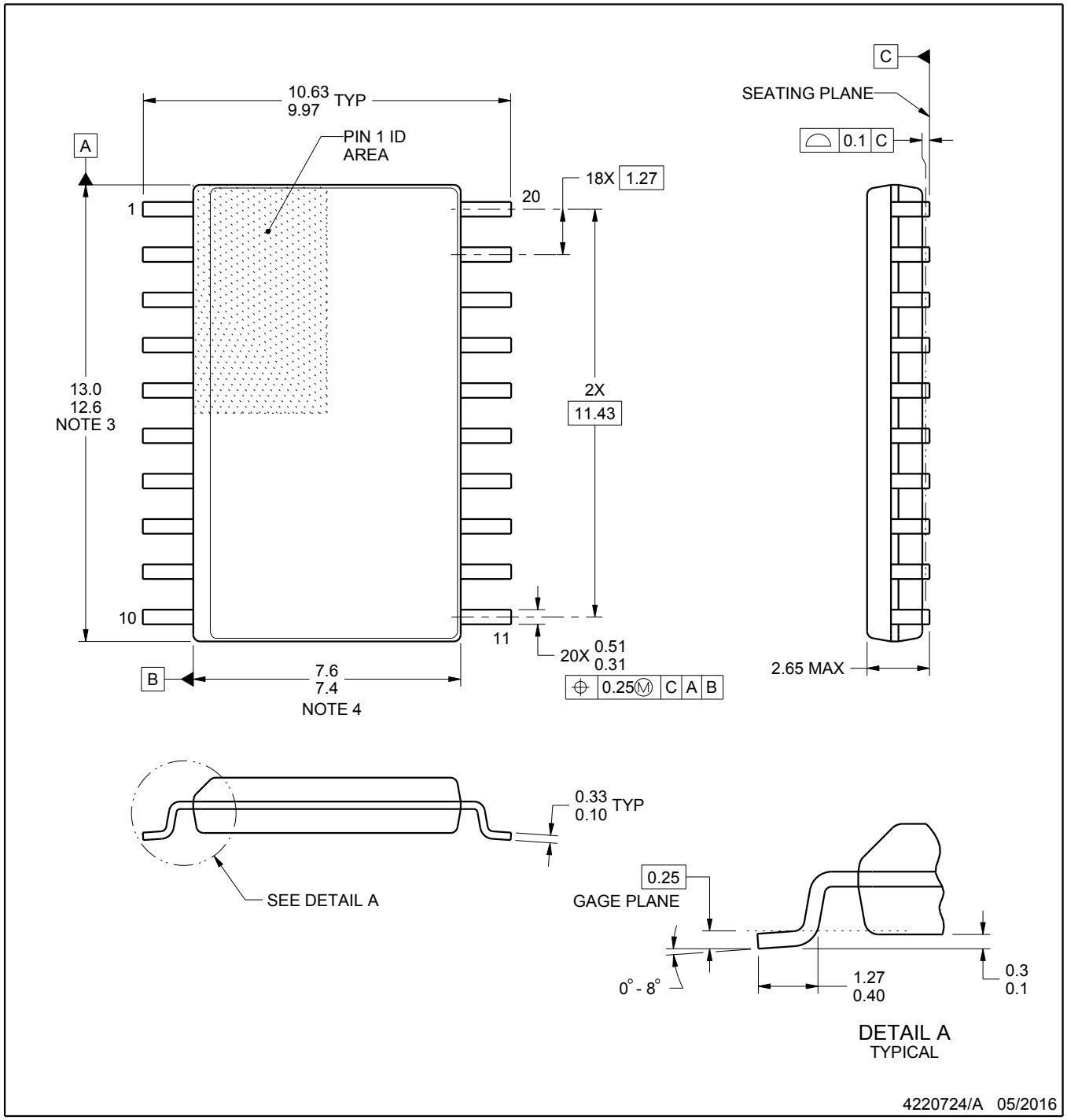


# PACKAGE OUTLINE

## DW0020A

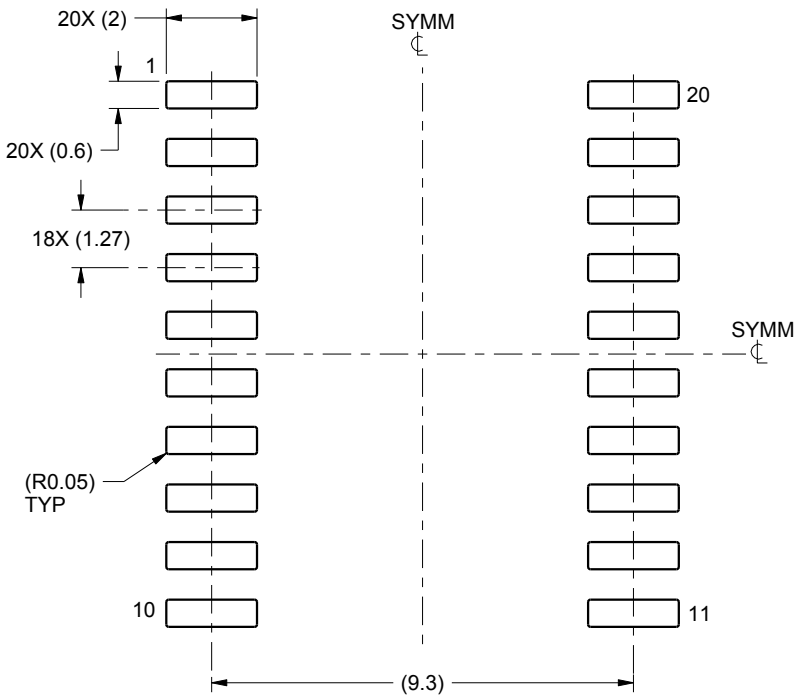
## SOIC - 2.65 mm max height

SOIC

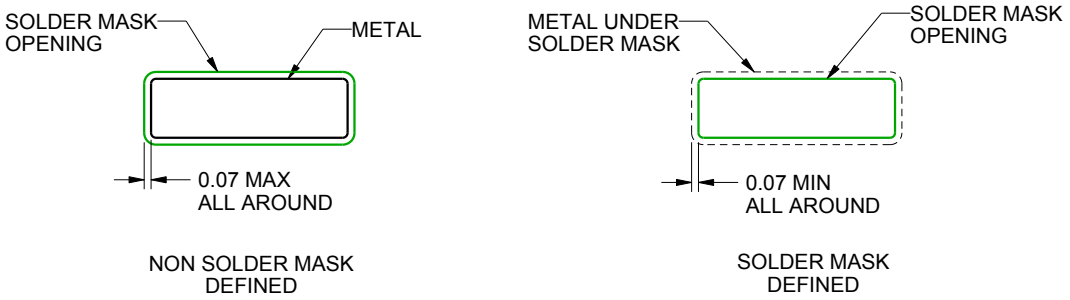



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

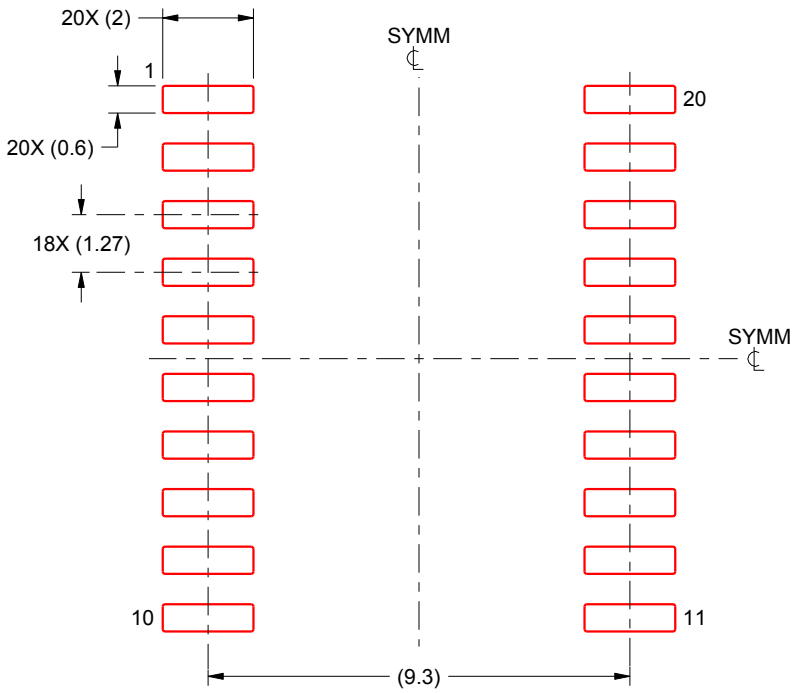



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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