SNx4AHCT240 Octal Inverting Buffers/Drivers With Tri-State Outputs

1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, All parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Network Switches
- Health and Fitness
- Televisions
- Power Infrastructures

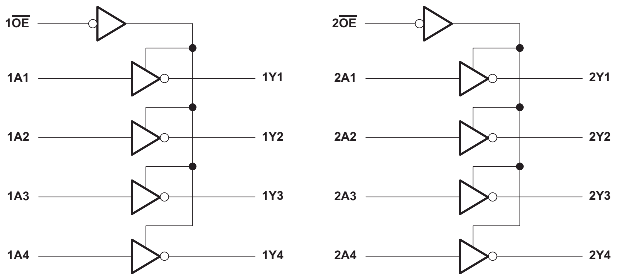
3 Description

The SNx4AHCT240 octal buffers/drivers are designed specifically to improve both the performance and density of tri-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AHCT240	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm x 5.30mm
	NS (SOP, 20)	12.60mm x 7.8mm	12.6mm x 5.30mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm x 4.40mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm x 7.5mm
	N (PDIP, 20)	24.33mm x 9.4mm	25.40mm x 6.35mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

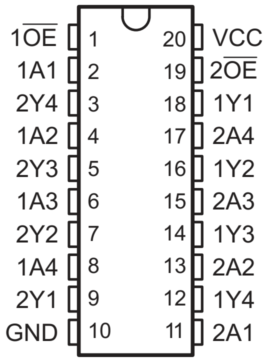


Figure 4-1. SN54AHCT240, J or W Package SN74AHCT240, DB, DGV, DW, N, NS, or PW Package (20) Pin Top View

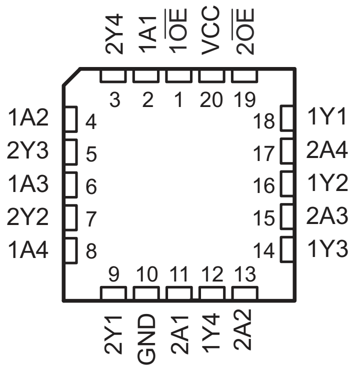


Figure 4-2. SN54AHCT240 FK Package (20) Pin Top View

PIN		I/O	DESCRIPTION
NAME	NO.		
1 $\overline{\text{OE}}$	1	I	Output Enable 1
1A1	2	I	1A1 Input
2Y4	3	O	2Y4 Output
1A2	4	I	1A2 Input
2Y3	5	O	2Y3 Output
1A3	6	I	1A3 Input
2Y2	7	O	2Y2 Output
1A4	8	I	1A4 Input
2Y1	9	O	2Y1 Output
GND	10	—	Ground Pin
2A1	11	I	2A1 Input
1Y4	12	O	1Y4 Output
2A2	13	I	2A2 Input
1Y3	14	O	1Y3 Output
2A3	15	I	2A3 Input
1Y2	16	O	1Y2 Output
2A4	17	I	2A4 Input
1Y1	18	O	1Y1 Output
2 $\overline{\text{OE}}$	19	I	Output Enable 2
V_{CC}	20	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I (2)	Input voltage		–0.5	7	V
V_O (2)	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHCT240		SN74AHCT240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level Input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
T_A	Operating free-air temperature	–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHCT240					UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.1	99.9	54.9	80.4	116.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.9	61.7	41.7	46.9	58.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	53.8	55.2	35.8	47.9	78.7	
Ψ_{JT}	Junction-to-top characterization parameter	19.5	22.6	27.9	19.9	12.6	
Ψ_{JB}	Junction-to-board characterization parameter	53.1	54.8	35.7	47.5	77.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = 25°C			SN54AHCT240		–40°C to 85°C SN74AHCT240		–40°C to 125°C SN74AHCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –50 µA, V_{CC} = 4.5 V	4.4	4.5		4.4		4.4		4.4		V
		I_{OH} = –8 mA, V_{CC} = 4.5 V	3.94			3.8		3.8		3.8		
V_{OL}	Low-level output voltage	I_{OL} = 50 µA, V_{CC} = 4.5 V			0.1		0.1		0.1		0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V			0.36		0.44		0.44		0.44	
I_{OZ}	High-impedance-state output current	V_O = V_{CC} or GND V_{CC} = 5.5 V			±0.25		±2.5		±2.5		±2.5	µA
I_I	Inflection-point current	V_I = 5.5 V or GND V_{CC} = 0 V to 5.5 V			±0.1		±1(1)		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND I_O = 0,V_{CC} = 5.5 V			4		40		40		40	µA
ΔI_{CC} (2)	Supply current change	One input at 3.4 V other inputs at V_{CC} or GND V_{CC} = 5.5 V			1.35		1.5		1.5		1.5	mA
C_i	Input capacitance	V_I = V_{CC} or GND V_{CC} = 5.5 V		2.5	10				10		10	pF

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = 25°C			SN54AHCT240		–40°C to 85°C SN74AHCT240		–40°C to 125°C SN74AHCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
C_o	Output capacitance	V_O = V_{CC} or GND V_{CC} = 5.5 V		3								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see *Section Parameter Measurement Information* section)

PARAMETER		TEST CONDITIONS		T_A = 25°C		SN54AHCT240		–40°C to 85°C SN74AHCT240		–40°C to 125°C SN74AHCT240		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time (low-to-high output)	A-to-Y	C_L = 15 pF	5.4(1)	7.4(1)	1(1)	8.5(1)	1	8.5	1	9.5	ns
t_{PHL}	Propagation delay time (high-to-low output)			5.4(1)	7.4(1)	1(1)	8.5(1)	1	8.5	1	9.5	
t_{PZH}	Enable time (to the high level)	$\overline{OE}$-to-Y	C_L = 15 pF	7.7(1)	10.4(1)	1(1)	12(1)	1	12	1	13	ns
t_{PZL}	Enable time (to the low level)			7.7(1)	10.4(1)	1(1)	12(1)	1	12	1	13	
t_{PHZ}	Disable time (from high level)	$\overline{OE}$-to-Y	C_L = 15 pF	8.3(1)	10.4(1)	1(1)	12(1)	1	12	1	13	ns
t_{PLZ}	Disable time (from low level)			8.3(1)	10.4(1)	1(1)	12(1)	1	12	1	13	
t_{PLH}	Propagation delay time (low-to-high output)	A-to-Y	C_L = 50 pF	5.9	8.4	1	9.5	1	9.5	1	10.5	ns
t_{PHL}	Propagation delay time (high-to-low output)			5.9	8.4	1	9.5	1	9.5	1	10.5	
t_{PZH}	Enable time (to the high level)	$\overline{OE}$-to-Y	C_L = 50 pF	8.2	11.4	1	13	1	13	1	14	ns
t_{PZL}	Enable time (to the low level)			8.2	11.4	1	13	1	13	1	14	
t_{PHZ}	Disable time (from high level)	$\overline{OE}$-to-Y	C_L = 50 pF	8.8	11.4	1	13	1	13	1	14	ns
t_{PLZ}	Disable time (from low level)			8.8	11.4	1	13	1	13	1	14	
$t_{sk(o)}$	Skew (time), output		C_L = 50 pF		1(2)		1		1		1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		SN74AHCT240			UNIT
		MIN	TYP	MAX	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

5.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	10	pF

5.9 Typical Characteristics

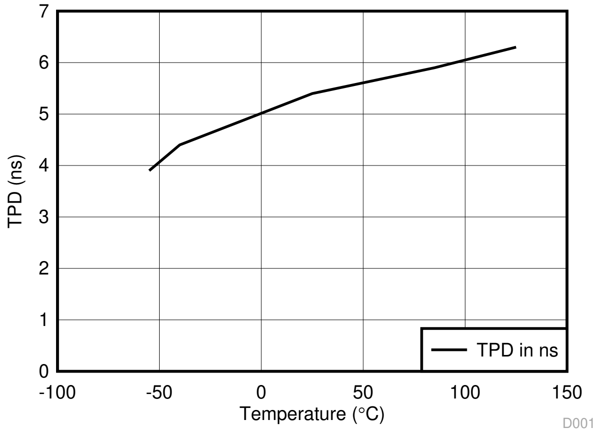


Figure 5-1. TPD vs Temperature

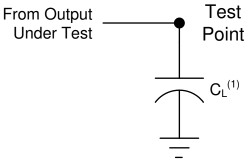
Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR ≤ 1 MHz
- Z_O = 50 Ω
- t_r ≤ 3 ns
- t_f ≤ 3 ns

Note

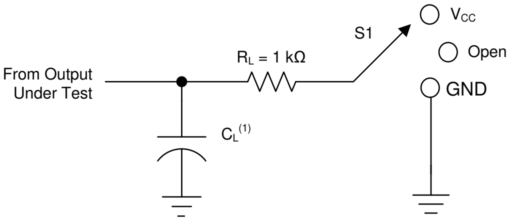
All parameters and waveforms are not applicable to all devices.



A. C_L includes probe and jig capacitance.

B. The outputs are measured one at a time, with one transition per measurement.

Figure 6-1. Load Circuit For Totem-Pole Outputs



A. C_L includes probe and jig capacitance.

B. The outputs are measured one at a time, with one transition per measurement.

Figure 6-2. Load Circuit For Tri-State And Open-Drain Outputs

Table 6-1. Loading Conditions For Parameter

TEST	S1
t_{PLH} (1), t_{PHL} (1)	Open
t_{PLZ} (3), t_{PZL} (2)	V_{CC}
t_{PHZ} (3), t_{PZH} (2)	GND
Open drain	V_{CC}

(1) t_{PLH} and t_{PHL} are the same as t_{pd}.
(2) t_{PZL} and t_{PZH} are the same as t_{en}.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

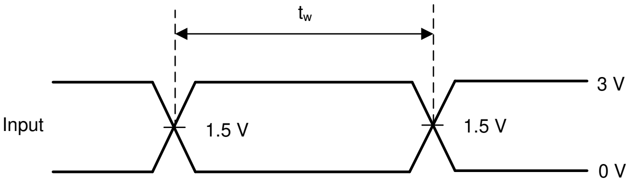
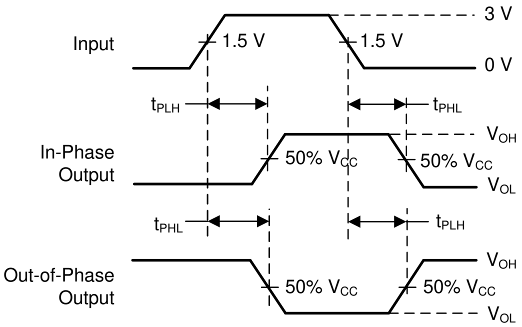


Figure 6-3. Voltage Waveforms Pulse Durations



A. The outputs are measured one at a time, with one transition per measurement.

Figure 6-4. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

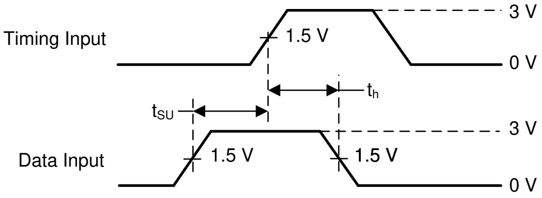
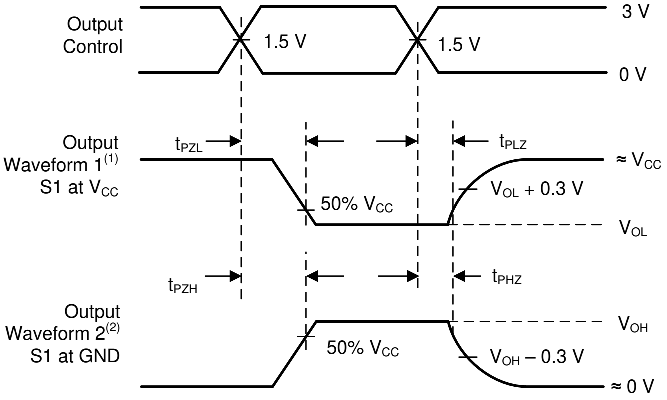


Figure 6-5. Voltage Waveforms Setup And Hold Times



A. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
B. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. The outputs are measured one at a time, with one transition per measurement.

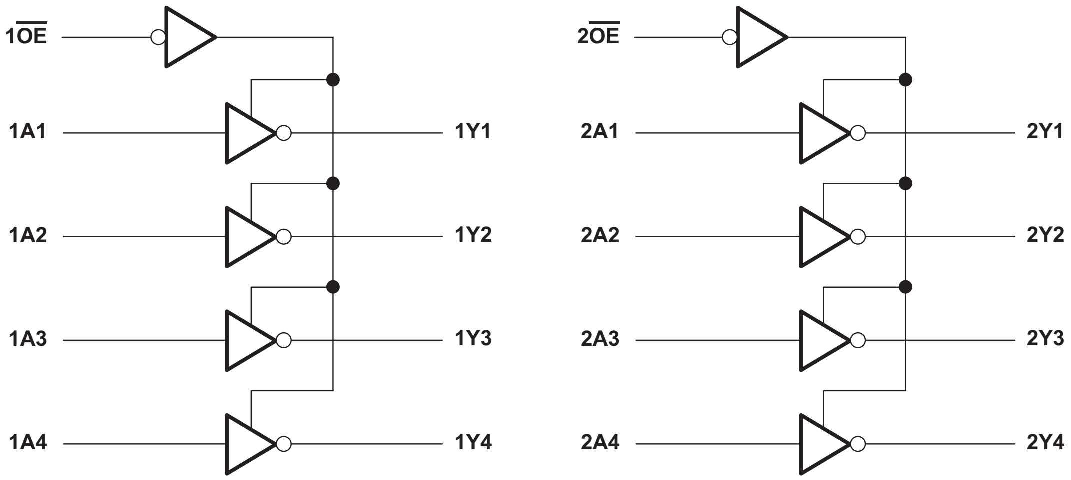
Figure 6-6. Voltage Waveforms Enable And Disable Times Low- and High-Level Enabling

6 Detailed Description

6.1 Overview

The SN74AHCT240 devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram



6.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows up-voltage translation from 3.3 V to 5 V
  - Inputs accept V_{IH} levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-voltage compatible

6.4 Device Functional Modes

Table 6-1. Function Table
(Each 4-bit Inverting Buffer/Driver)

INPUTS		OUTPUT Y
$\overline{OE}$	**A**	
L	H	L
L	L	H
H	X	Z

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The SNx4AHCT240 device is a low-drive CMOS device that may be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH}. This feature makes the SNx4AHCT240 device ideal for translating up from 3.3 V to 5 V. Figure 7-1 shows this type of translation.

7.2 Typical Application

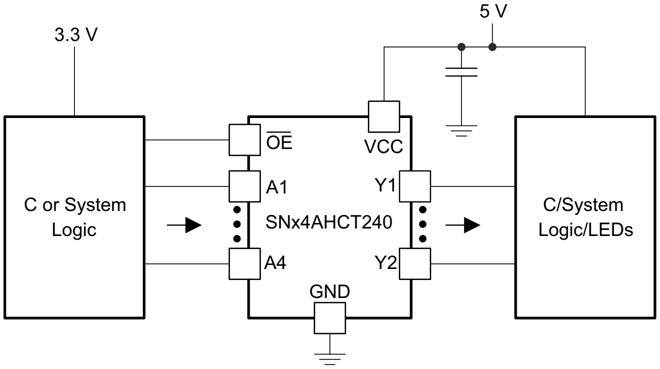


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Figure 7-1. Application Diagram

7.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

7.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
    - For rise time and fall time specifications, see Δt/ΔV in the *Section 5.3* table.
    - For specified high and low levels, see V_{IH} and V_{IL} in the *Section 5.3* table.
    - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions:
    - Load currents should not exceed 25 mA per output and 75 mA total for the part.
    - Outputs should not be pulled above V_{CC}.

7.2.3 Application Curves

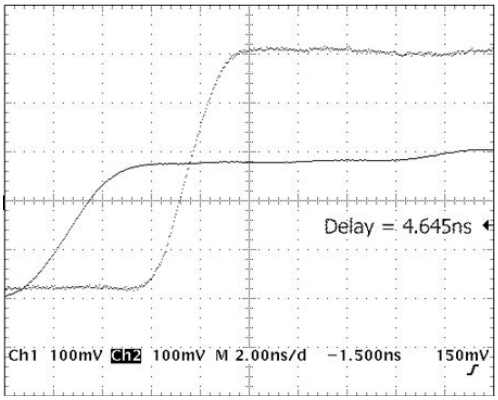


Figure 7-2. Application Scope Capture

7.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

7.4 Layout

7.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Such examples are when only two inputs of a triple-input AND gate are used, or only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.4.2 Layout Example

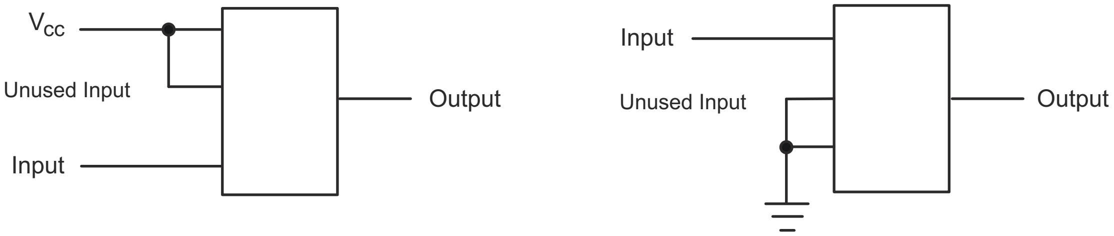


Figure 7-3. Layout Diagram

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT240	Click here	Click here	Click here	Click here	Click here
SN74AHCT240	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision O (July 2024) to Revision P (January 2025) **Page**

- Updated HBM and CDM values in *ESD Ratings* table.. 4

Changes from Revision N (January 2018) to Revision O (July 2024) **Page**

- Added package size to *Device Information* table.. 1
- Updated RθJA values: PW = 105.4 to 116.8, DW = 83.0 to 81.1; Updated PW and DW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W 5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9680601Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601Q2A SNJ54AHCT240FK
5962-9680601QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601QRA SNJ54AHCT240J
5962-9680601QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601QSA SNJ54AHCT240W
SN74AHCT240DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB240
SN74AHCT240DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB240
SN74AHCT240DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB240
SN74AHCT240DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	AHCT240
SN74AHCT240DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT240
SN74AHCT240DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT240
SN74AHCT240N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT240N
SN74AHCT240N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT240N
SN74AHCT240NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT240
SN74AHCT240NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT240
SN74AHCT240PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	HB240
SN74AHCT240PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB240
SN74AHCT240PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB240
SN74AHCT240PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB240
SN74AHCT240RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT240
SNJ54AHCT240FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601Q2A SNJ54AHCT240FK

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHCT240FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601Q2A SNJ54AHCT 240FK
SNJ54AHCT240J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601QRA SNJ54AHCT240J
SNJ54AHCT240J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601QRA SNJ54AHCT240J
SNJ54AHCT240W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601QSA SNJ54AHCT240W
SNJ54AHCT240W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680601QSA SNJ54AHCT240W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54AHCT240, SN74AHCT240 :

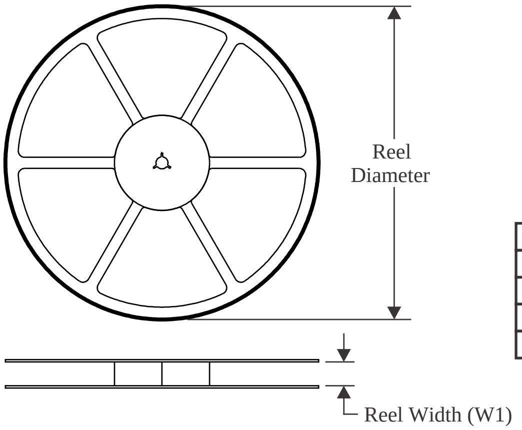
- Catalog : SN74AHCT240
- Automotive : SN74AHCT240-Q1, SN74AHCT240-Q1
- Military : SN54AHCT240

NOTE: Qualified Version Definitions:

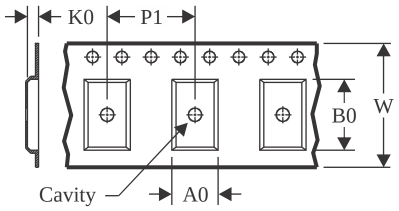
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

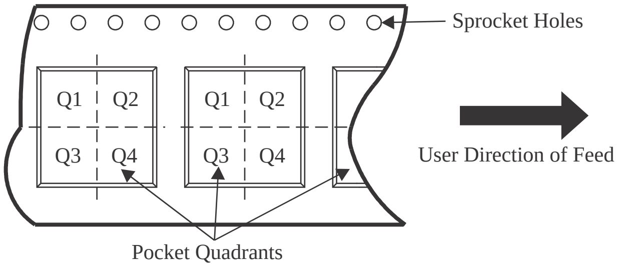


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

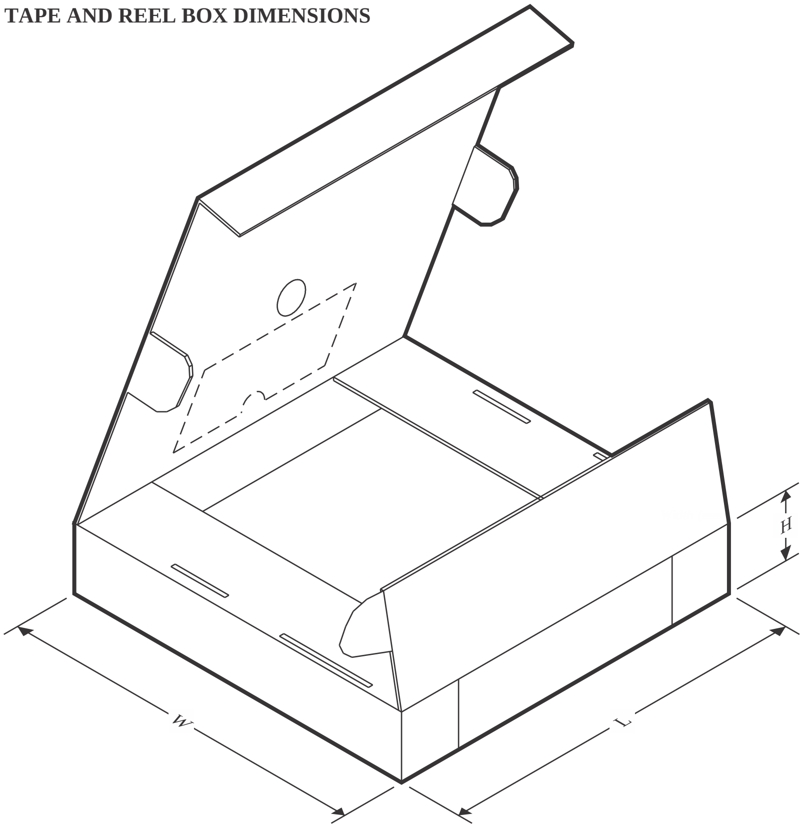
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT240DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHCT240DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHCT240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT240RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

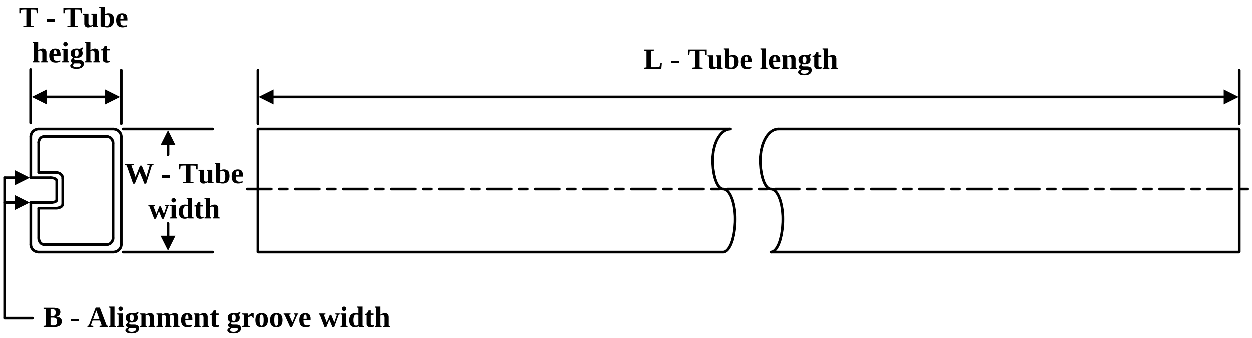
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

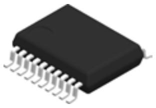
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT240DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHCT240DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHCT240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT240NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHCT240PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT240RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

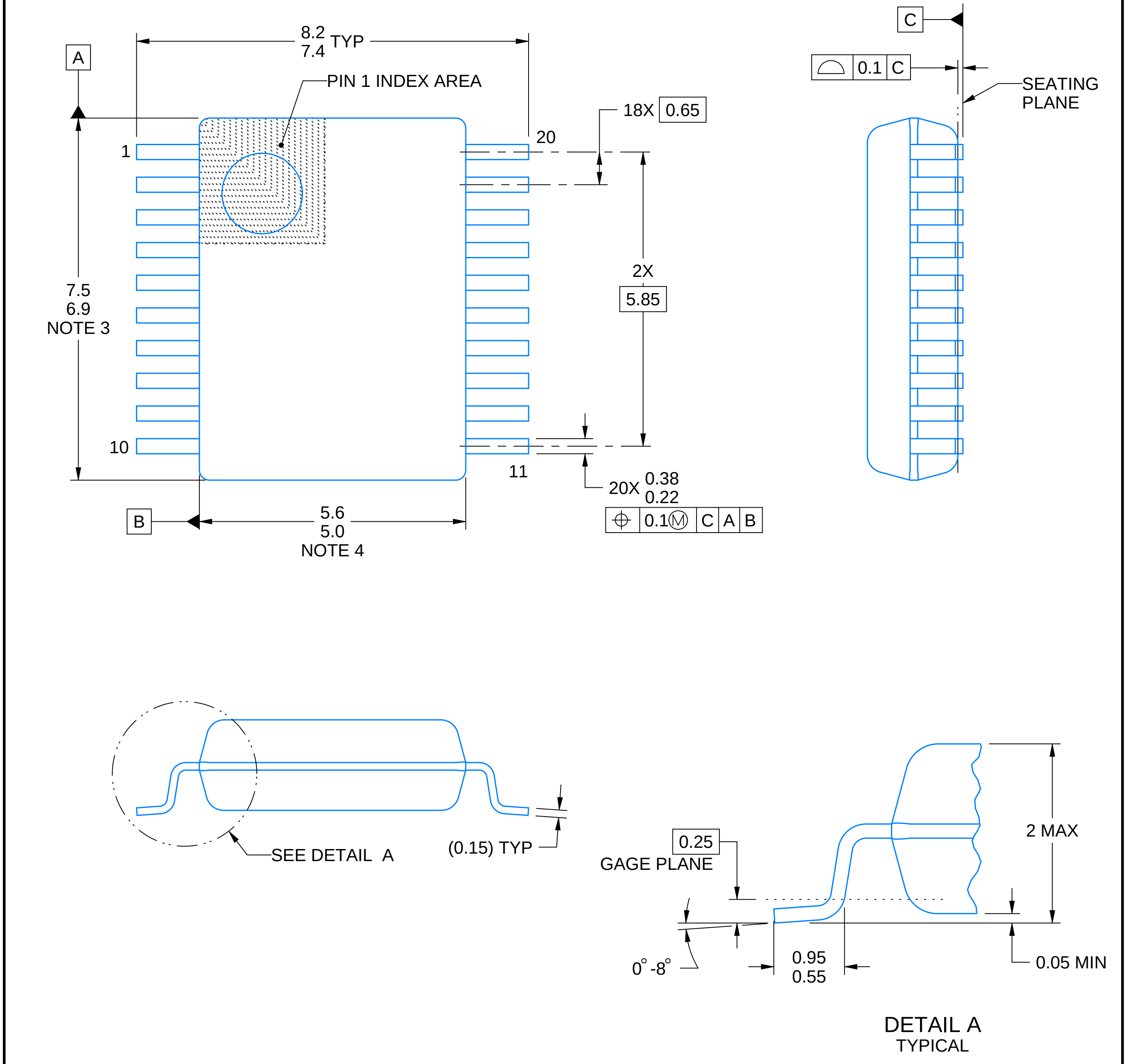
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9680601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9680601QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT240N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHCT240N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT240FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT240W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHCT240W.A	W	CFP	20	25	506.98	26.16	6220	NA



PACKAGE OUTLINE

SSOP - 2 mm max height

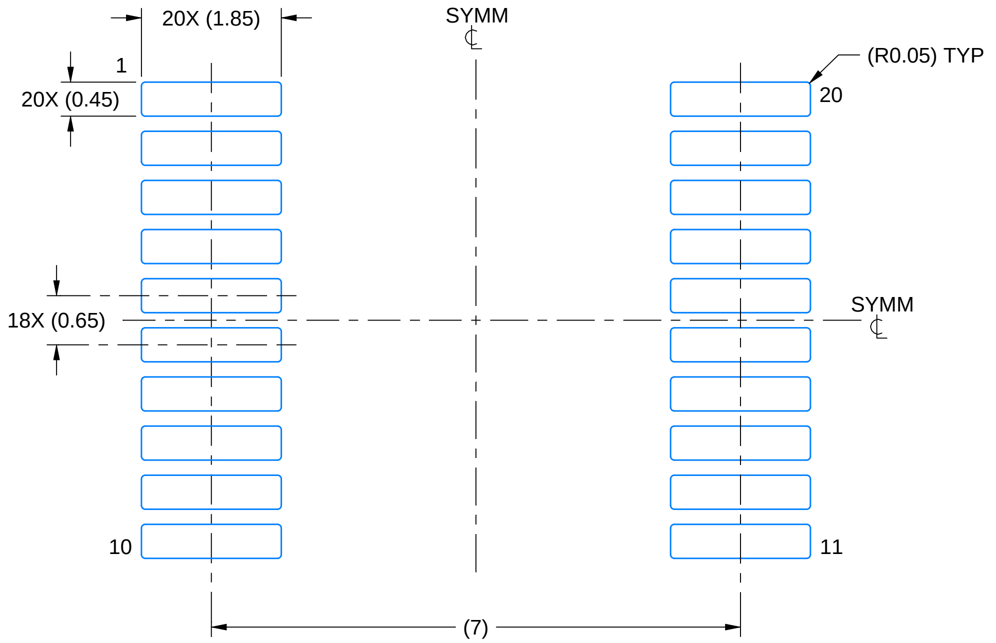
SMALL OUTLINE PACKAGE



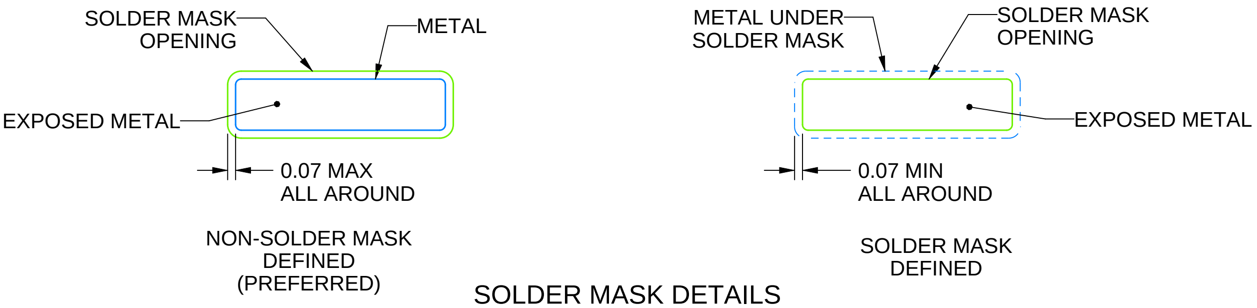
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

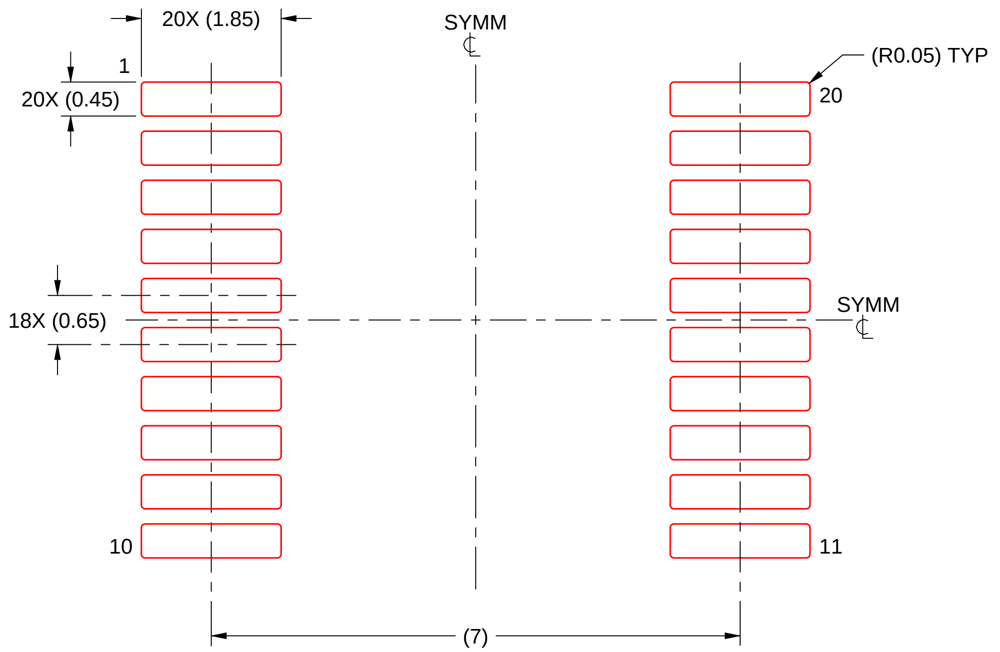


SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

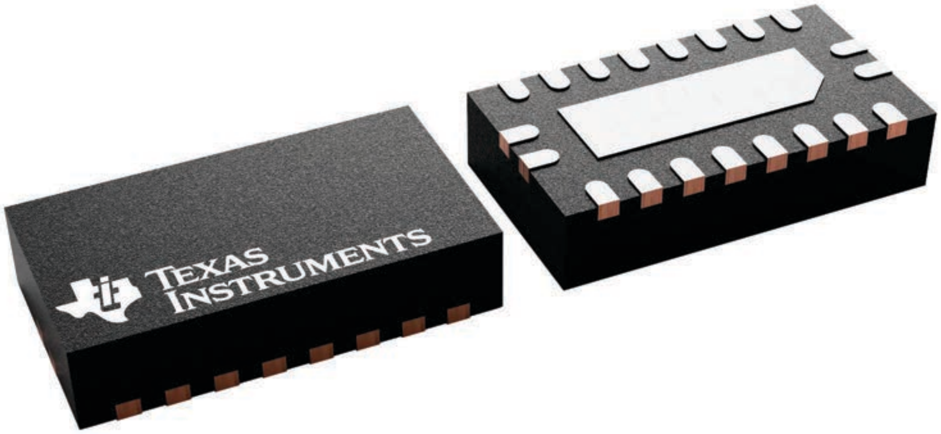
RKS 20

VQFN - 1 mm max height

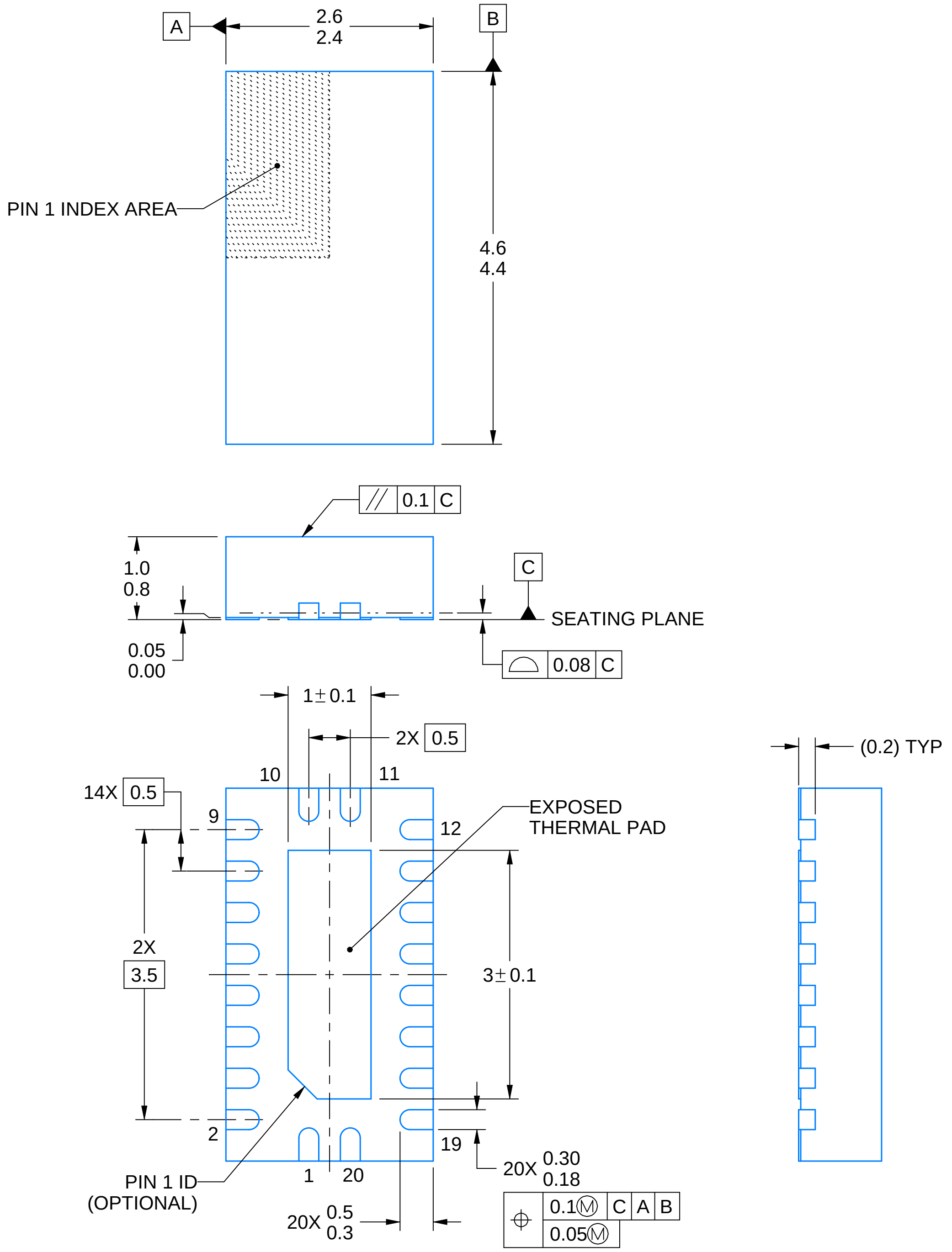
2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

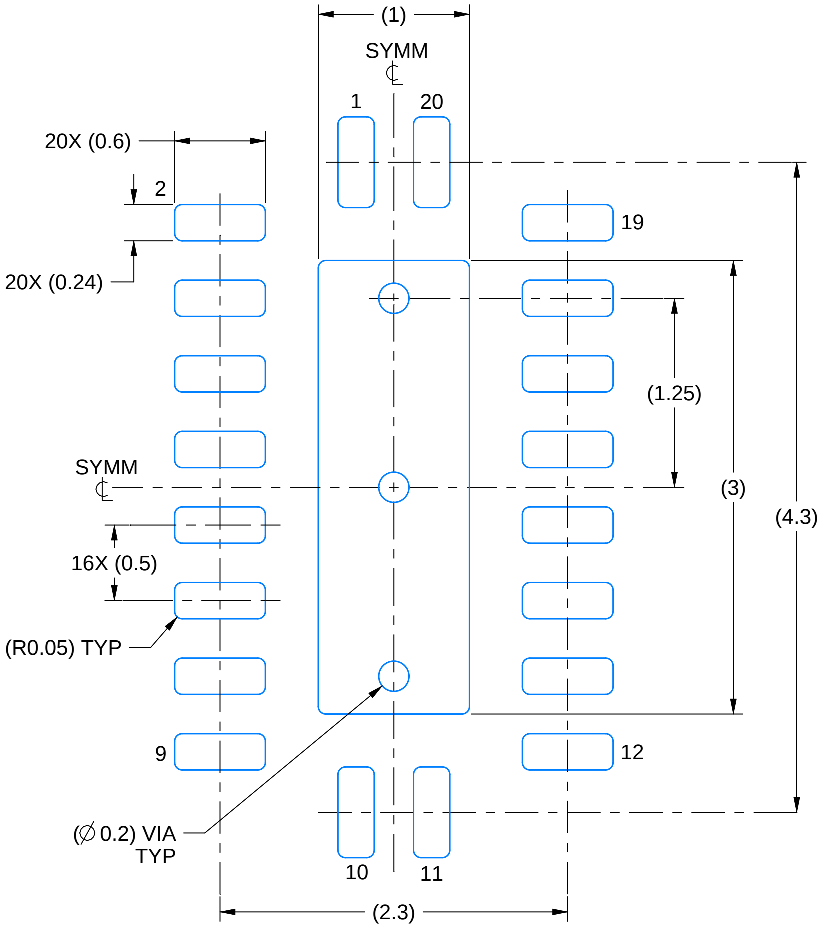


4226872/A

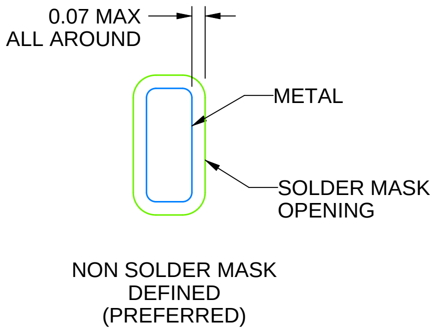


NOTES:

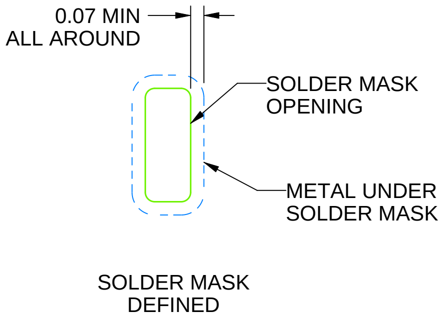
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

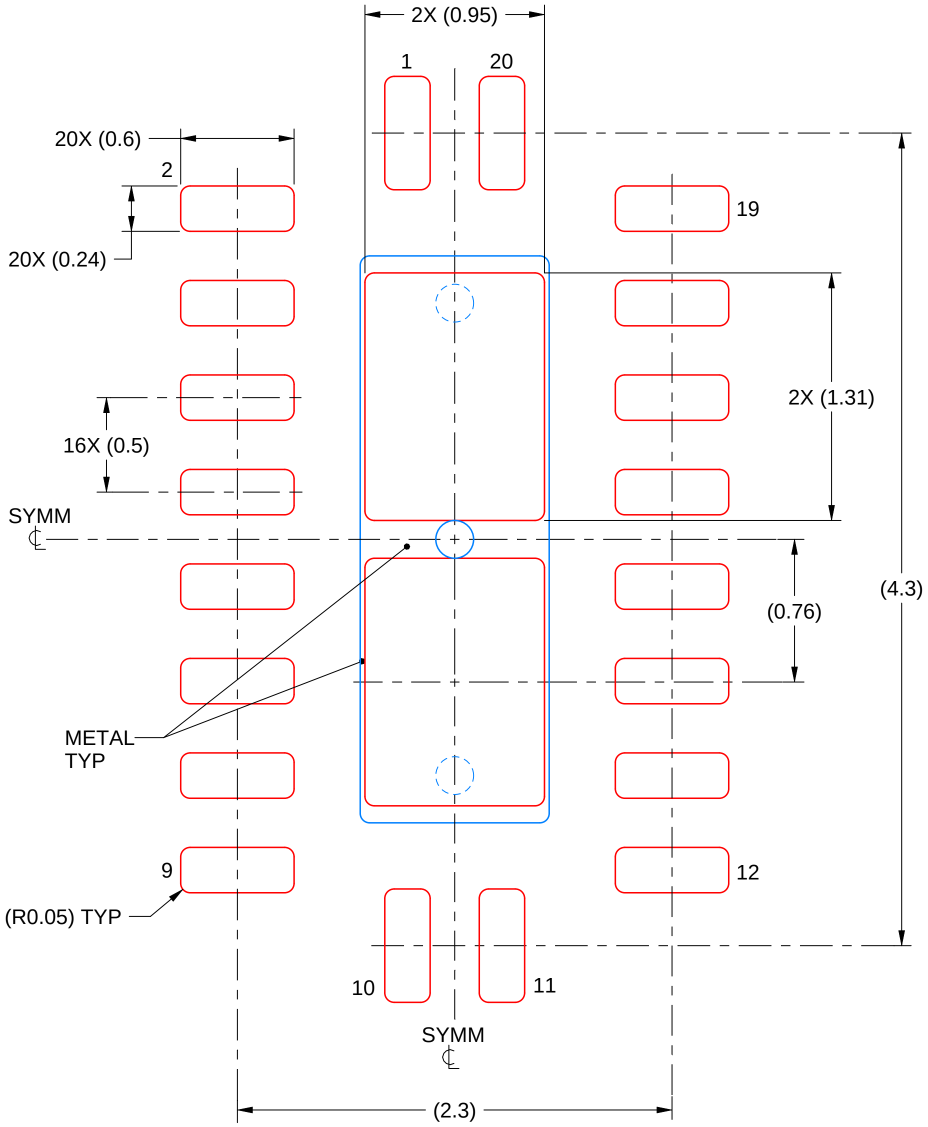


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

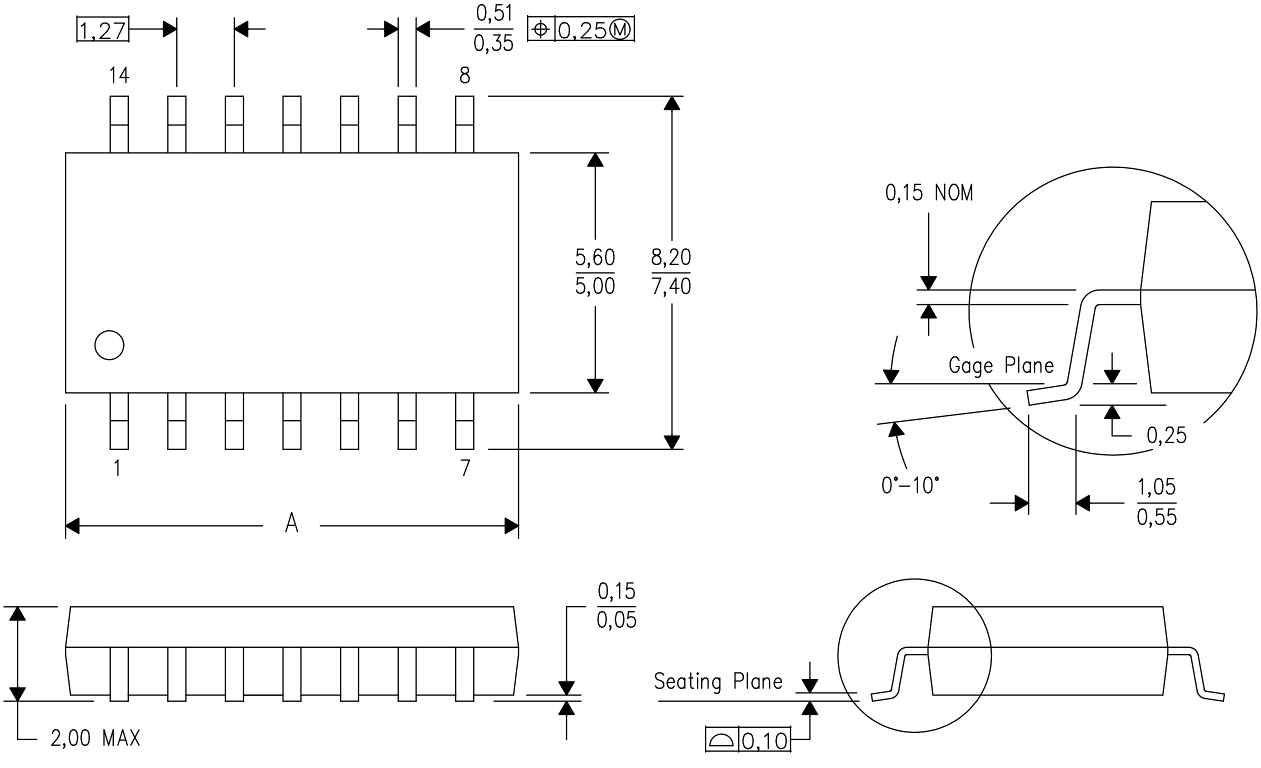
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



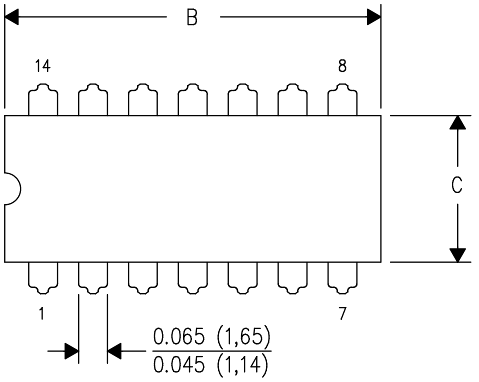
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

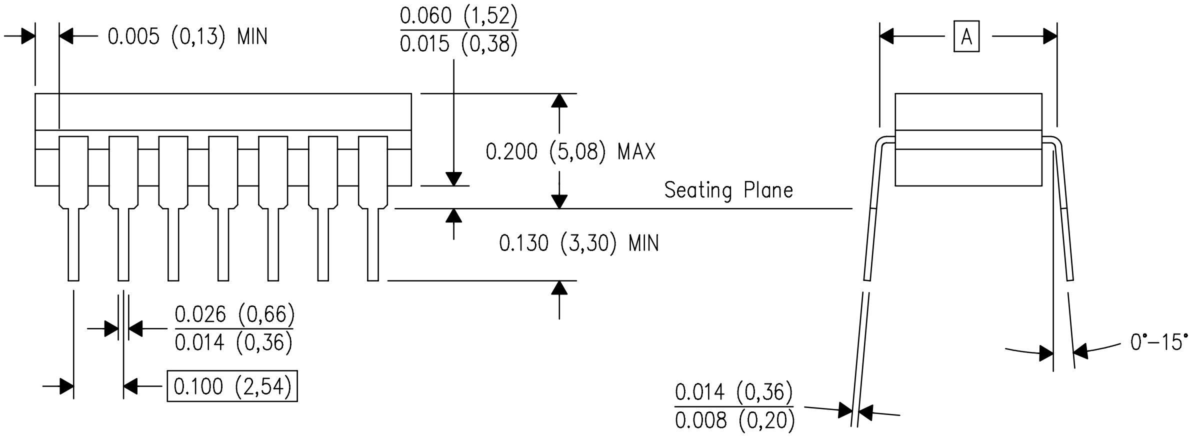
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

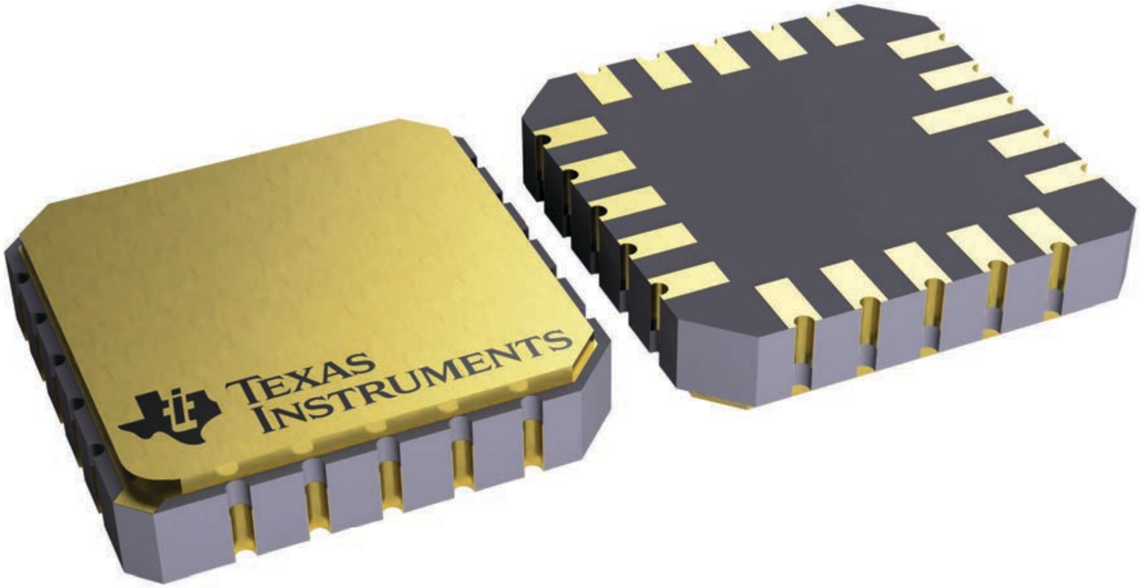
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

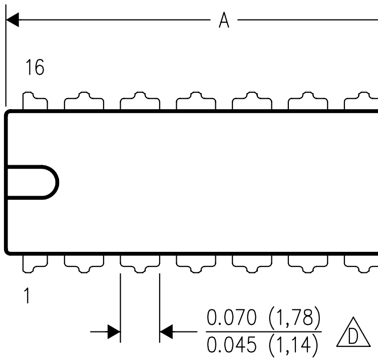
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



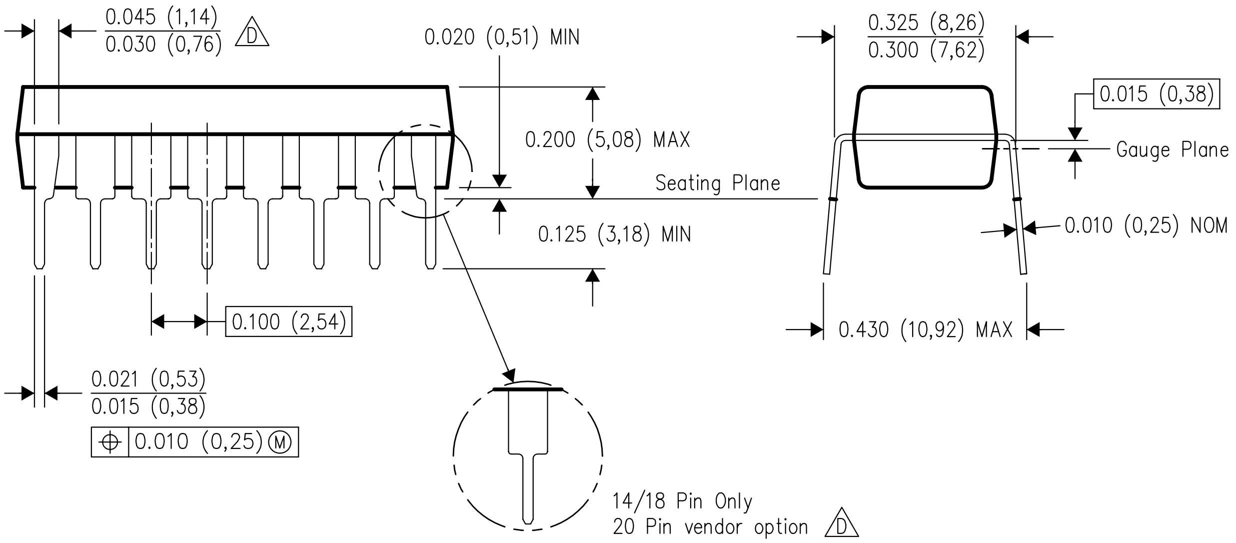
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

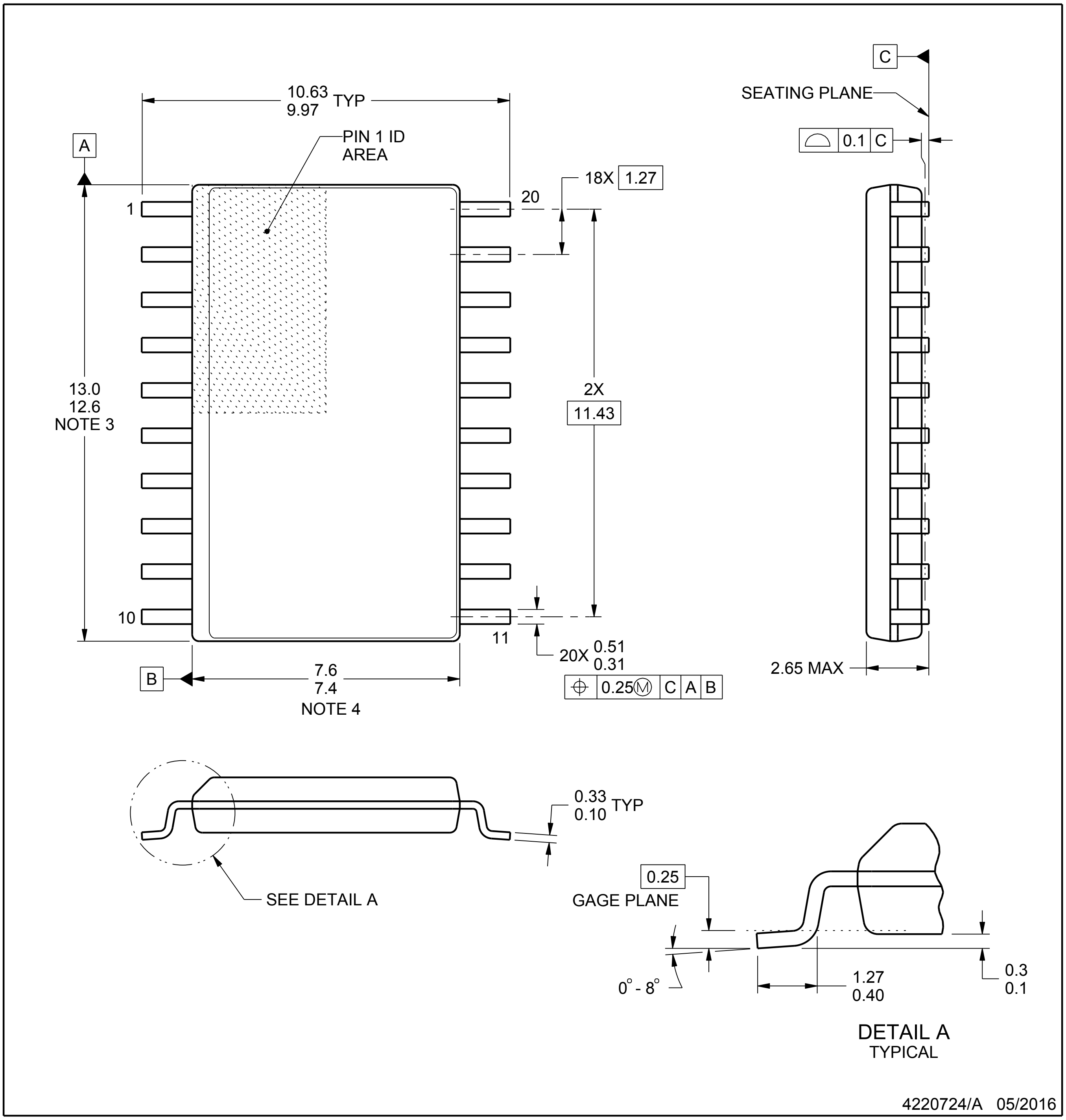


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



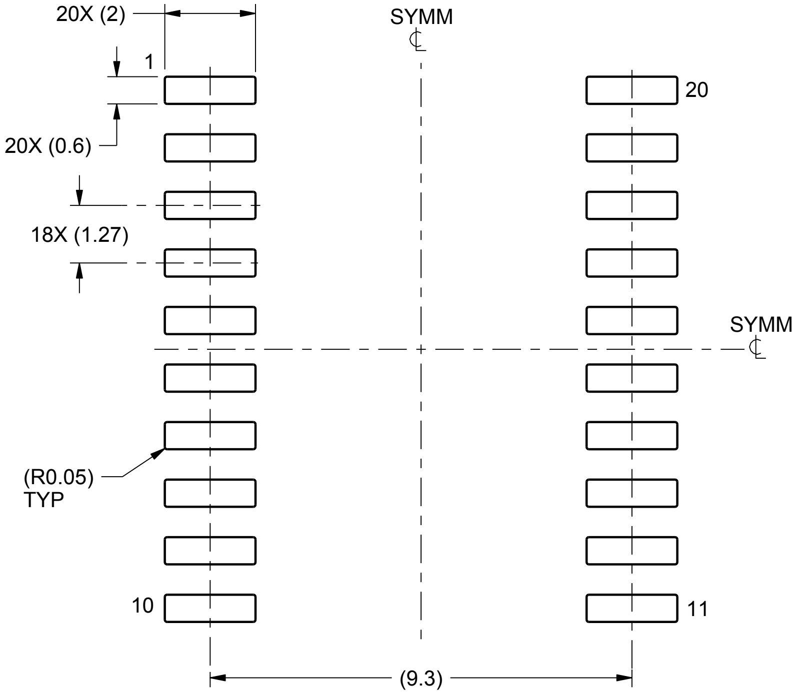
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

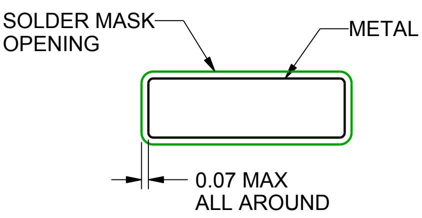


NOTES:

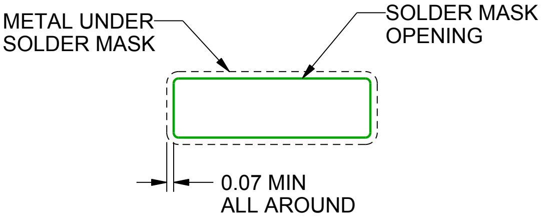
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED



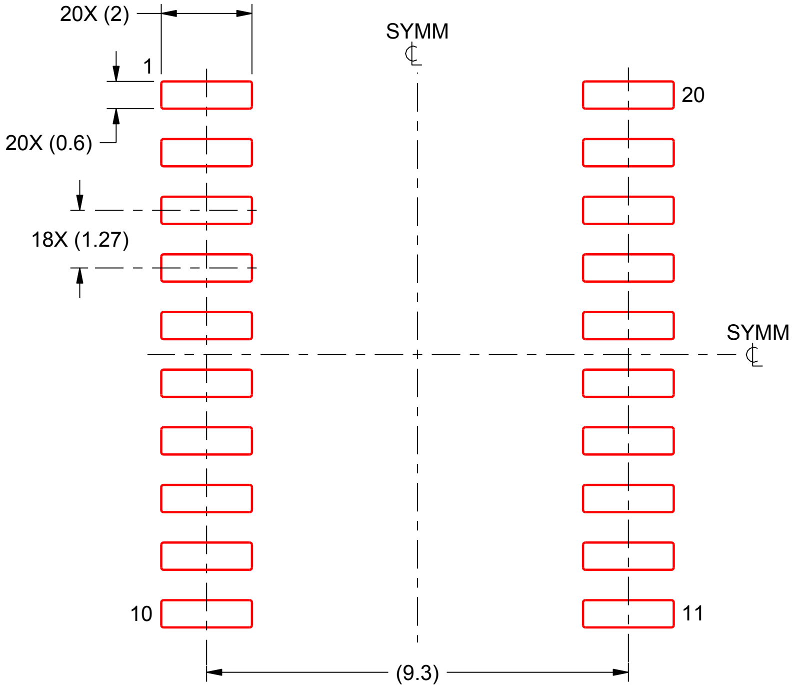
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



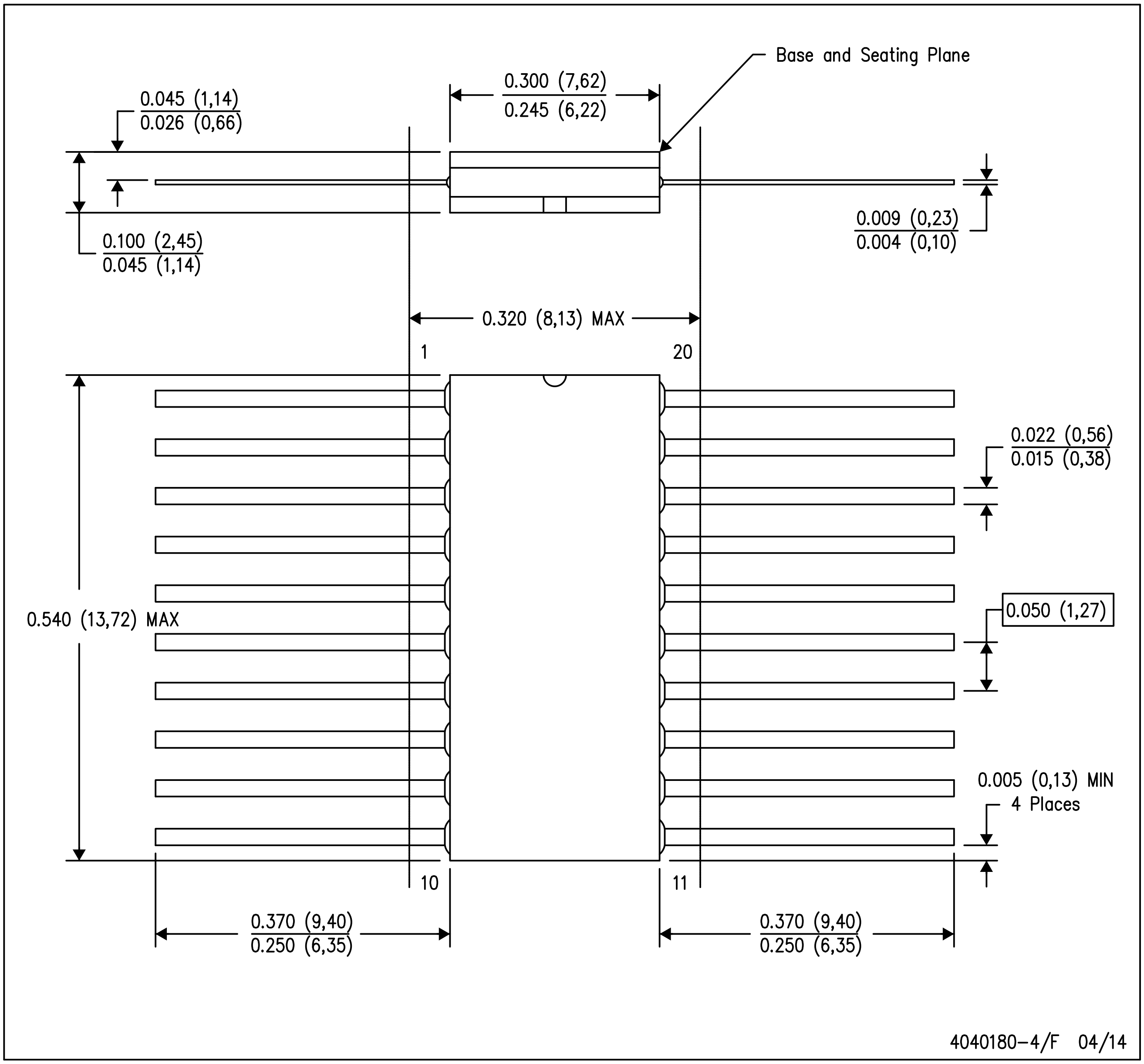
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

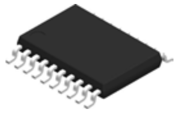
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

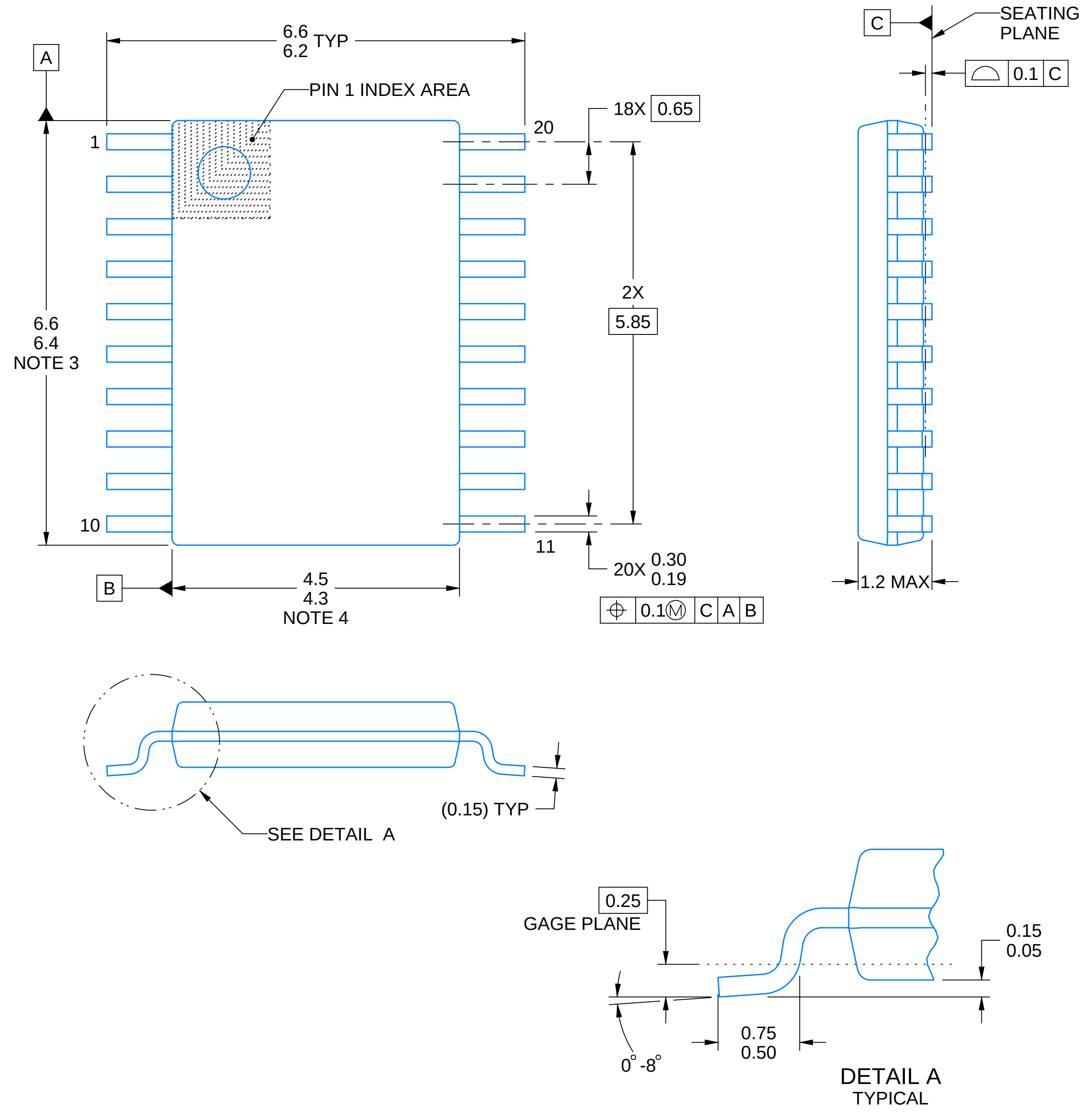
PACKAGE OUTLINE



PW0020A

TSSOP - 1.2 mm max height

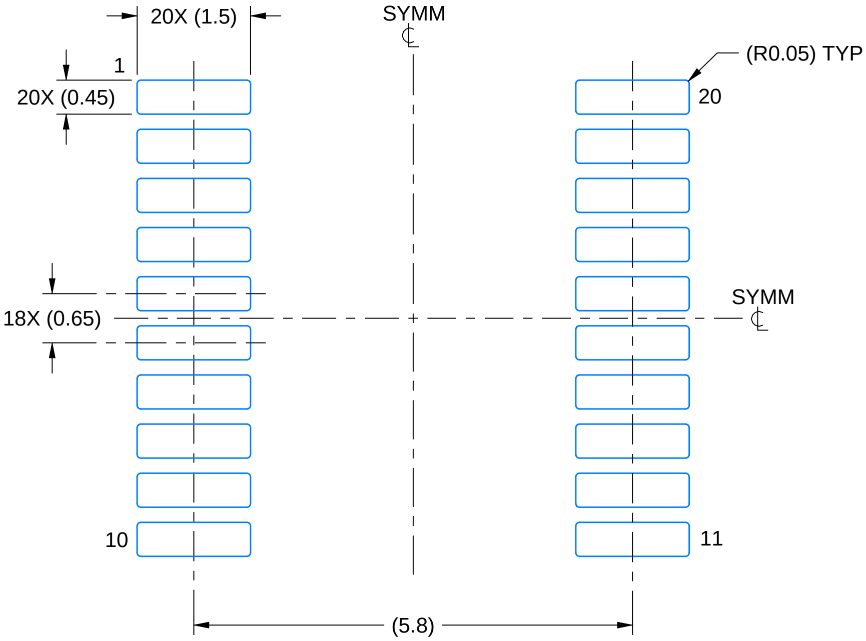
SMALL OUTLINE PACKAGE



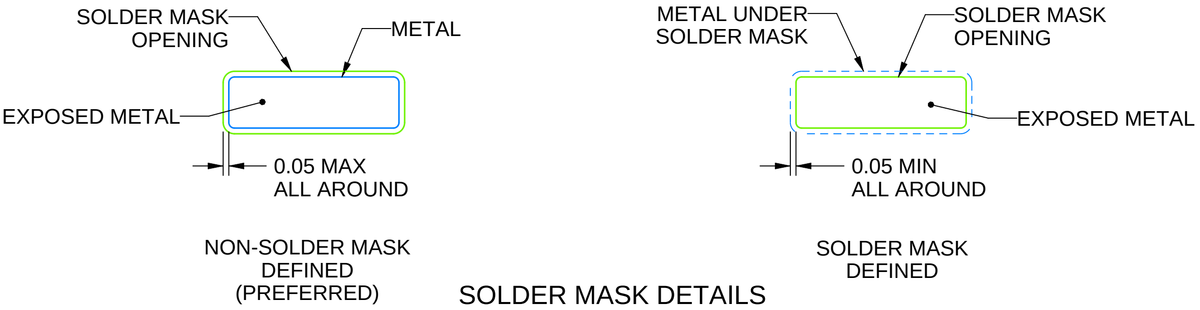
4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

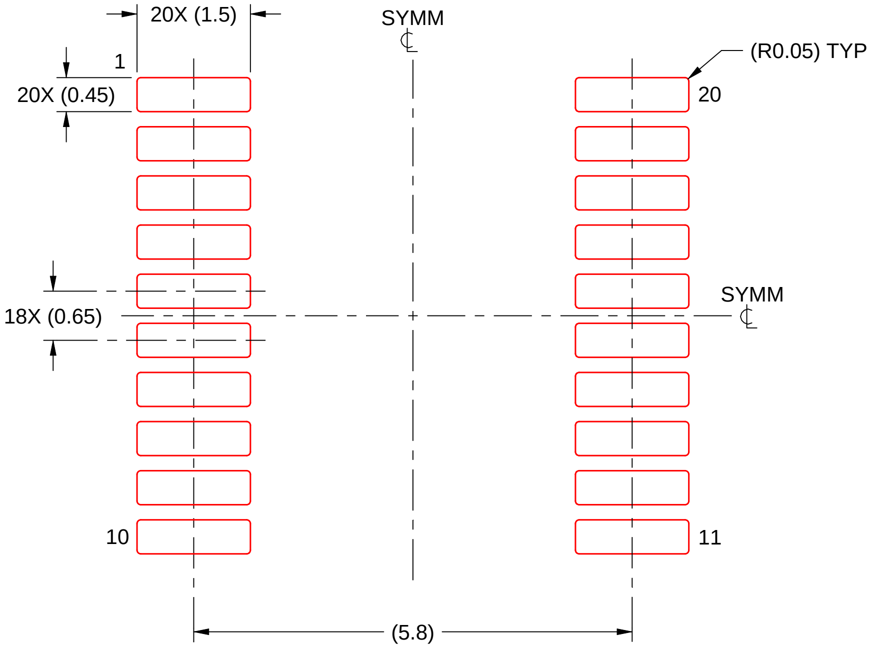


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

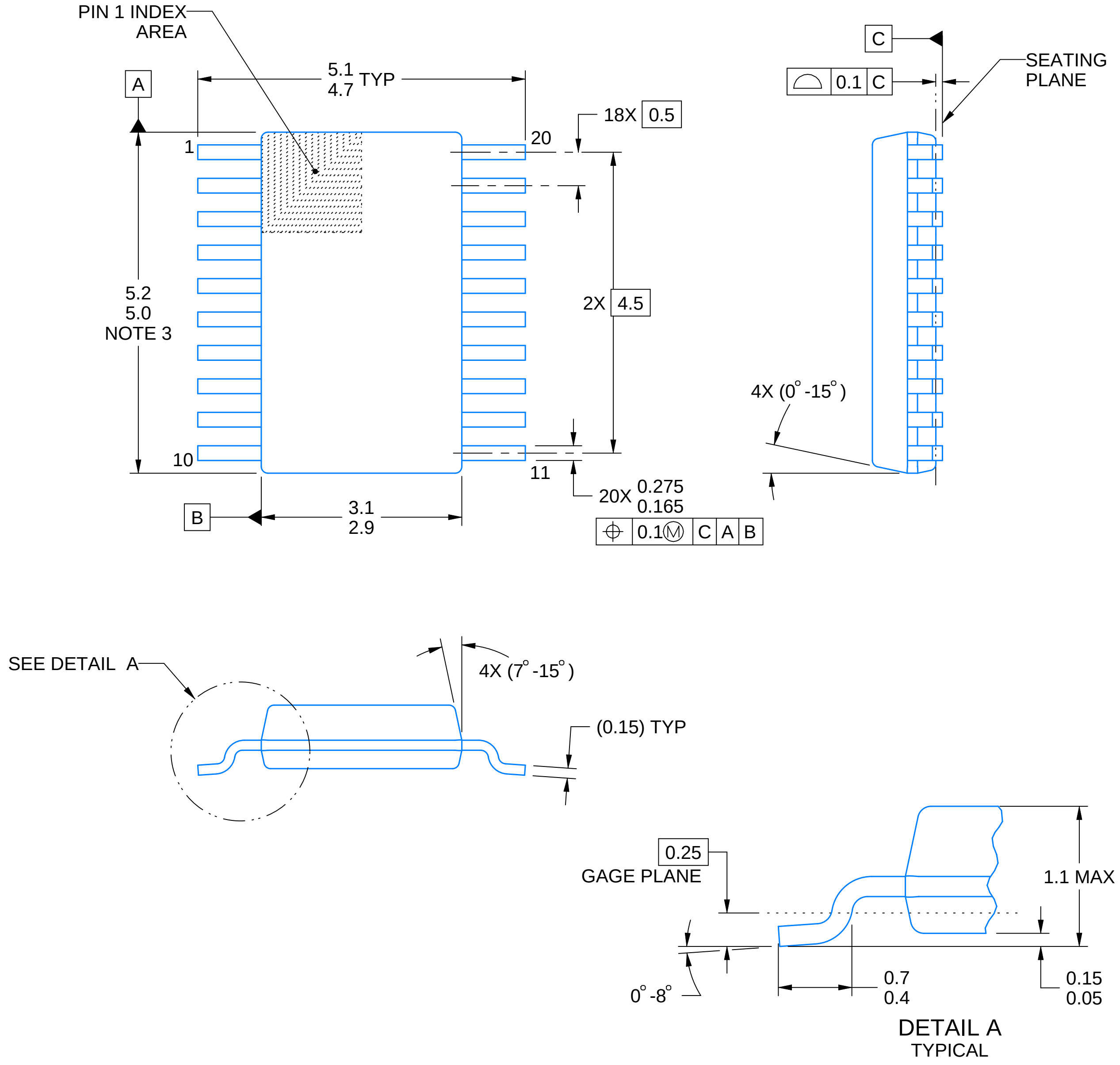


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

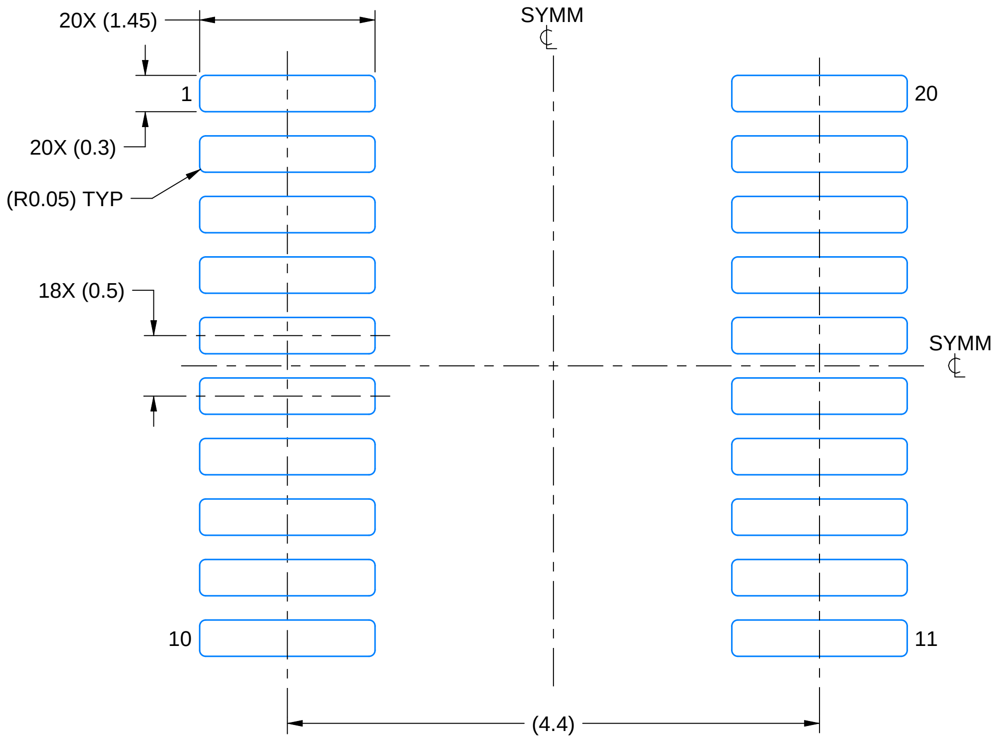


4226367/A 10/2020

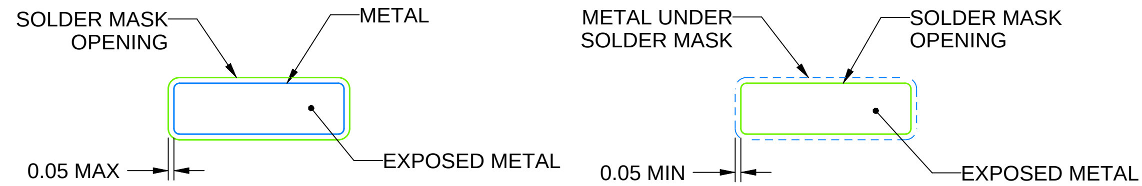
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X



NON-SOLDER MASK
DEFINED
(PREFERRED)

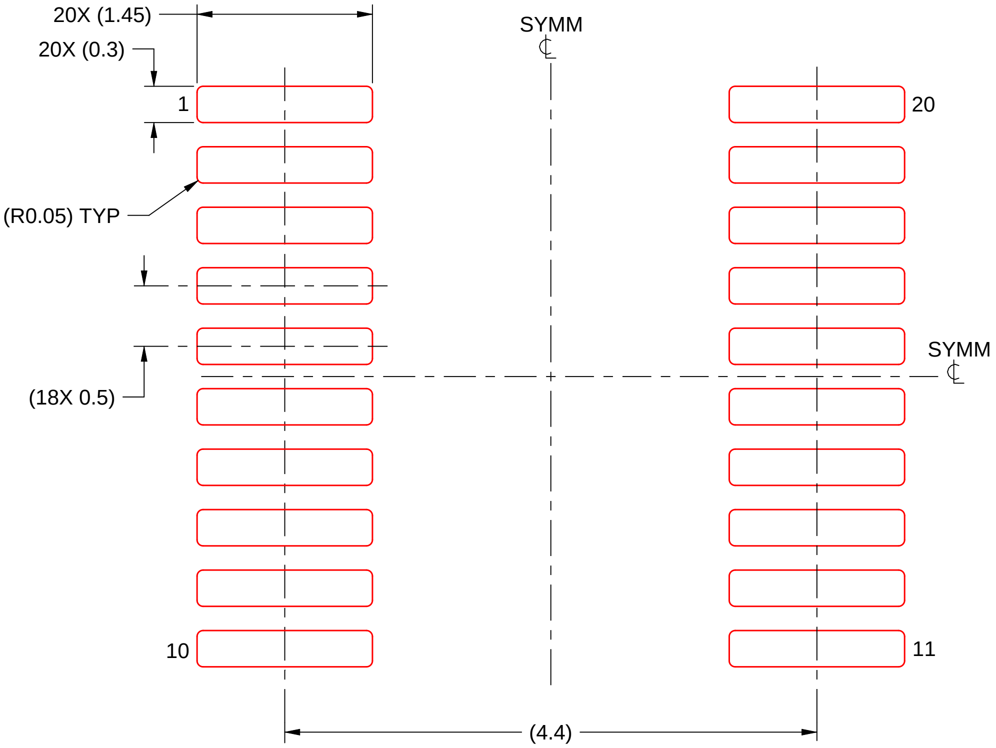
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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