









SN74AHCT1G86

SCLS324P - MARCH 1996 - REVISED FEBRUARY 2024

# SN74AHCT1G86 Single 2-Input Exclusive-OR Gate

#### 1 Features

- Operating range of 4.5V to 5.5V
- Max t<sub>nd</sub> of 8ns at 5V
- Low power consumption, 10A maximum I<sub>CC</sub>
- 8mA output drive at 5V
- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD

# 2 Applications

- Industrial PCs
- Stepper Motors
- **AC Inverter Drives**
- Notebook PCs
- **Smart Meters: Data Concentrators**
- **Enterprise Servers**

# 3 Description

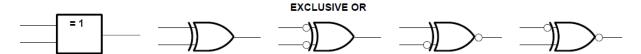
The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A \overline{B}$  in positive logic.

#### **Package Information**

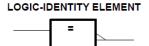
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AHCT1G86	DBV (SOT-23, 5)	2.90mm × 2.8mm	2.9mm × 1.6mm
SIV/4AIICI IGOO	DCK (SC-70, 5)	2.00mm × 1.25mm	2.00mm × 1.25mm

- (1) For more information, see Section 11.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

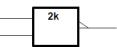


These five equivalent exclusive-OR symbols are valid for an SN74AHCT1G86 gate in positive logic; negation may be shown at any two ports.



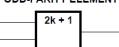
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

#### **EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

## **ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

**Exclusive-OR Logic** 



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# **4 Pin Configuration and Functions**

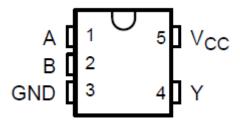


Figure 4-1. DBV or DCK Package 5-Pin SOT-23 Top View

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME	IIFE\/	DESCRIPTION
1	Α	I	A input
2	В	I	B input
3	GND	_	Ground pin
4	Y	0	Output
5	V <sub>CC</sub>	_	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output



# **5 Specifications**

# 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
VI	Input voltage <sup>(2)</sup>	-0.5	7	V	
Vo	Output voltage <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-20	mA
I <sub>OK</sub>	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	-20	20	mA
Io	Continuous output current	$V_O = 0$ to $V_{CC}$	-25	25	mA
	Continuous current through V <sub>CC</sub> or GND		-50	50	mA
T <sub>stg</sub>	Storage temperature		-65	150	°C
TJ	Junction Temperature			150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
Vo	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
t/v	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

Product Folder Links: SN74AHCT1G86

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### **5.4 Thermal Information**

		SN74AF		
	THERMAL METRIC <sup>(1)</sup>	DBV (SOT-23)	DCK (SC-70)	UNIT
		5 PINS	5 PINS	
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	278	289.2	
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	180.5	205.8	
R <sub>0JB</sub>	Junction-to-board thermal resistance	184.4	176.2	°C/W
Ψлт	Junction-to-top characterization parameter	115.4	117.6	C/VV
ΨЈВ	Junction-to-board characterization parameter	183.4	175.1	
R <sub>0JC(bot)</sub>	Junction-to-case (bot) thermal resistance	N/A	N/A	

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

#### 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V	T,	4 = 25°C		-40°C to	85°C	-40°C to 1	25°C	UNIT
	PARAIVIETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>OH</sub>	High level output	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
V OH	voltage	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		V
Low level output		I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	V
V <sub>OL</sub>	voltage	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		0.44	•
II	Input leakage current	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μA
I <sub>cc</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			1		10		10	μА
ΔI <sub>CC</sub> (1)	Supply-current change	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5	mA
Ci	Input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10		10	pF

<sup>(1)</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

# **5.6 Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM			FROM TO LOAD		TO LOAD T <sub>A</sub> = 25°C		°C	-40°C to 85°C		-40°C to 125°C		UNIT
TANAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	TYP	MAX	MIN	MAX	MIN	MAX	UNII			
t <sub>PLH</sub>	A or B	<b>V</b>	C <sub>1</sub> = 15 pF	5	6.2	1	8	1	9	ns			
t <sub>PHL</sub>	AOIB	AUD	C <sub>L</sub> = 15 pr	5	6.2	1	8	1	9	113			
t <sub>PLH</sub>	A or B	V	C <sub>1</sub> = 50 pF	5.5	7.9	1	9	1	10	no			
t <sub>PHL</sub>		A OI B	C <sub>L</sub> = 50 pr	5.5	7.9	1	9	1	10	ns			



# **5.7 Operating Characteristics**

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	PARAMETER	TEST (	CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

# **5.8 Typical Characteristics**

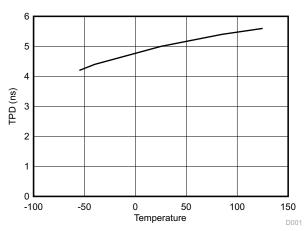


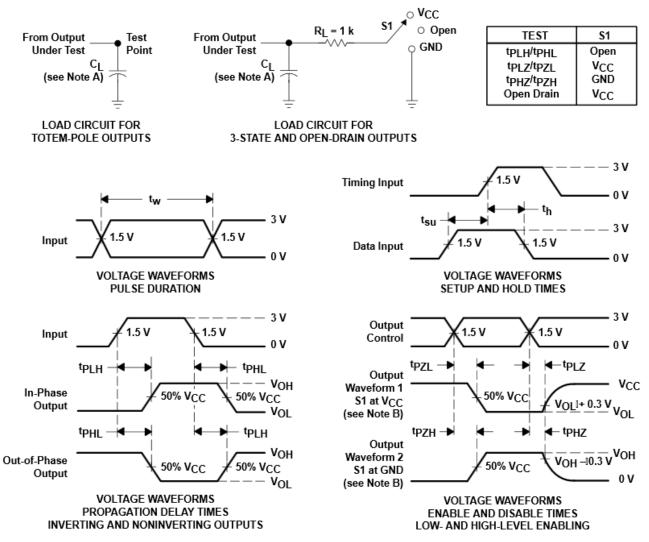
Figure 5-1. TPD vs. Temperature

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### **6 Parameter Measurement Information**



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR 1 MHz, ZO = 50 , tr 3 ns, tf 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms



# 7 Detailed Description

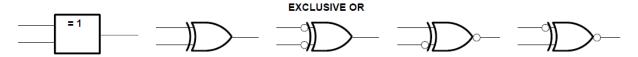
#### 7.1 Overview

The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{AB} + A \overline{B}$  in positive logic.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

# 7.2 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These five equivalent exclusive-OR symbols are valid for an SN74AHCT1G86 gate in positive logic; negation may be shown at any two ports.

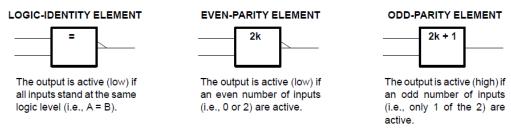


Figure 7-1. Exclusive-OR Logic

### 7.3 Feature Description

The device is ideal for operating in a 5-V logic system. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

#### 7.4 Device Functional Modes

**Table 7-1. Function Table** 

INP	JTS <sup>(1)</sup>	OUTPUT <sup>(2)</sup>
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74AHCT1G86 is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V  $V_{IL}$  and 2-V  $V_{IH}$ . This feature makes it Ideal for translating up from 3.3 V to 5 V.

### 8.2 Typical Application

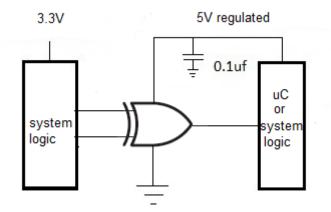


Figure 8-1. Typical Application Schematic

## 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- · Recommended input conditions:
  - Rise time and fall time specs. See ( $\Delta t/\Delta V$ ) in Section 5.3.
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in Section 5.3.
- · Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V<sub>CC</sub>.

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# 8.2.3 Application Curves

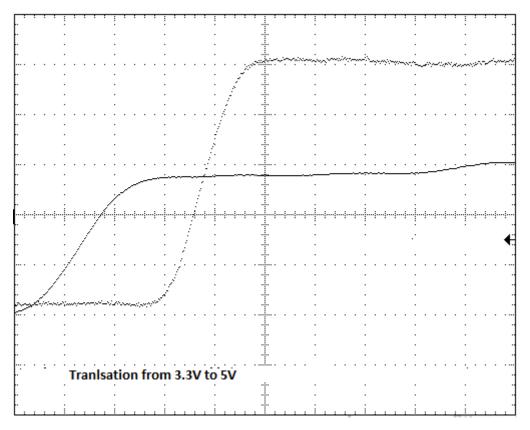


Figure 8-2. Translation From 3.3 V to 5.5 V



## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 5.3.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor and if there are multiple  $V_{CC}$  terminals then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

#### 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

## 8.4.2 Layout Example

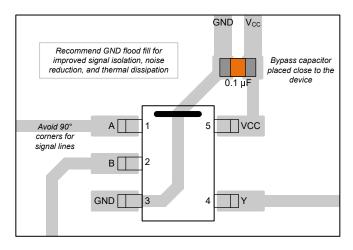


Figure 8-3. Layout Example for the SN74AHCT1G86



# 9 Device and Documentation Support

## 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.4 Trademarks

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#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

## Changes from Revision O (October 2023) to Revision P (February 2024)

**Page** 

Updated thermal values for DBV package from RθJA = 208.2 to 278, RθJC(top) = 76.1 to 180.5, RθJB = 52.5 

#### Changes from Revision N (August 2022) to Revision O (October 2023)

Page

Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 

Product Folder Links: SN74AHCT1G86



# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
74AHCT1G86DBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B86G
74AHCT1G86DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B86G
74AHCT1G86DBVTG4	Obsolete	Production	SOT-23 (DBV)   5	-	-	Call TI	Call TI	-40 to 125	B86G
SN74AHCT1G86DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39EH, 3CDF, B863, B86G, B86J, B 86S)
SN74AHCT1G86DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39EH, 3CDF, B863, B86G, B86J, B 86S)
SN74AHCT1G86DBVT	Obsolete	Production	SOT-23 (DBV)   5	-	-	Call TI	Call TI	-40 to 125	(B863, B86G, B86J, B86S)
SN74AHCT1G86DCKR	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QV, BH3, BHG, BH J, BHL, BHS)
SN74AHCT1G86DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QV, BH3, BHG, BH J, BHL, BHS)
SN74AHCT1G86DCKT	Obsolete	Production	SC70 (DCK)   5	-	-	Call TI	Call TI	-40 to 125	(BH3, BHG, BHJ, BH S)

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74AHCT1G86:

Automotive: SN74AHCT1G86-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G86DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G86DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G86DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G86DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G86DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHCT1G86DCKR	SC70	DCK	5	3000	210.0	185.0	35.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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