# SN74AHCT1G32-Q1 Automotive Single 2-Input Positive-OR Gate

## 1 Features

- Qualified for automotive applications
- Operating range of 4.5V to 5.5V
- Max $t_{pd}$ of 9.5ns at 5V
- Low power consumption, 20µA max $I_{CC}$
- Output drive of ±8mA at 5V
- Inputs are TTL-voltage compatible

## 2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

## 3 Description

The SN74AHCT1G32-Q1 device is a single 2-input positive-OR gate. The device performs the Boolean function Y = A + B in positive logic.

### Package Information

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] | BODY SIZE[3] |
|---|---|---|---|
| SN74AHCT1G32-Q1 | DBV (SOT-23, 5) | 2.9mm x 2.8mm | 2.9mm × 1.6mm |
| | DCK (SOT-SC70, 5) | 2.00mm × 1.25mm | 2.00mm × 1.25mm |
| | DTX (X2SON, 5) | 1.1mm x 0.85mm | 1.1mm x 0.85mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



**Logic Diagram (Positive Logic)**

## Table of Contents

Product Folder Links: *SN74AHCT1G32-Q1*

# 4 Pin Configuration and Functions



**Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SOT-SC70 (Top View)**



Not to scale
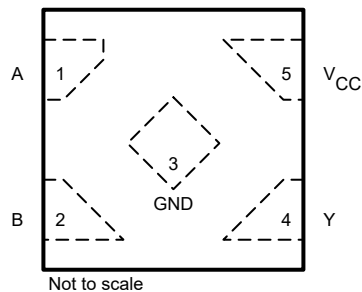
**Figure 4-2. DTX Package, 5-Pin X2SON (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A | 1 | I | Input A |
| B | 2 | I | Input B |
| GND | 3 | — | Ground Pin |
| Y | 4 | O | Output Y |
| $V_{CC}$ | 5 | — | Power Pin |

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 | 7 | V |
| $V_I$ | Input voltage | | −0.5 | 7 | V |
| $V_O$ | Output voltage | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | −20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | −65 | 150 | °C |

(1)    Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime .

Note: The input and output voltage ratings may be exceeded if the input and output current ratings are observed. The package thermal impedance is calculated in accordance with JESD 51-7.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002[1] | ±2000 | V |
| | | Charged-Device Model (C5), per AEC Q100-011 , all pins | ±1000 | |

(1)    AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | −8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | −40 | 125 | °C |

(1)    All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| | | SN74AHCT1G32-Q1 | | | |
|---|---|---|---|---|---|
| **THERMAL METRIC**[1] | | DBV (SOT-23) | DCK (SOT-70) | DTX (X2SON) | **UNIT** |
| | | **5 PINS** | **5 PINS** | **5 PINS** | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278 | 289.2 | 184.7 | °C/W |

(1)    For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.7 | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.52 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | | 20 | µA |
| $\Delta I_{CC}$ [(1)] | Supply-current change | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.65 | mA |
| $C_i$ | Input Capacitance | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | 10 | | 10 | pF |

(1)    This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)
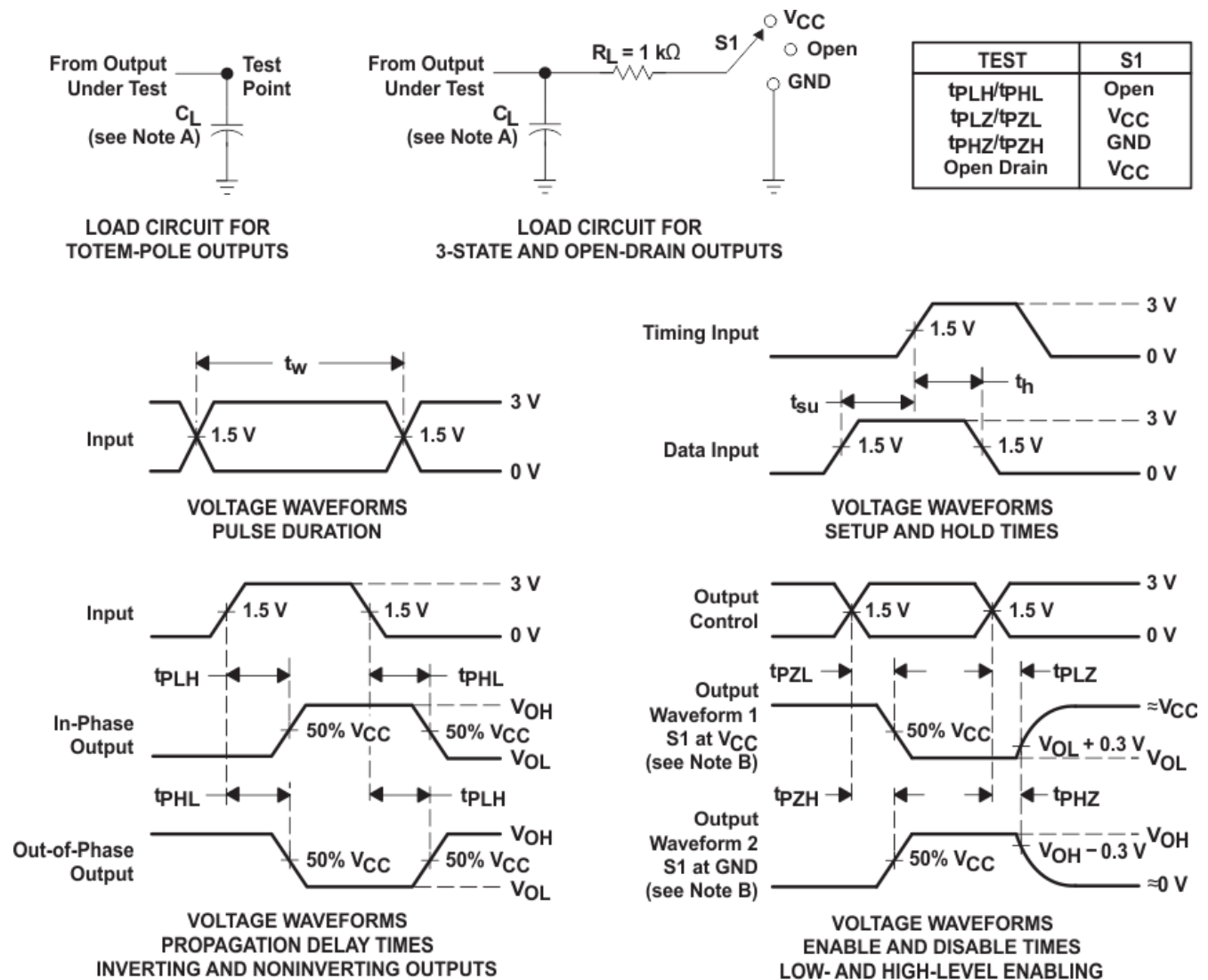
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5 | 6.9 | 1 | 8 | | 9.5 | ns |
| $t_{PHL}$ | | | | | 5 | 6.9 | 1 | 8 | | 9.5 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 9 | | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | 9 | | 10.5 | |

## 5.7 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 11.5 | pF |

## 6 Parameter Measurement Information



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

**LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS**

**VOLTAGE WAVEFORMS PULSE DURATION**

**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING**

NOTES:   A.   $C_L$ includes probe and jig capacitance.
B.   Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D.   The outputs are measured one at a time, with one input transition per measurement.
E.   All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

Product Folder Links: *SN74AHCT1G32-Q1*

# 7 Detailed Description

## 7.1 Overview

The SN74AHCT1G32-Q1 device is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{A \times B}$ in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when $V_{CC} = 0$ V.

## 7.2 Functional Block Diagram



**Figure 7-1. Logic Diagram (Positive Logic)**

## 7.3 Feature Description

- Slow rise and fall time on outputs allow for low noise outputs.
- TTL inputs Allows up translation from 3.3 V to 5 V

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS[1] | | OUTPUT[2] |
| --- | --- | --- |
| **A** | **B** | **Y** |
| H | X | H |
| X | H | H |
| L | L | L |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

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**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.
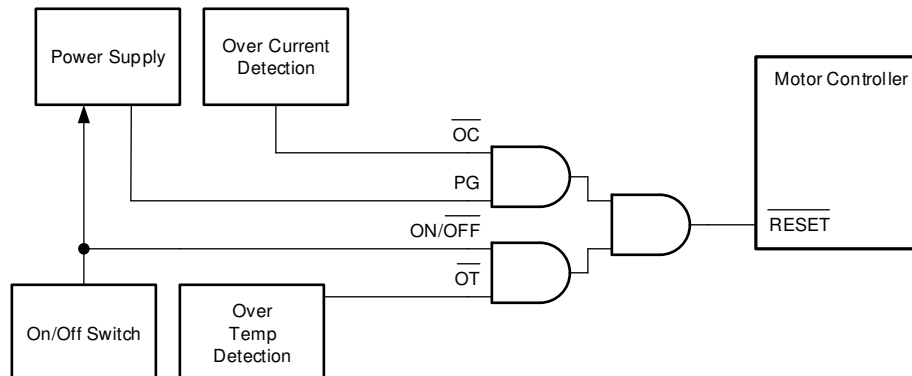
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## 8.1 Typical Application



**Figure 8-1. Typical Application Block Diagram**

### 8.1.1 Design Requirements

#### 8.1.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHCT1G32-Q1 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHCT1G32-Q1 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74AHCT1G32-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74AHCT1G32-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

Product Folder Links: *SN74AHCT1G32-Q1*

> **CAUTION**
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.1.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ $V_{t-(min)}$ to be considered a logic LOW, and $V_{IH(min)}$ $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHCT1G32-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74AHCT1G32-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

The SN74AHCT1G32-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.1.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

*Submit Document Feedback* 9

Product Folder Links: *SN74AHCT1G32-Q1*

### 8.1.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHCT1G32-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω, so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

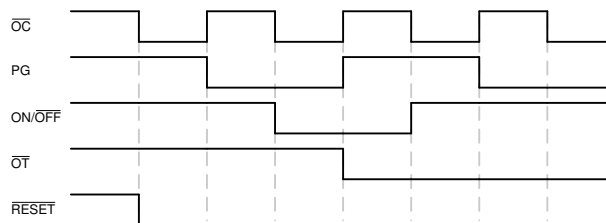### 8.1.3 Application Curves



**Figure 8-2. Application Timing Diagram**

## 8.2 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple $V_{CC}$ pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.3 Layout

### 8.3.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.
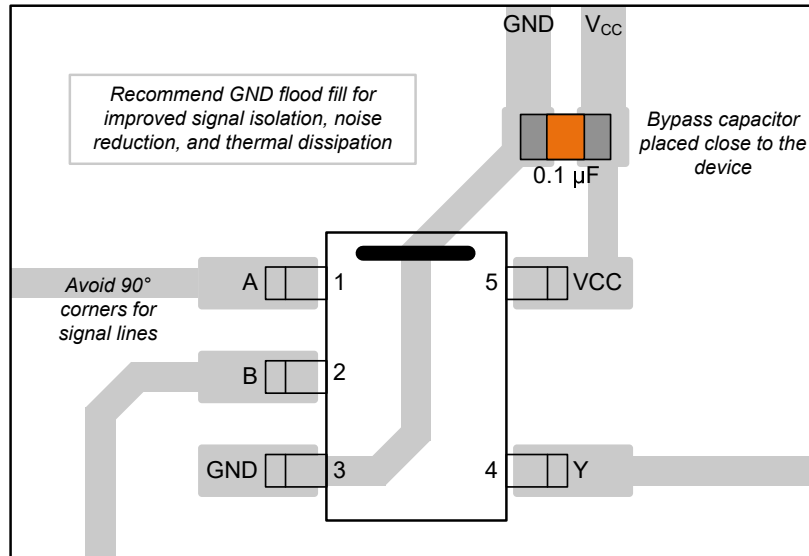
### 8.3.1.1 Layout Example



**Figure 8-3. Example Layout for the SN74AHCT1G32-Q1**

# 9 Device and Documentation Support

## 9.1 Documentation Support (Analog)

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary          This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

**Changes from Revision E (February 2024) to Revision F (October 2024)**                                    **Page**

- Added DTX package to *Package Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table ...........................................................................................................................1

**Changes from Revision D (October 2023) to Revision E (February 2024)**                                    **Page**

- Added body size to *Package Information* table.........................................................................................1
- Updated RθJA value: DBV = 206 to 278, all values in °C/W ....................................................................4

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable part number (1) | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CAHCT1G32QDBVRQ1 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (36GH, B32U) |
| CAHCT1G32QDBVRQ1.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (36GH, B32U) |
| CAHCT1G32QDCKRQ1 | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BGU |
| CAHCT1G32QDCKRQ1.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BGU |
| CAHCT1G32WDTXRQ1 | Active | Production | X2SON (DTX) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 8 |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF SN74AHCT1G32-Q1 :**

- Catalog : SN74AHCT1G32

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CAHCT1G32QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| CAHCT1G32QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| CAHCT1G32WDTXRQ1 | X2SON | DTX | 5 | 3000 | 180.0 | 8.4 | 1.0 | 1.25 | 0.48 | 2.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CAHCT1G32QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| CAHCT1G32QDCKRQ1 | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |
| CAHCT1G32WDTXRQ1 | X2SON | DTX | 5 | 3000 | 210.0 | 185.0 | 35.0 |

PIN 1
INDEX AREA

3.0
2.6

1.75
1.45

B

A

C

0.1 C

1

5

2

4

3

2X 0.95

1.9

3.05
2.75

1.9

(0.1)

(0.15)

5X 0.5
0.3

0.2 Ⓜ C A B

NOTE 5

4X 0° -15°

0.15
0.00 TYP

(1.1)

1.45
0.90

4X 4° -15°

GAGE PLANE

0.25

0.22
0.08 TYP

8° TYP
0°

0.6
0.3 TYP

SEATING PLANE

4214839/K  08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

5X (1.1)
PKG ℄
1
5X (0.6)
5
SYMM ℄
2
(1.9)
2X (0.95)
3
4
(R0.05) TYP
(2.6)

SOLDER MASK DETAILS

SOLDER MASK OPENING — METAL

EXPOSED METAL

0.07 MAX ARROUND

NON SOLDER MASK DEFINED (PREFERRED)

METAL UNDER SOLDER MASK — SOLDER MASK OPENING

EXPOSED METAL

0.07 MIN ARROUND

SOLDER MASK DEFINED

4214839/K   08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## DBV0005A

### SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

PKG ₵

5X (1.1)

1

5X (0.6)

5

2

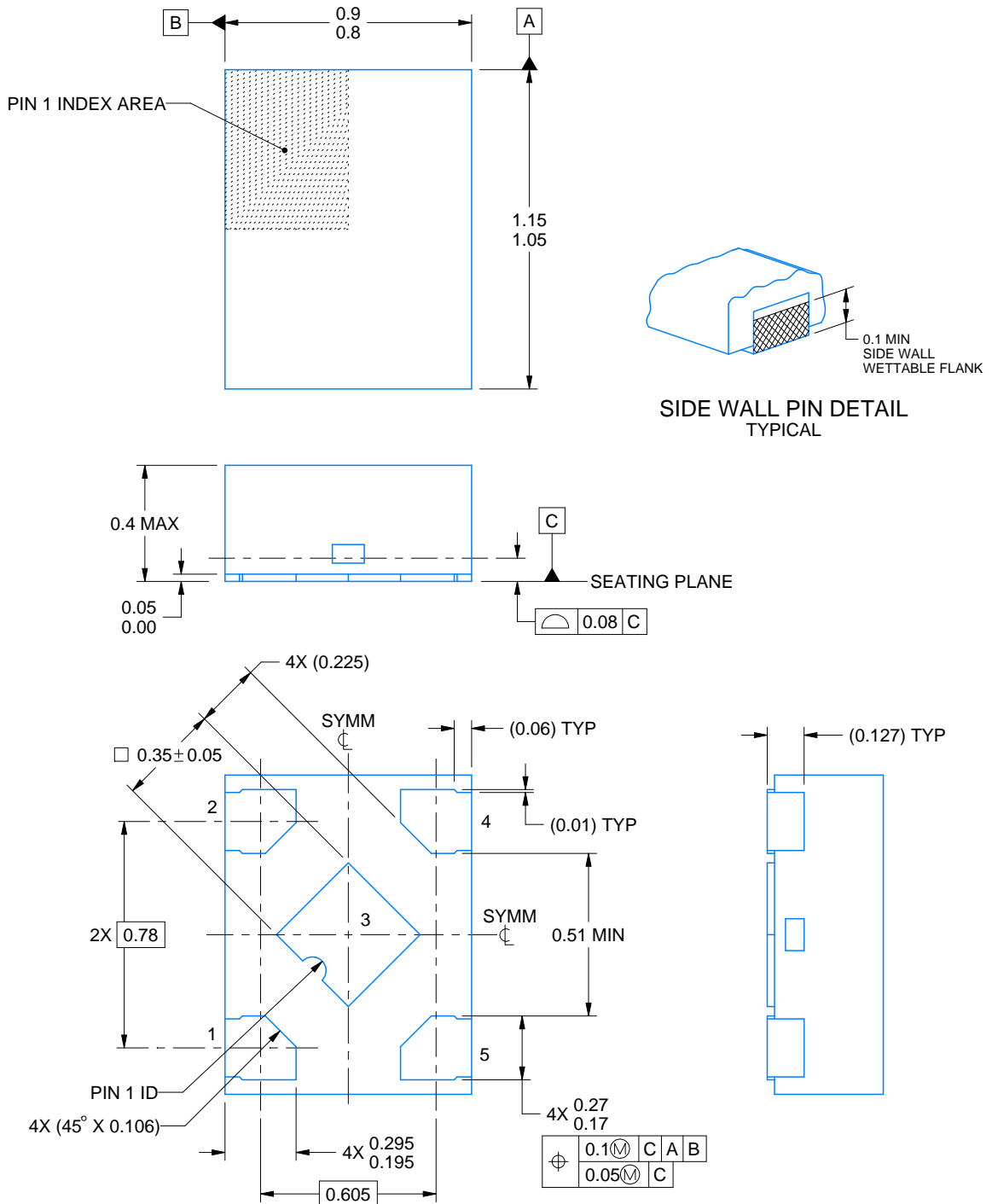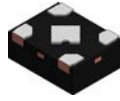SYMM ₵

(1.9)

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K   08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

B

0.9
0.8

A

PIN 1 INDEX AREA

1.15
1.05

0.1 MIN
SIDE WALL
WETTABLE FLANK

**SIDE WALL PIN DETAIL**
TYPICAL

0.4 MAX

C

SEATING PLANE

0.05
0.00

| | 0.08 | C |

4X (0.225)

SYMM

(0.06) TYP

□ 0.35 ± 0.05

2

4

(0.01) TYP

2X 0.78

3

SYMM

0.51 MIN

(0.127) TYP

1

PIN 1 ID

5

4X (45° X 0.106)

4X 0.295
0.195

0.605

4X 0.27
0.17

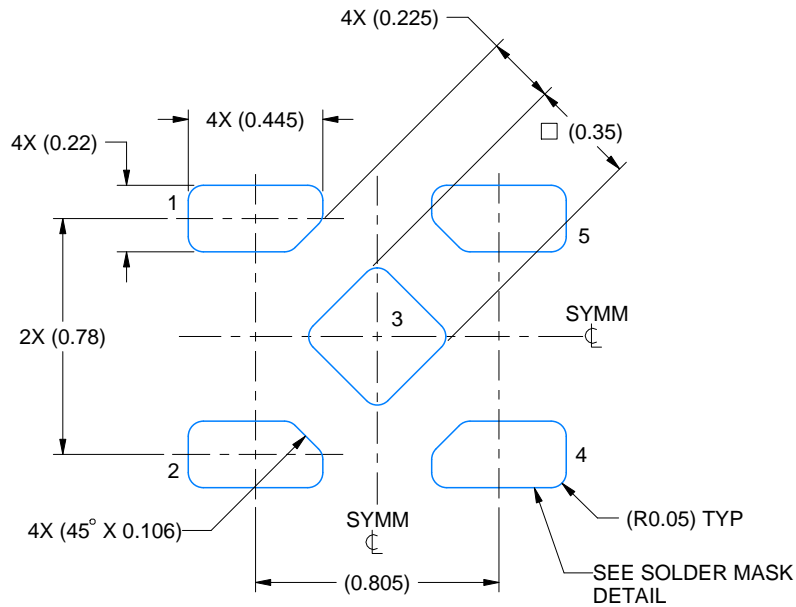| ⊕ | 0.1 Ⓜ | C | A | B |
|---|---|---|---|---|
| | 0.05 Ⓜ | C | | |

4229388/C   10/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**TEXAS INSTRUMENTS**
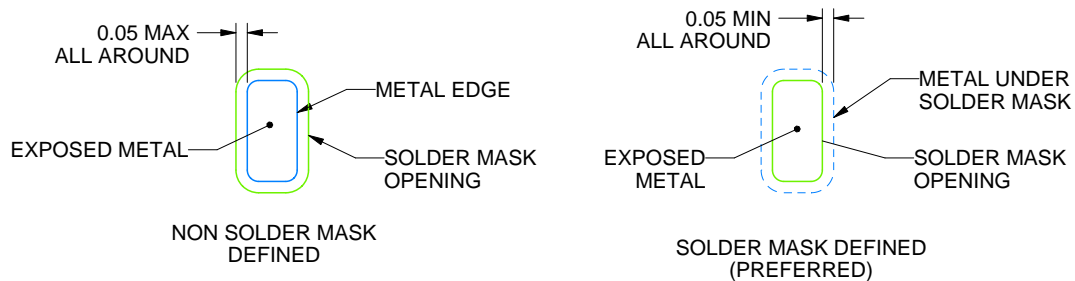www.ti.com

4X (0.225)

4X (0.445)

□ (0.35)

4X (0.22)

1

5

2X (0.78)

3

SYMM
℄

2

4

4X (45° X 0.106)

SYMM
℄

(R0.05) TYP

(0.805)

SEE SOLDER MASK
DETAIL

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

0.05 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED
(PREFERRED)

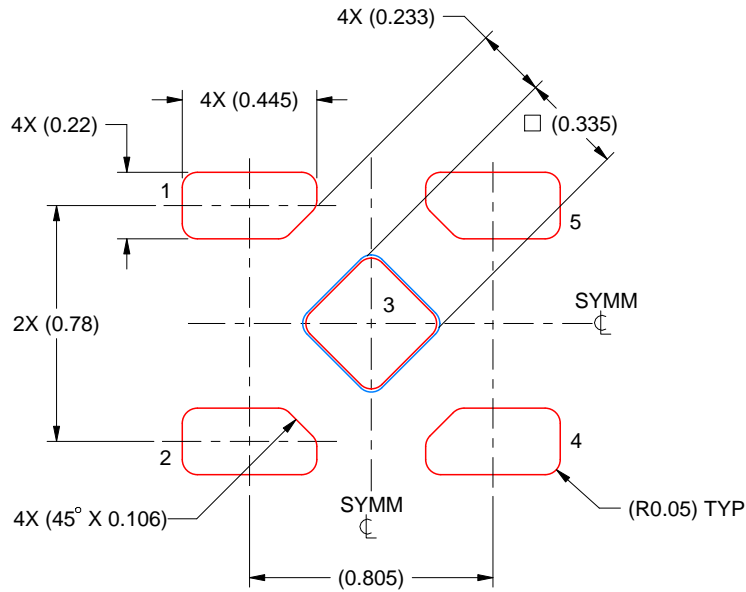SOLDER MASK DETAILS

4229388/C   10/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
number SLUA271 (www.ti.com/lit/slua271).

4X (0.233)

4X (0.445)

4X (0.22)

□ (0.335)

1

5

2X (0.78)

3

SYMM
℄

2

4

4X (45° X 0.106)

(R0.05) TYP

SYMM
℄

(0.805)

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

PRINTED SOLDER PASTE COVERAGE BY AREA UNDER PACKAGE
PAD 5: 92%

4229388/C   10/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.

## DCK0005A

### SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G   11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

## DCK0005A

5X (0.95)

PKG ℄

1

5X (0.4)

2

2X (0.65)

3

(R0.05) TYP

5

SYMM ℄

(1.3)

4

(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214834/G   11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G   11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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