









SN74AHCT1G126

SCLS380L - AUGUST 1997 - REVISED MARCH 2024

SN74AHCT1G126 Single Bus Buffer Gate With 3-State Output

1 Features

- Operating range of 4.5V to 5.5V
- Max t_{nd} of 6ns at 5V
- Low power consumption, 10µA max I_{CC}
- ±8mA output drive at 5V
- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Motor Controls: AC Induction
- **Graphics Cards**
- Advanced Driver Assistance Systems (ADAS)
- Motor Drives & Controls
- **DLP Front Projection Systems**
- Server Motherboards

3 Description

The SN74AHCT1G126 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

Package Information

PART NUMBER	PART NUMBER PACKAGE ⁽¹⁾		BODY SIZE(3)
SN74AHCT1G126	DBV (SOT-23, 5)	2.9mm x 2.8mm	2.9mm x 1.6mm
3N74A1101113120	DCK (SC-70, 5)	2mm x 2.1mm	2mm x 1.25mm

- For more information, see Section 11.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.

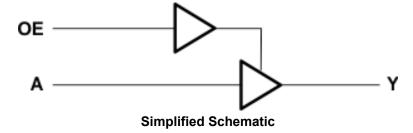




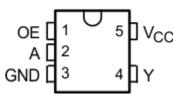
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4 Pin Configuration and Functions

DBV OR DCK PACKAGE (TOP VIEW)



	PIN	TYPE	DESCRIPTION			
NO.	NAME	IIFE	DESCRIPTION			
1	OE	I	Output Enable			
2	Α	I	Input A			
3	GND	_	Ground Pin			
4	Y	0	Output Y			
5	V _{CC}	_	Power Pin			

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V	
V _I ⁽²⁾	Input voltage		-0.5	7	V
V _O (2)	Output voltage		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)		-20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V _O = 0 to V _{CC})		±25	mA
	Continuous channel current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
Vo	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-8	mA
I _{OL}	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



5.4 Thermal Information

		SN74AH	CT1G126	
	THERMAL METRIC ⁽¹⁾	DBV	DCK	UNIT
		5 F	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	
R _{0JC(top)}	Junction-to-case (top) thermal resistance	180.5	205.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	176.2	°C/W
ΨЈТ	Junction-to-top characterization parameter	115.4	117.6	- C/VV
ΨЈВ	Junction-to-board characterization parameter	183.4	175.1	
R _{0JC(bot)}	Junction-to-case (bot) thermal resistance	N/A	N/A	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			-40°C to 85°C		-40°C to 125°C		UNIT
PARAWETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
V _{OH}	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		V
V	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
V _{OL}	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	V
I ₁	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μΑ
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10		10	μΑ
ΔI _{CC} ⁽¹⁾	One input at 3.4 V, Other input at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		4	10		10		10	pF
Co	V _O = V _{CC} or GND	5 V		10						pF

⁽¹⁾ This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	LOAD	TA	= 25°C	;	-40°C to	85°C	-40°C to 1	25°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	А	Y	C _L = 15 pF		3.8	5.5	1	6.5	1	7	ns
t _{PHL}	^	I	OL = 13 pr		3.8	5.5	1	6.5	1	7	115
t _{PZH}	OE	Υ	C _L = 15 pF		3.6	5.1	1	6	1	6.5	ns
t _{PZL}	OL	I	OL = 13 pr		3.6	5.1	1	6	1	6.5	115
t _{PHZ}	OE	Υ	C _L = 15 pF		4.6	6.8	1	8	1	8.5	ns
t _{PLZ}	OL	I	OL = 13 pr		4.6	6.8	1	8	1	8.5	115
t _{PLH}	А	Y	C _L = 50 pF		5.3	7.5	1	8.5	1	9.5	ns
t _{PHL}	^	'	OL = 30 pi		5.3	7.5	1	8.5	1	9.5	115
t _{PZH}	OE	Υ	C _L = 50 pF		5.1	7.1	1	8	1	9	ns
t _{PZL}	OE	I	CL = 30 pr		5.1	7.1	1	8	1	9	115
t _{PHZ}	OE	Y	C _L = 50 pF		6.1	8.8	1	10	1	11	ns
t _{PLZ}	OE	ľ	C _L = 50 pr		6.1	8.8	1	10	1	11	115



5.7 Operating Characteristics

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

5.8 Typical Characteristics

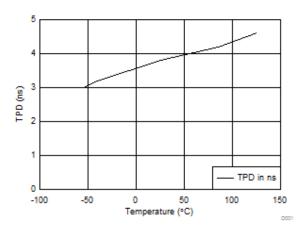
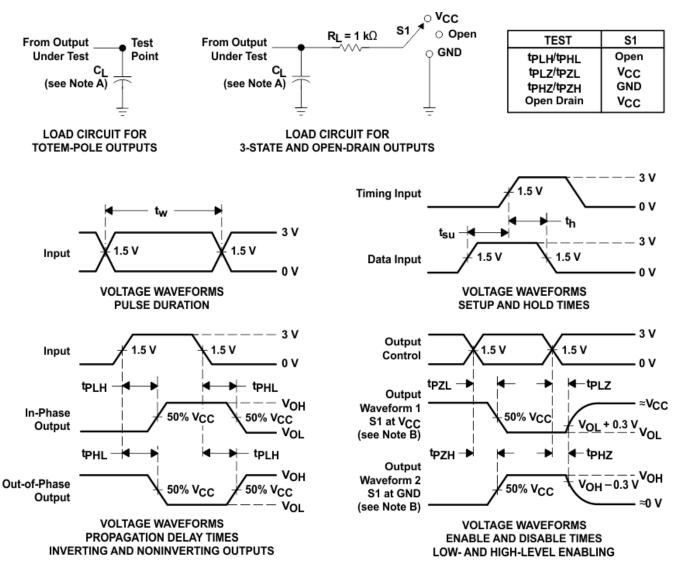


Figure 5-1. TPD vs Temperature



6 Parameter Measurement Information



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns. $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHCT1G126 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

7.2 Functional Block Diagram

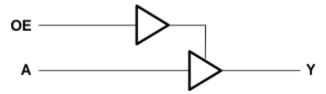


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- · TTL Inputs
 - Lowered switching threshold allows up translation 3.3 V to 5 V
- · Slow edges reduce output ringing

7.4 Device Functional Modes

Table 7-1. Function Table

INP	JTS	OUTPUT
OE	Α	Y
Н	Н	Н
Н	L	L
L	Χ	Z

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74AHCT1G126 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of $0.8\text{-V}\ \text{V}_{\text{IL}}$ and $2\text{-V}\ \text{V}_{\text{IH}}$. This feature makes it Ideal for translating up from $3.3\ \text{V}$ to $5\ \text{V}$. Figure 8-2 shows this type of translation.

8.2 Typical Application

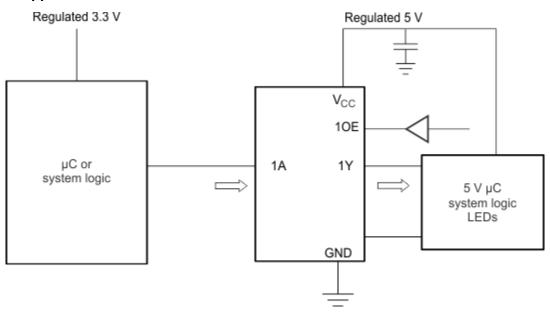


Figure 8-1. Typical Application Schematic

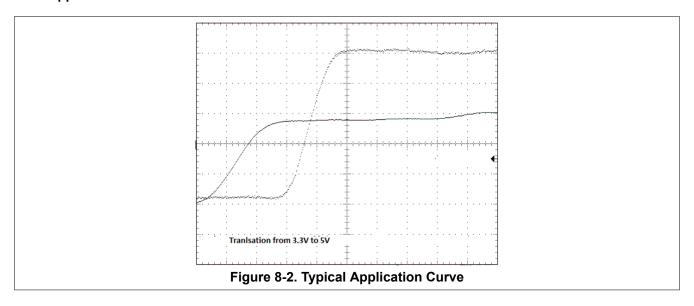
8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the Section 5.3 table.
 - For specified High and low levels, see V_{IH} and V_{II} in the Section 5.3 table.
- 2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 5.3 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.1.1 Layout Example

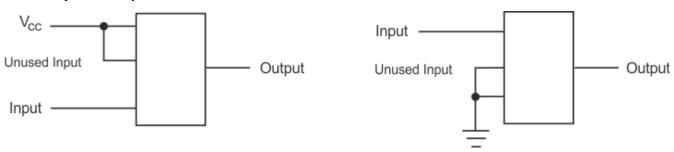


Figure 8-3. Layout Diagram



9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
74AHCT1G126DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B26G
74AHCT1G126DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B26G
74AHCT1G126DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B26G
74AHCT1G126DBVTG4	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	B26G
74AHCT1G126DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BN3
74AHCT1G126DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BN3
74AHCT1G126DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BN3
74AHCT1G126DCKTG4.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BN3
SN74AHCT1G126DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(38ZH, 3C9F, B263, B26G, B26J, B 26S)
SN74AHCT1G126DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(38ZH, 3C9F, B263, B26G, B26J, B 26S)
SN74AHCT1G126DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QT, BN3, BNG, BN J, BNL, BNS, B NU, BNY)
SN74AHCT1G126DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QT, BN3, BNG, BN J, BNL, BNS, B NU, BNY)
SN74AHCT1G126DCKT	Obsolete	Production	SC70 (DCK) 5	-	-	Call TI	Call TI	-40 to 125	(BN3, BNG, BNJ, BN S)

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHCT1G126:

Automotive: SN74AHCT1G126-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G126DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G126DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74AHCT1G126DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G126DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G126DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G126DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G126DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
74AHCT1G126DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G126DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHCT1G126DCKR	SC70	DCK	5	3000	210.0	185.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025