









SN74AHCT1G02 SCLS341M - APRIL 1996 - REVISED FEBRUARY 2024

SN74AHCT1G02 Single 2-Input Positive-NOR GateSN74AHCT1G02 Single 2-Input **Positive-NOR Gate**

1 Features

- Operating range of 4.5 V to 5.5 V
- eMax t_{nd} of 6.5 ns at 5 V
- Low power consumption, 10-µA max I_{CC}
- ± 8-mA output drive at 5 V
- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA per JESD

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

3 Description

This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A + B}$ positive logic.

Package Information

	PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
	SN74AHCT1G02	DBV (SOT-23, 5)	2.8 mm x 2.8 mm
		DCK (SC-70, 5)	2.1 mm x 1.25 mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.





Table of Contents

1 Features	1	7.4 Device Functional Modes	7
2 Applications	1	8 Application Information Disclaimer	8
3 Description	1	8.1 Application Information	8
4 Pin Configuration and Functions	3	8.2 Typical Application	
5 Specifications	4	8.3 Power Supply Recommendations	
5.1 Absolute Maximum Ratings		8.4 Layout	10
5.2 ESD Ratings	4	9 Device and Documentation Support	12
5.3 Recommended Operating Conditions		9.1 Documentation Support (Analog)	12
5.4 Thermal Information	4	9.2 Receiving Notification of Documentation Updates	1 <mark>2</mark>
5.5 Electrical Characteristics	<mark>5</mark>	9.3 Support Resources	12
5.6 Switching Characteristics	<mark>5</mark>	9.4 Trademarks	12
5.7 Operating Characteristics	<u>5</u>	9.5 Electrostatic Discharge Caution	12
6 Parameter Measurement Information	6	9.6 Glossary	12
7 Detailed Description	<mark>7</mark>	10 Revision History	12
7.1 Overview	<mark>7</mark>	11 Mechanical, Packaging, and Orderable	
7.2 Functional Block Diagram	<mark>7</mark>	Information	13
7.3 Feature Description	7		



4 Pin Configuration and Functions

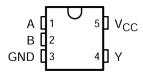


Figure 4-1. DBV or DCK Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION		
NO.	NAME	IIPE	DESCRIPTION		
1	A	I	Input A		
2	В	I	Input B		
3	GND	_	Ground Pin		
4	Y	0	Output Y		
5	V _{CC}	_	Power Pin		



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I (2)	Input voltage range		-0.5	7	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)		-20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
Vo	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-8	mA
I _{OL}	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

5.4 Thermal Information

			SN74AHCT1G02		
THERMAL METRIC(1)		DBV	DCK	UNIT	
		5 PINS	5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	°C/W	

¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

Product Folder Links: SN74AHCT1G02

The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T _A = 25°C			MIN MA	MAX	UNIT	
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	IVIIIN	WAA	UNII	
V	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		V	
V_{OH}	I _{OH} = -8 mA	4.5 V	3.94			3.8		, V	
\/	I _{OL} = 50 μA	4.5 V			0.1		0.1	V	
V_{OL}	I _{OL} = 8 mA	4.5 V	-		0.36		0.44	V	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	-		1		10	μA	
ΔI _{CC} ⁽¹⁾	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			1.35		1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		4	10		10	PF	

⁽¹⁾ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

DADAMETED	EDOM (INDUT)	TO (OUTDUT)	LOAD	T,	_A = 25°C		MINI	MAY	UNIT			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT			
t _{PLH}	A or B	A or D V	Y C _L = 15	0 - 45 -5		2.4	5.5	1	6.5	no		
t _{PHL}		7 4016		τ C _L = 13 pr	C _L = 15 pr		3.5	5.5	1	6.5	ns	
t _{PLH}	A == D	A D	A D			0 - 50 - 5		3.4	7.5	1	8.5	no
t _{PHL}	A or B	ř	$C_L = 50 pF$		4.5	7.5	1	8.5	ns			

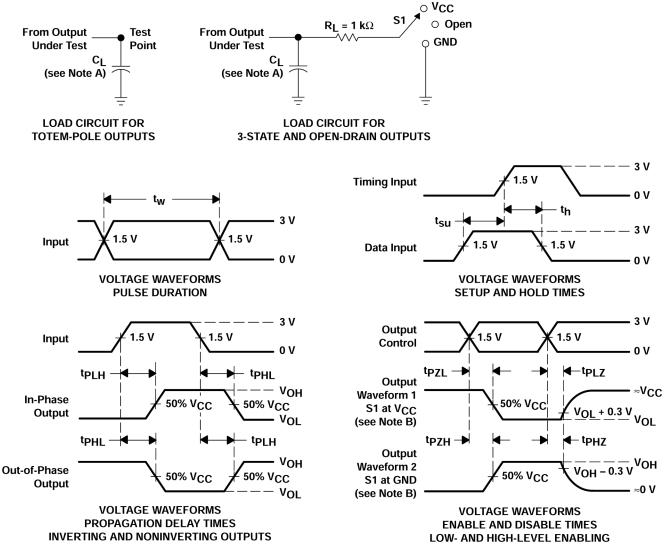
5.7 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TES	ST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	17	pF



6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND
Open Drain	V _{CC}

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7 Detailed Description

7.1 Overview

The SN74AHCT1G02 contains four independent 2-input AND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = A \times B$ in positive logic. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

7.2 Functional Block Diagram



Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in Figure 7-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

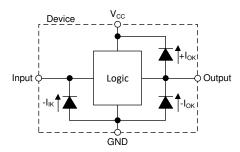


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table (Each Gate)

INP	JTS	OUTPUT Y
Α	В	OUIFOLL
Н	Х	L
Х	Н	L
L	L	Н

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Figure 8-1. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHCT1G02 is used to directly control the RESET pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

8.2 Typical Application

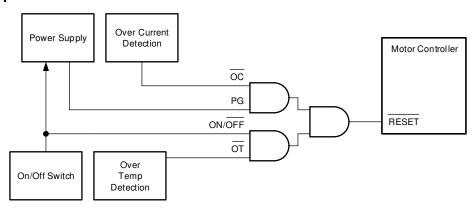


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHCT1G02 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHCT1G02 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

Product Folder Links: SN74AHCT1G02

The SN74AHCT1G02 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74AHCT1G02 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption* and *Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ $V_{t-(min)}$ to be considered a logic LOW, and $V_{IH(min)}$ $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHCT1G02 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74AHCT1G02 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

The SN74AHCT1G02 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

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Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the
 device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the Layout
 section.
- 2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHCT1G02 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$, so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

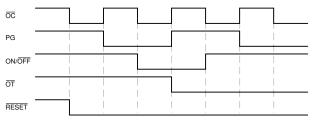


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

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When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

Product Folder Links: SN74AHCT1G02



8.4.1.1 Layout Example

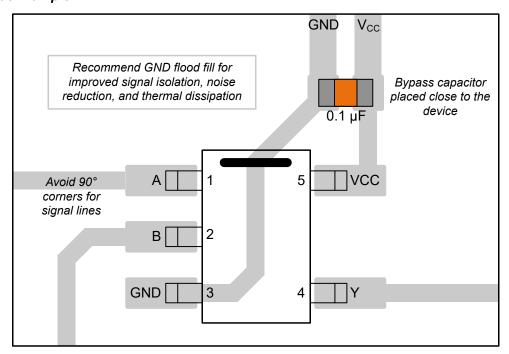


Figure 8-3. Example Layout for the SN74AHCT1G02



9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision L (October 2023) to Revision M (February 2024)

Page

Updated RθJA values: DBV = 206 to 278, all values in °C/W......4

Changes from Revision K (February 2003) to Revision L (October 2023)

Page

Product Folder Links: SN74AHCT1G02



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74AHCT1G02DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	(4) NIPDAU	(5) Level-1-260C-UNLIM	-40 to 85	B02G
74AHCT1G02DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	B02G
			, , ,	·					
74AHCT1G02DBVTG4	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 85	B02G
74AHCT1G02DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BB3
74AHCT1G02DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BB3
74AHCT1G02DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BB3
SN74AHCT1G02DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(38UH, 3C6F, B023, B02G, B02J, B 02S)
SN74AHCT1G02DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(38UH, 3C6F, B023, B02G, B02J, B 02S)
SN74AHCT1G02DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 85	(B023, B02G, B02J, B02S)
SN74AHCT1G02DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(1QR, BB3, BBG, BB J, BBS)
SN74AHCT1G02DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(1QR, BB3, BBG, BB J, BBS)

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHCT1G02:

Automotive: SN74AHCT1G02-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G02DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G02DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G02DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G02DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G02DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G02DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G02DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHCT1G02DCKR	SC70	DCK	5	3000	210.0	185.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025