SN74AHCT138Q-Q1 Automotive 3-Line to 8-Line Decoders/Demultiplexers

1 Features

- Qualified for Automotive Applications
- EPIC (Enhanced-Performance Implanted CMOS) Process
- Inputs Are TTL-Voltage Compatible
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception
- Latch-Up Performance Exceeds 250mA Per JESD 17
- ESD Protection Exceeds 2000V Per MIL-STD-833, Method 3015

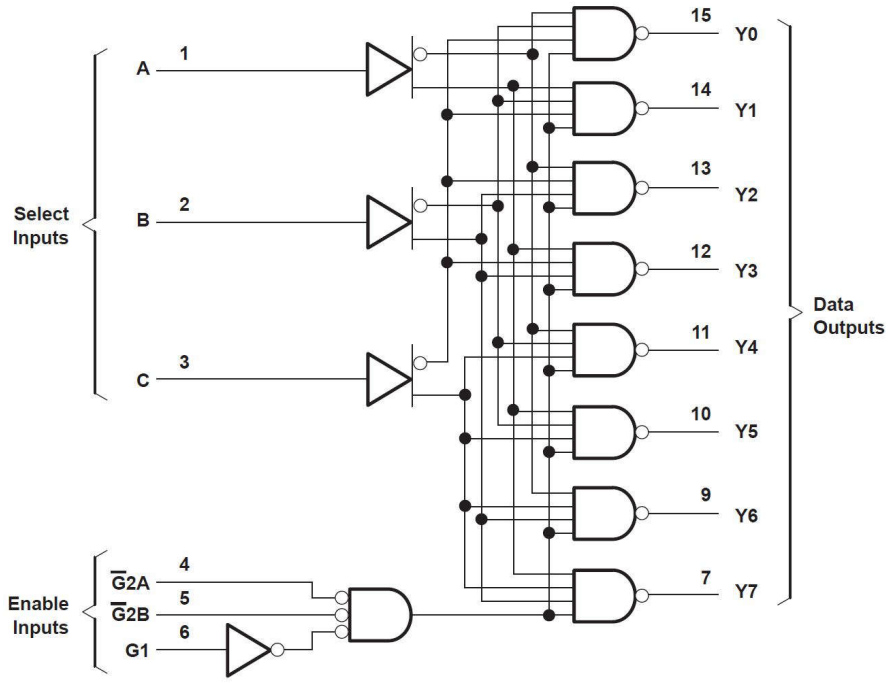
2 Description

The SN74AHCT138Q 3-line to 8-line decoder/ demultiplexer is designed to be used in high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AHCT138Q-Q1	BQB (WQFN, 16)	3.5mm x 2.5mm	3.5mm x 2.5mm
	D (SOIC, 16)	9.9mm x 6mm	9.9mm x 3.9mm
	PW (TSSOP, 16)	5.00mm x 6.4mm	5.00mm x 4.40mm

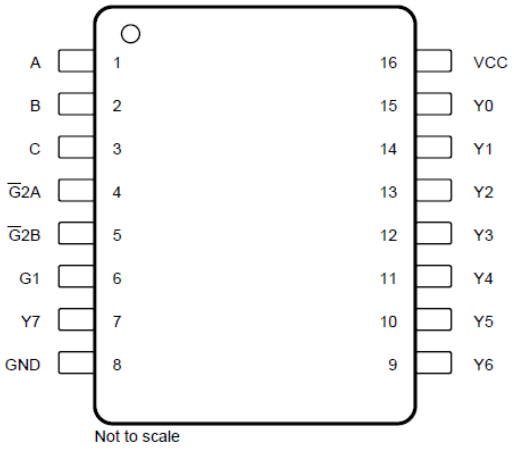
(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



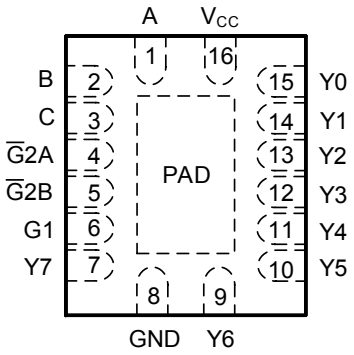
Logic Diagram (Positive Logic)

Table of Contents

3 Pin Configuration and Functions



D or PW Package, 16-Pin SOIC or TSSOP (Top View)



BQB Package, 16-Pin WBQB (Top View)

PIN		I/O[1]	DESCRIPTION
NAME	SOIC, TSSOP, WQFN		
A	1	I	Select input A (least significant bit)
B	2	I	Select input B
C	3	I	Select input C (most significant bit)
$\overline{G}$2A	4	I	Active low enable A
$\overline{G}$2B	5	I	Active low enable B
G1	6	I	Active high enable
GND	8	—	Ground
NC	—	—	No internal connection
V_{CC}	16	—	Supply voltage
Y0	15	O	Output 0 (least significant bit)
Y1	14	O	Output 1
Y2	13	O	Output 2
Y3	12	O	Output 3
Y4	11	O	Output 4
Y5	10	O	Output 5
Y6	9	O	Output 6
Y7	7	O	Output 7 (most significant bit)
Thermal pad[2]		The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.	

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.
(2) WBQB package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range		–0.5	7	V
V_O	Output voltage range		−0.5V	V_{CC} + 0.5	V
I_{IK}	Input clamp current(2)	V_I < 0		−20	mA
I_{OK}	Output clamp current(2)	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	
I_{OL}	Low-level output current		8	
Δt/Δv	Input transition rise or fall time		20	ns/V
T_A	Operating free-air temperature	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

4.4 Thermal Information

THERMAL METRIC(1)		SN74AHCT138Q-Q1			UNIT
		BQB (WQFN)	D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.6	73	135.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50µA		4.5V	4.4	4.5		4.4		V
	I_{OH} = −8mA			3.94			3.8		
V_{OL}	I_{OL} = 50µA		4.5V			0.1		0.1	V
	I_{OL} = 8mA					0.36		0.5	
I_I	V_I = 5.5V or GND		0 V to 5.5 V			±0.1		± 1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5V			4		40	µA
Δ_{ICC} 1	One input at 3.4 V, Other inputs at V_{CC} or GND		5.5V			1.35		1.5	mA
C_i	V_I = V_{CC} or GND		5V		2	10			pF

1. This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0V or V_{CC}.

4.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) See Load Circuit and Voltage Waveforms

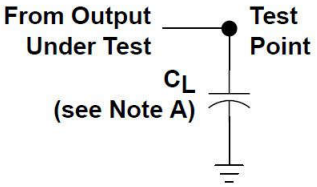
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}					7.6	10.4	1	12	
t_{PLH}	G1	Any Y	C_L = 15 pF		6.6	9.1	1	10.5	ns
t_{PHL}					6.6	9.1	1	10.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		7	9.6	1	11	ns
t_{PHL}					7	9.6	1	11	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

4.7 Operating Characteristics

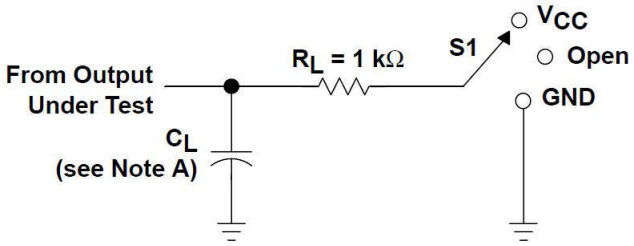
V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1MHz	14	pF

5 Parameter Measurement Information

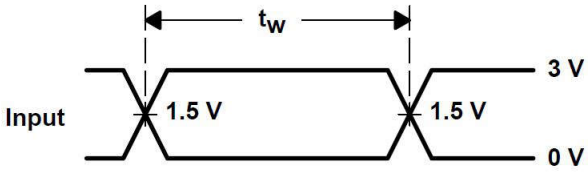


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

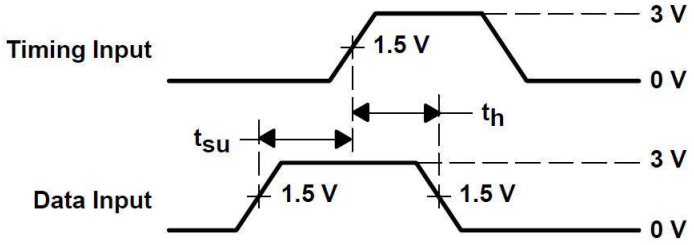


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

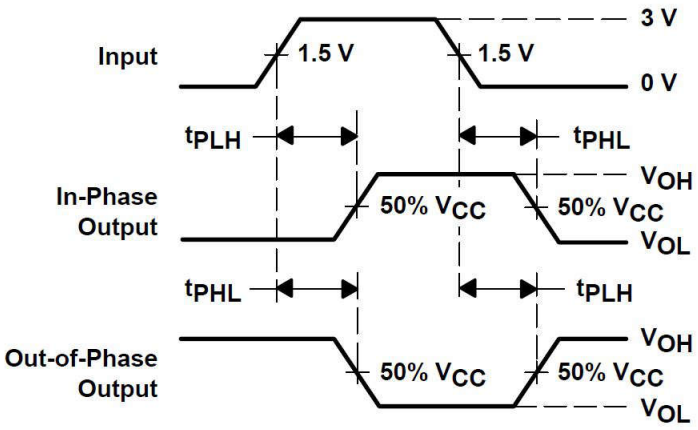
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



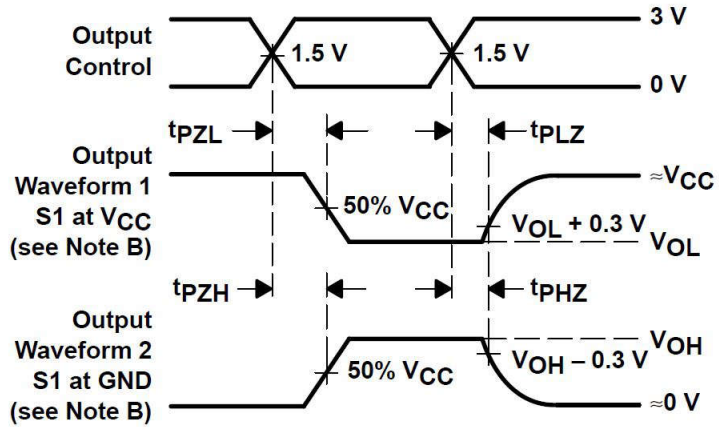
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_r ≤ 3ns, t_f ≤ 3ns.
E. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

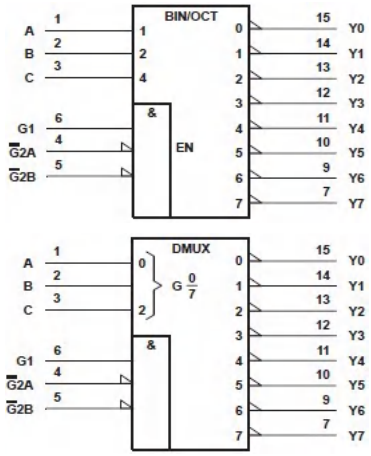
6 Detailed Description

6.1 Overview

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

6.2 Functional Block Diagram

Logic Symbols (Alternatives)



6.3 Device Functional Modes

Table 6-1. Function Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

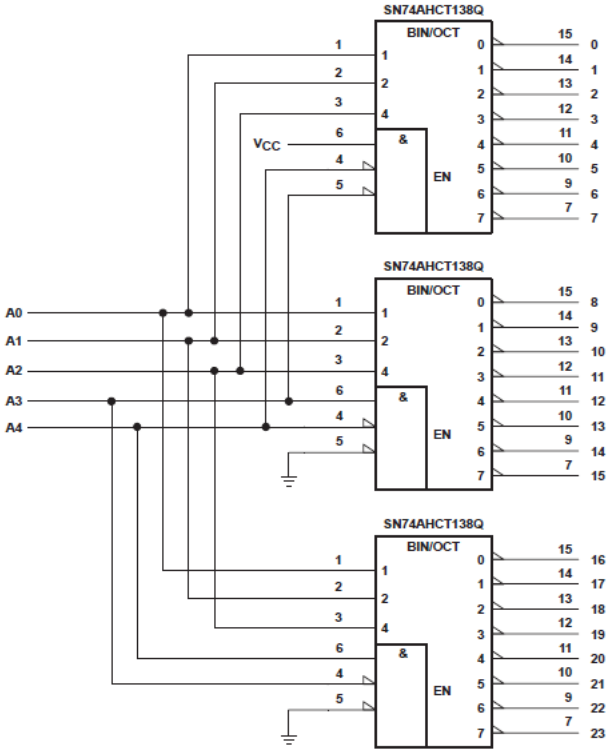


Figure 7-1. 24-Bit Decoding Scheme

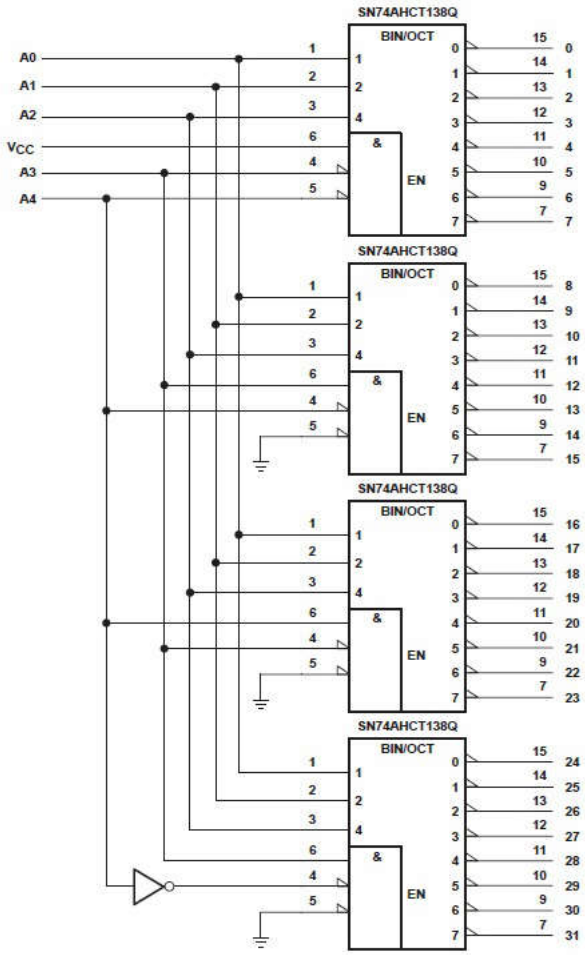


Figure 7-2. 32-Bit Decoding Scheme

7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 4.3*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1µF bypass capacitor is recommended to be placed close to the V_{CC} terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise; 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

7.3 Layout

7.3.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace (resulting in the reflection). It is a given that not all PCB traces can be straight, and so they have to turn corners. Figure 7-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

7.3.2 Layout Example

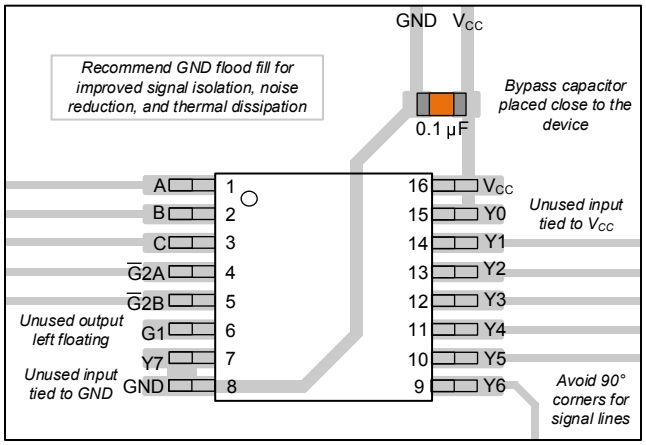


Figure 7-3. Example Layout for the SN74AHCT138Q-Q1

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

8.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT138Q-Q1	Click here	Click here	Click here	Click here	Click here

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2002) to Revision B (March 2024)	Page
• Added BQB package to *Package Information* table, *Pin Configuration and Functions*, and *Thermal Information* table	1
• Updated thermal value for PW package from RθJA = 108 to 135.9; added RθJC(top), ΨJT, ΨJB, all values in °C/W	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CAHCT138QPWRG4Q1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB138Q
CAHCT138QPWRG4Q1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB138Q
CAHCT138QWBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AT138Q
CAHCT138QWBQBRQ1.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AT138Q
SN74AHCT138QDRQ1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT138Q
SN74AHCT138QDRQ1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT138Q
SN74AHCT138QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT138Q
SN74AHCT138QPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT138Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

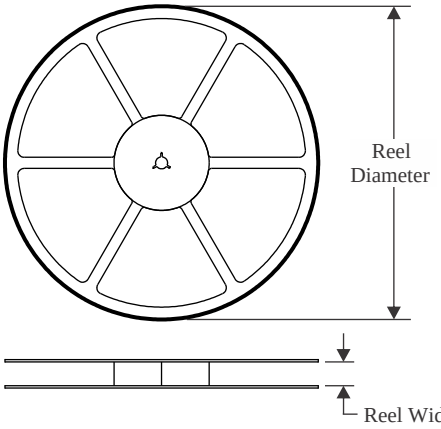
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

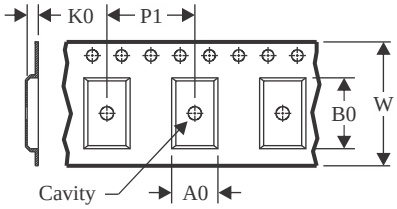
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

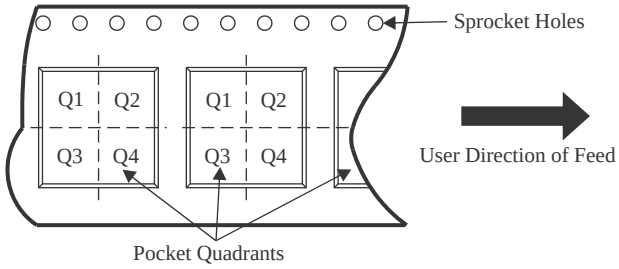


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

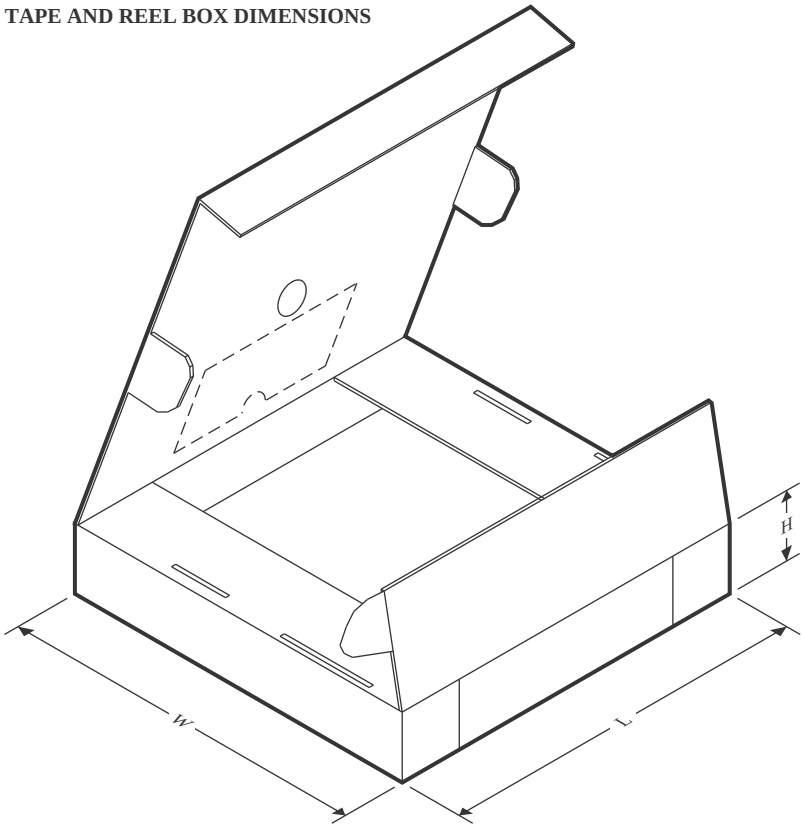
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT138QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CAHCT138QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AHCT138QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

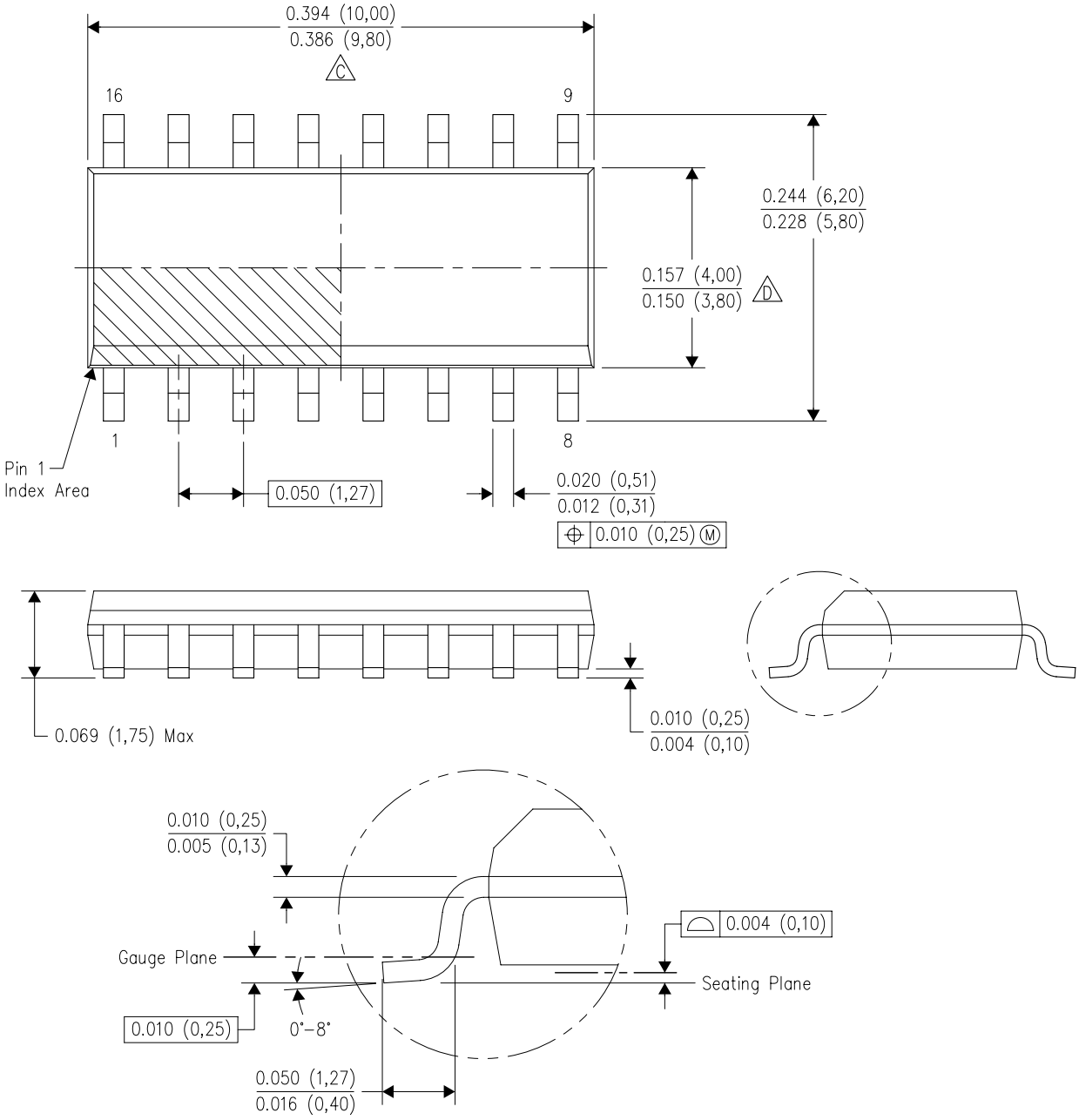
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT138QPWRG4Q1	TSSOP	PW	16	2000	353.0	353.0	32.0
CAHCT138QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AHCT138QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

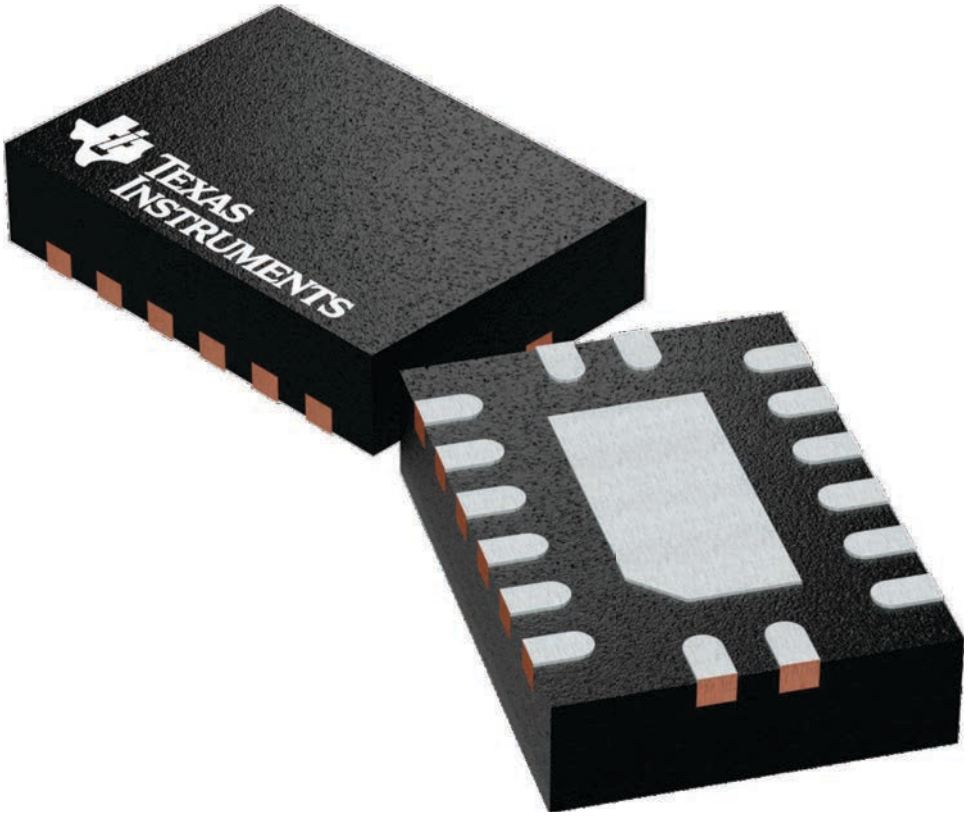
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



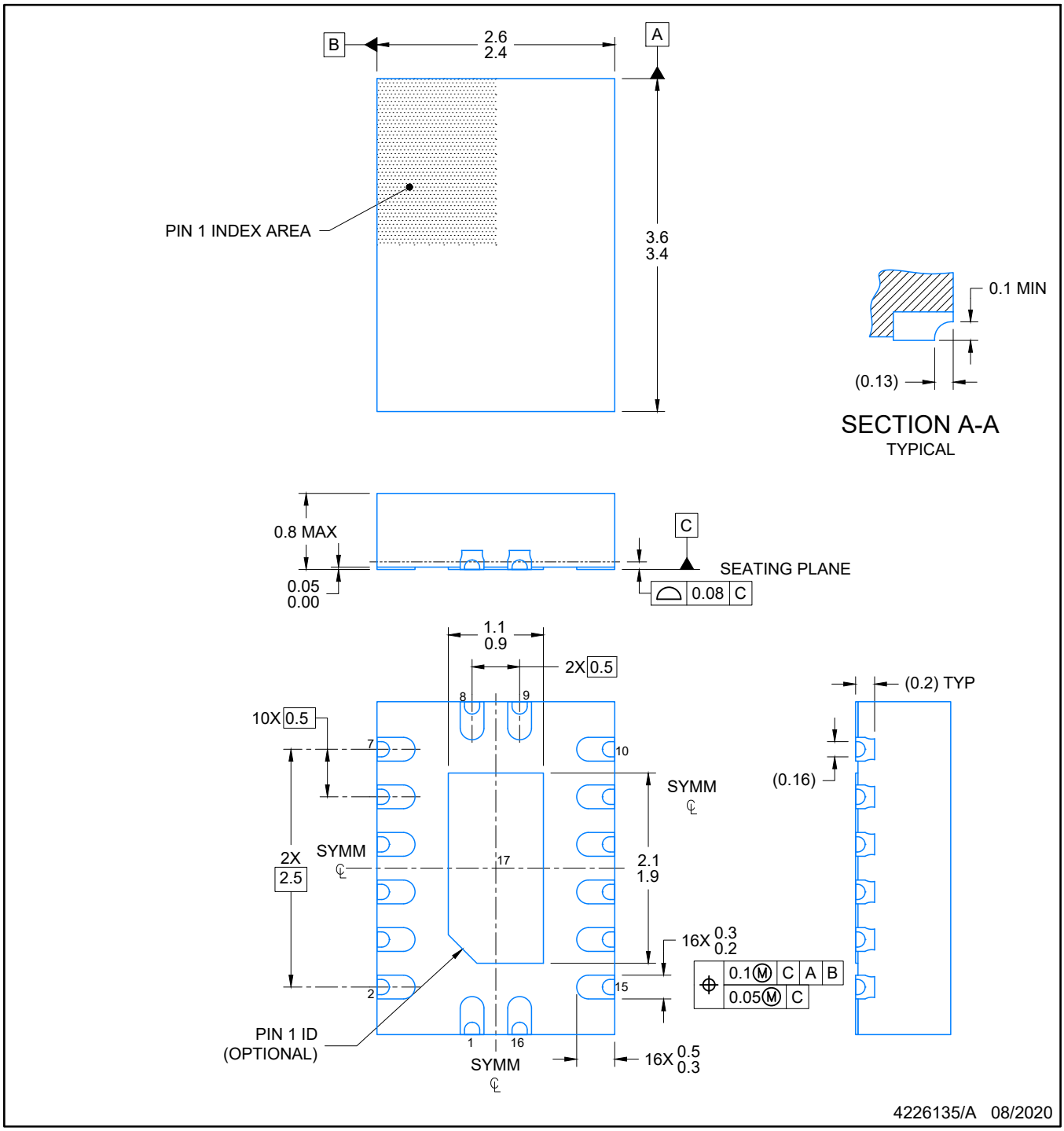
4226161/A

PACKAGE OUTLINE

BQB0016B

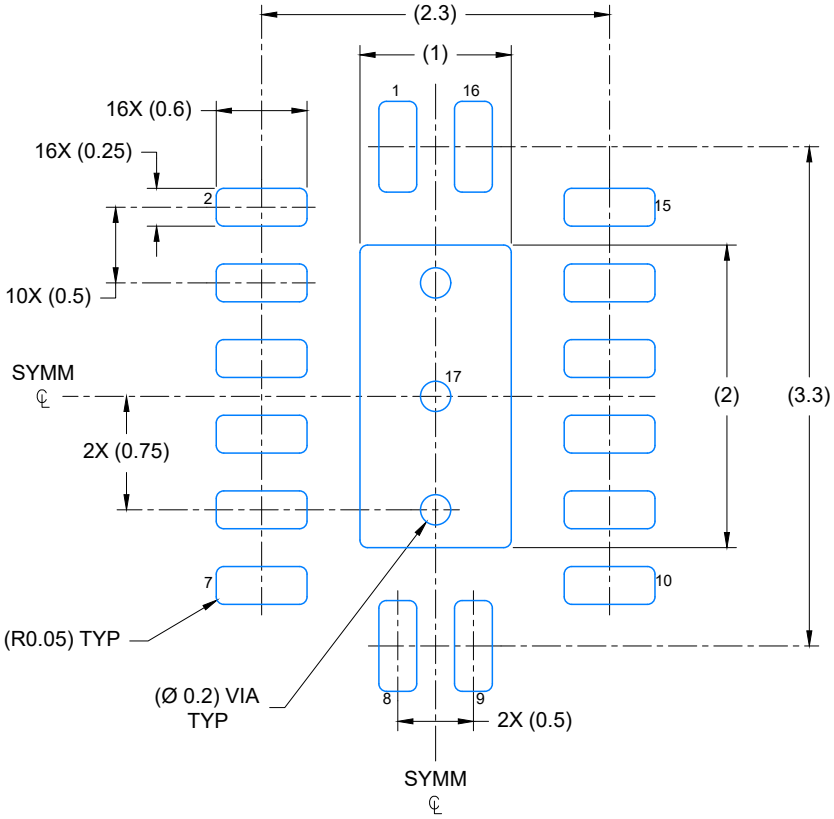
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

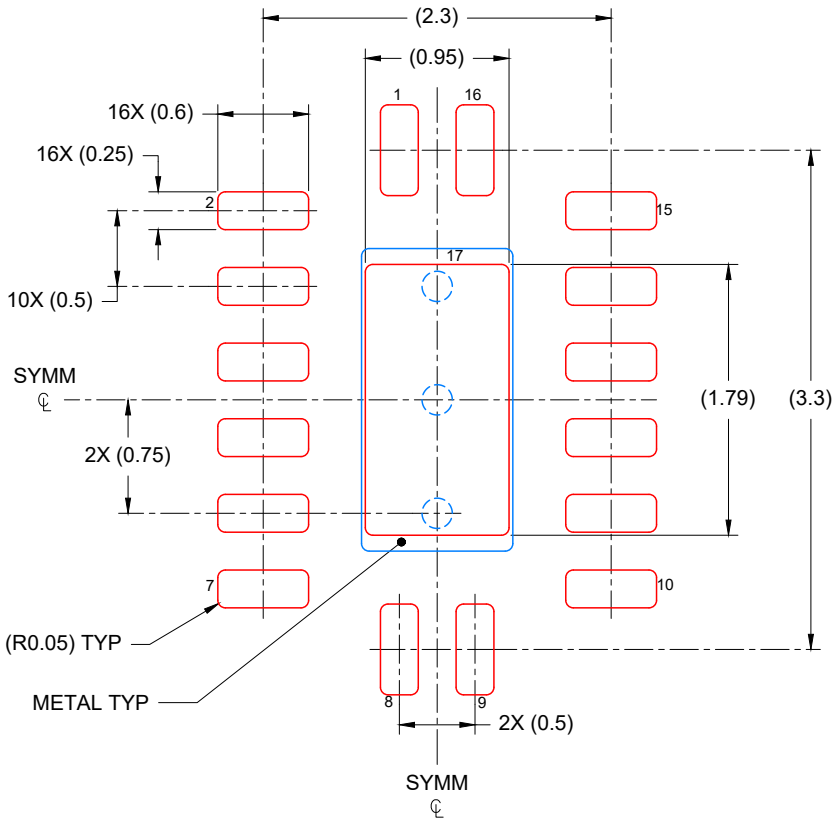


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

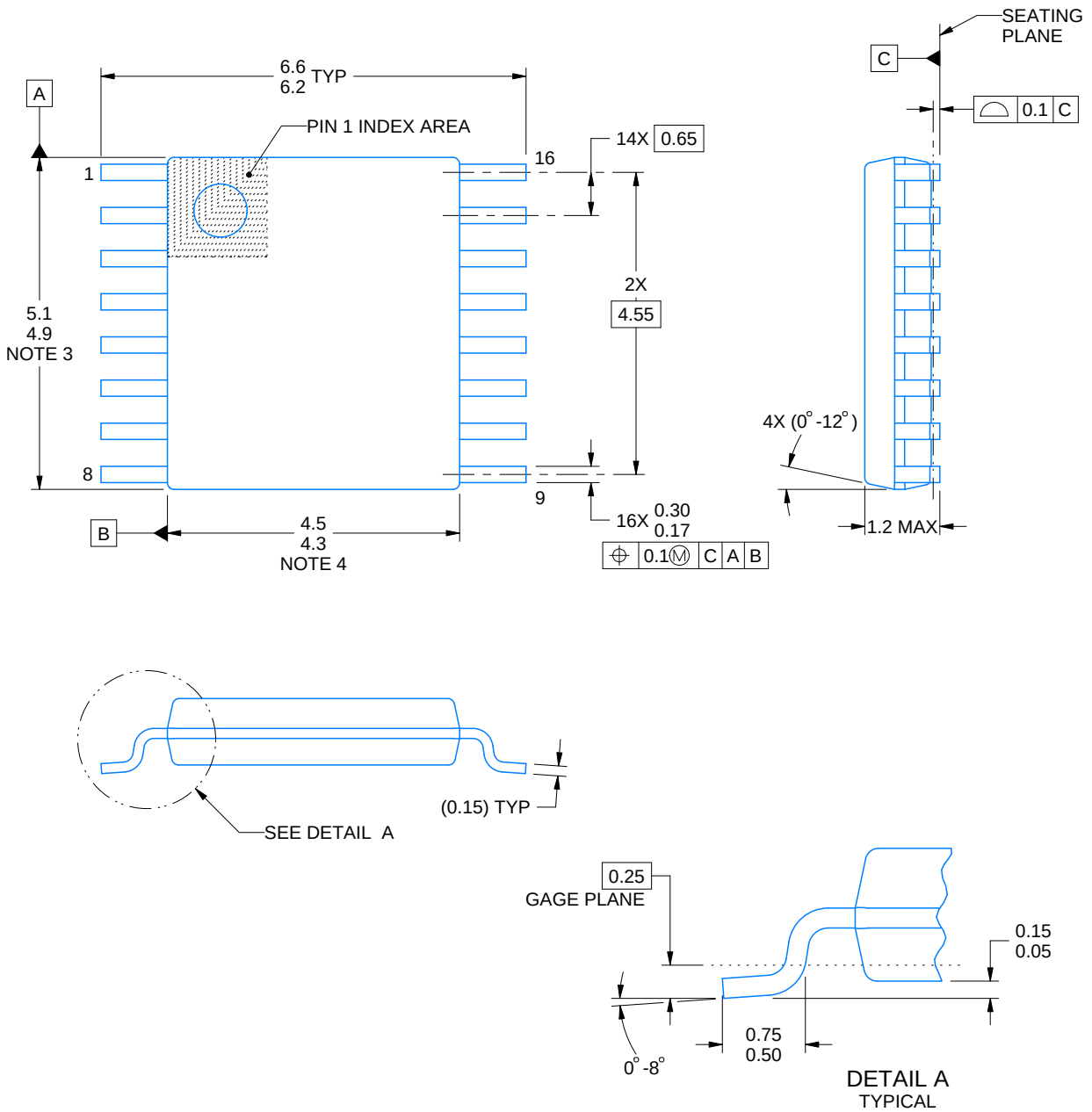
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

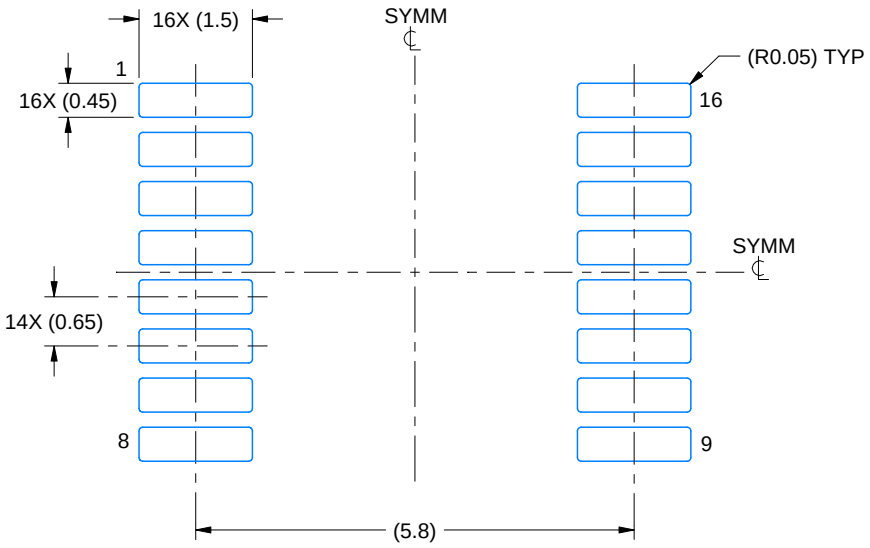
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



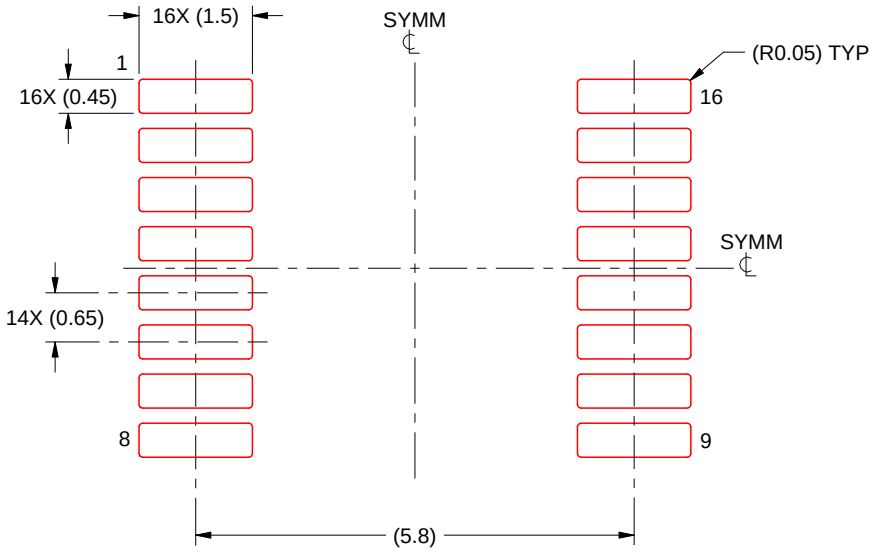
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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