









SN74AHC1G125

SCLS377M - AUGUST 1997 - REVISED FEBRUARY 2024

SN74AHC1G125 Single Bus Buffer Gate With 3-State Output

1 Features

- Operating range of 2V to 5.5V
- Max t_{pd} of 6ns at 5V
- Low power consumption, 10µA max I_{CC}
- ±8mA output drive at 5V

2 Applications

- **Projectors**
- TVs
- Servers
- Motor Controls: AC Induction
- **Patient Monitoring**
- Electronic Points of Sale

3 Description

The SN74AHC1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is high. When \overline{OE} is low, true data is passed from the A input to the Y output.

Package Information

PART NUMBER	PART NUMBER PACKAGE ⁽¹⁾		BODY SIZE(3)
	DBV (SOT-23, 5)	2.8mm × 2.8mm	2.9mm x 1.6mm
SN74AHC1G125	DCK (SC-70, 5)	2.00mm × 2.1mm	2mm × 1.25mm
	DRL (SOT-553, 5)	1.6mm x 1.6mm	1.6mm × 1.2mm

- For more information, see Section 11.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length x width) is a nominal value and does not include pins.

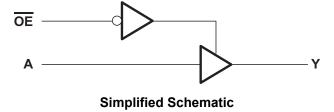


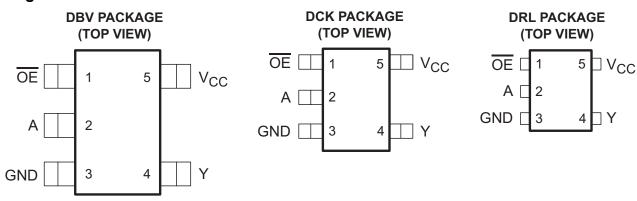


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4 Pin Configuration and Functions



See mechanical drawings for dimensions.

Table 4-1. Pin Functions

	PIN	TYPE ⁽¹⁾	DESCRIPTION			
NO.	NAME	I TPE\''	DESCRIPTION			
1	ŌĒ	I	Output Enable			
2	A	I	Input A			
3	GND	_	Ground Pin			
4	Y	0	Output Y			
5	V _{CC}	-	Power Pin			

(1) Signal Types: I = Input, O = Output, I/O = Input or Output



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I (2)	(2) Input voltage range				V
V _O (2)	Output voltage range	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous channel current through V _{CC} or GND		±50	mA	
T _{stg}	Storage temperature range	-65	150	°C	
TJ	Junction Temperature			150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1500	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		2	5.5	V	
		V _{CC} = 2 V	1.5			
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V	
		V _{CC} = 5.5 V	3.85			
		V _{CC} = 2 V		0.5		
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V	
		V _{CC} = 5.5 V		1.65		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 2 V		-50	μA	
I _{OH}	High-level output current	V _{CC} = 3.3 V ± 0.3 V		-4	mA	
		V _{CC} = 5 V ± 0.5 V		-8		
		V _{CC} = 2 V		50	μΑ	
I _{OL}	Low-level output current	V _{CC} = 3.3 V ± 0.3 V		4	mA	
		V _{CC} = 5 V ± 0.5 V		8	IIIA	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		
ΔΨΔν	input transition rise of fall fale	V _{CC} = 5 V ± 0.5 V		20	ns/V	

Product Folder Links: SN74AHC1G125

²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
T _A	Operating free-air temperature	-40	125	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

5.4 Thermal Information

			SN74AHC1G125					
	THERMAL METRIC ⁽¹⁾	THERMAL METRIC ⁽¹⁾ DBV (SOT-23, 5) DCK (SC-70, 5) ORL (SOT-553, 5)						
			5 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	328.7				
R _{0JC(top)}	Junction-to-case (top) thermal resistance	180.5	205.8	105.1				
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	176.2	150.3	°C/W			
ΨЈТ	Junction-to-top characterization parameter	115.4	117.6	6.9	C/VV			
ΨЈВ	Junction-to-board characterization parameter	183.4	175.1	148.4				
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A				

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEST			_ = 25°C		-40°C to	85°C	-40°C to	125°C	UNIT
	PARAMETER	CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			2 V	1.9	2		1.9		1.9		
		I _{OH} = –50 μA	3 V	2.9	3		2.9		2.9		
V _{OH}	High level output voltage		4.5 V	4.4	4.5		4.4		4.4		V
		I _{OH} = −4 mA	3 V	2.58			2.48		2.48		
		I _{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
			2 V			0.1		0.1		0.1	
	Low level output voltage	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
V _{OL}			4.5 V			0.1		0.1		0.1	V
		I _{OL} = 4 mA	3 V			0.36		0.44		0.44	
		I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
I	Input leakage current	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μA
I _{OZ}	Off-State (High-Impedance State) Output Current (of a 3- State Output)	V _I = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μА
I _{CC}	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10		10	μA
Ci	Input capacitance	V _I = V _{CC} or GND	5 V		4	10		10		10	pF
Co	Output capacitance	V _O = V _{CC} or GND	5 V		10						pF



5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

DADAMETED	PARAMETER FROM TO LOAD		LOAD		T _A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT		
t _{PLH}	Α	Y	C ₁ = 15 pF	·	5.6	8	1	9.5	1	10.5	ns		
t _{PHL}			О[– 13 рі	·	5.6	8	1	9.5	1	10.5	115		
t _{PZH}	ŌĒ	Y	C ₁ = 15 pF	·	5.4	8	1	9.5	1	10.5	ns		
t _{PZL}	- OE		О[– 13 рі	·	5.4	8	1	9.5	1	10.5	115		
t _{PHZ}	ŌĒ	Y	C _L = 15 pF	·	7	9.7	1	11.5	1	12.5	ns		
t _{PLZ}	OE .	OL	OL	ı	С[– 13 рі	·	7	9.7	1	11.5	1	12.5	115
t _{PLH}	А	Y	C ₁ = 50 pF	·	8.1	11.5	1	13	1	14	ns		
t _{PHL}	^		оլ – 50 рі	·	8.1	11.5	1	13	1	14	115		
t _{PZH}	ŌĒ	Y	C _L = 50 pF	·	7.9	11.5	1	13	1	14	ns		
t _{PZL}	- UE	I I	о_ – 50 рі	·	7.9	11.5	1	13	1	14	115		
t _{PHZ}	ŌĒ	Y	C _L = 50 pF		9.5	13.2	1	15	1	16	ne		
t _{PLZ}	OE .	ľ	OL - 50 PF		9.5	13.2	1	15	1	16	ns		

5.7 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER FROM TO		то	LOAD	Т	A = 25°C		-40°C to 8	55°C	-40°C to 125°C		UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
t _{PLH}	А	Y	C ₁ = 15 pF		3.8	5.5	1	6.5	1	7	ns
t _{PHL}		l	OL = 13 pi		3.8	5.5	1	6.5	1	7	115
t _{PZH}	ŌĒ	Y	C _L = 15 pF		3.6	5.1	1	6	1	6.5	ns
t _{PZL}	- OE	·	OL - 10 pi		3.6	5.1	1	6	1	6.5	113
t _{PHZ}	ŌĒ	Y	C ₁ = 15 pF		4.6	6.8	1	8	1	8.5	ns
t _{PLZ}	OL	l	OL = 13 pi		4.6	6.8	1	8	1	8.5	115
t _{PLH}	Α	Y	C ₁ = 50 pF		5.3	7.5	1	8.5	1	9.5	ns
t _{PHL}		l	С[– 30 рі		5.3	7.5	1	8.5	1	9.5	115
t _{PZH}	ŌĒ	Y	C ₁ = 50 pF		5.1	7.1	1	8	1	9	ns
t _{PZL}	JOE	l	С[– 30 рі		5.1	7.1	1	8	1	9	115
t _{PHZ}	ŌĒ	Y	C _L = 50 pF		6.1	8.8	1	10	1	11	ns
t _{PLZ}	OE .	ľ	OL - 50 pr		6.1	8.8	1	10	1	11	115

5.8 Operating Characteristics

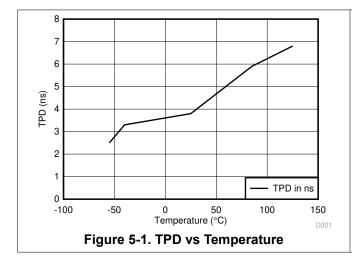
 $V_{CC} = 5 \text{ V}, T_{A} = 25^{\circ}\text{C}$

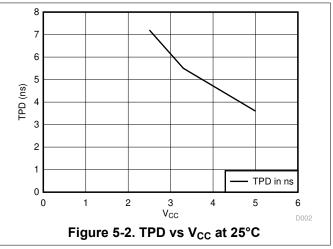
PARAMETER		TEST CON	DITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

Product Folder Links: SN74AHC1G125



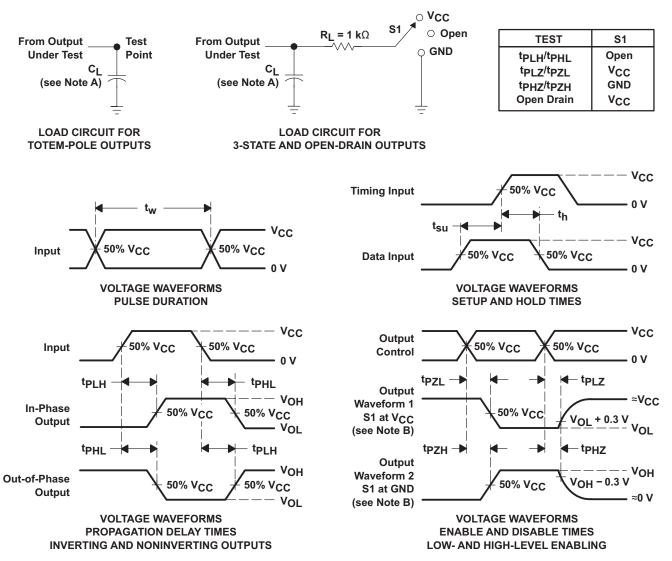
5.9 Typical Characteristics







6 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , $t_f \leq$ 3 ns. $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74AHC1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

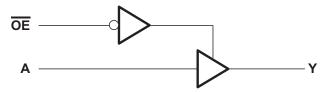


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- · Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V

7.4 Device Functional Modes

Table 7-1. Function Table

INPUT	S ⁽¹⁾	OUTPUT ⁽²⁾
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74AHC1G125 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5~V at any valid V_{CC} making it Ideal for down translation.

8.2 Typical Application

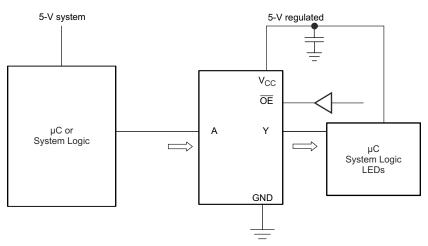


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Product Folder Links: SN74AHC1G125

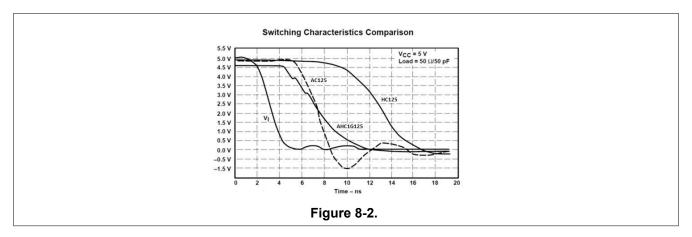
8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the Section 5.3 table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the Section 5.3 table.
- 2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

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8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 5.3 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.1.1 Layout Example

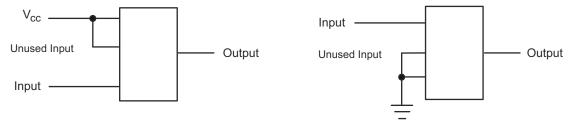


Figure 8-3. Layout Diagram



9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision L (October 2023) to Revision M (February 2024)

Page

Changes from Revision K (December 2014) to Revision L (October 2023)

Page

Product Folder Links: SN74AHC1G125



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74AHC1G125DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A25G
74AHC1G125DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A25G
74AHC1G125DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A25G
74AHC1G125DBVTE4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A25G
74AHC1G125DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A25G
74AHC1G125DBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A25G
74AHC1G125DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM3
74AHC1G125DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM3
74AHC1G125DCKTG4	Obsolete	Production	SC70 (DCK) 5	-	-	Call TI	Call TI	-40 to 125	AM3
SN74AHC1G125DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39HH, 3BXF, A253, A25G, A25J, A 25L, A25S)
SN74AHC1G125DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39HH, 3BXF, A253, A25G, A25J, A 25L, A25S)
SN74AHC1G125DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	(A253, A25G, A25J, A25S)
SN74AHC1G125DCK3	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	AMY
SN74AHC1G125DCK3.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	AMY
SN74AHC1G125DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1RB, AM3, AMG, AM J, AML, AMS)
SN74AHC1G125DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1RB, AM3, AMG, AM J, AML, AMS)
SN74AHC1G125DCKT	Obsolete	Production	SC70 (DCK) 5	-	-	Call TI	Call TI	-40 to 125	(AM3, AMG, AMJ, AM S)
SN74AHC1G125DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AMS
SN74AHC1G125DRLR.A	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AMS

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHC1G125:

Automotive: SN74AHC1G125-Q1

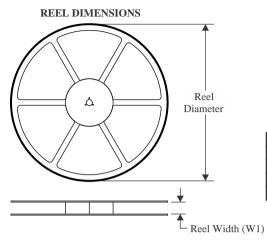
NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHC1G125DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHC1G125DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G125DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AHC1G125DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHC1G125DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHC1G125DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G125DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHC1G125DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHC1G125DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-293 Variation UAAD-1



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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